PHYTEC

miniMODUL-166

Hardware-Manual

Edition April 2001

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Preface

This miniMODUL-166 Hardware Manual describes the board's design and functions. Precise specifications for the SAB 80C166 microcontroller can be found in the enclosed microcontroller Data-Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration regarding EMV-Conformity of the PHYTEC miniMODUL-166

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

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PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the EMVG-statute only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

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The miniMODUL-166 is one of a series of PHYTEC Single Board Computers that can be fitted with different controllers and, hence, offers various functions and configurations.
PHYTEC supports all common 8- and 16-bit controllers in two ways:

(1) as the basis for Rapid Development Kits in which user-designed hardware can be implemented on a wrap-field around the controller and

(2) as insert-ready, fully functional micro-/mini- and phyCORE modules which can be embedded directly into the user's peripheral hardware design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market. Please contact PHYTEC for additional information:

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1 Introduction

The miniMODUL-166 presents a highly affordable, compact and functional solution to a wide range of real-time embedded control applications. The Infineon SAB80C166 controller as the on-board CPU offers high performance (100 ns instruction cycles at 40 MHz CPU clock) and extensive peripheral functionality. The controller can operate in three configurable controller modes: 16-bit multiplexed, 16-bit non-multiplexed and single chip mask-programmed.

The standard board offers 256 kByte external SRAM and 256 kByte external Flash memory for DATA and CODE storage. The miniMODUL-166 has two RS-232 interfaces, one of which can be configured as RS-485 for network connectivity.

All controller signals and ports extend from the controller to standard-width (2.54 mm) pin header rows aligning three edges of the board, allowing it to be plugged like a "big chip" into a target application. Precise specifications for the controller populating the board can be found in the applicable controller User's Manual or Data Sheet.

The miniMODUL-166 offers the following features:

- single board computer in credit card-size dimensions (55 x 85 mm) populated with the 16-bit microcontroller SAB80C166 from Infineon
- minimum instruction cycles of 100 ns at 40 MHz CPU-clock
- multi-layer PCB (6 layers) populated with components in advanced SMD technology
- flexible address decoding via PLD, customer-specific memory models available on request
- flexible memory configuration
- maximum controller address space of 256 kByte
- 128 kByte socketed EPROM in LCC32 packaging
- 256 kByte SRAM

- max. 256 kByte FLASH-EPROM (5 V or 12 V) in PLCC32 packaging
- RAM bank switching possible using freely available port lines
- on-board programming of FLASH-EPROM devices, booting of application software via RS-232/RS-485 interface
- integrated BOOT of the SAB80C166 on mask revision CB and higher
- two RS-232 serial interfaces, one optionally configurable as RS-485 for networking purposes
- two free 16-bit controller ports (mode-dependent)
- address latch serves as an additional output port in non-multiplexed mode
- 12-channel A/D converter with 10-bit resolution
- all controller ports and signals extend to standard-width (2.54 mm) pins aligning three edges of the board
- three controller modes available: 16-bit multiplexed, 16-bit non-multiplexed or mask programmed single chip mode
- buffered data bus, buffered address bus (A0...A15)
- requires single 5 V/<250 mA power supply
- operates in a temperature range from 0 to 70°C.

Caution:
The miniMODUL-166 has been redesigned. Due to this redesign, changes in the jumpers have resulted. Furthermore, the memory models differ from those on the older model. Additional information on these changes can be found in the *AII Revision History", Changes*.

2 Hints for Using the Module

2.1 Absolute Processing Speed

In contrast to other standard products from PHYTEC, the absolute processing speed of the miniMODUL-166 depends on the current supply of high-speed memory devices in the market. At the time of initial creation of this manual (Feb. ’93) it was not possible to get fast memory devices of high capacity and short delivery time in all packaging variants. Although availability of FLASH-EPROM devices allow new application and offer various advances, access times of currently 150 ns cause some limitations on the processing speed. This must be taken into consideration and accepted in the case of the miniMODUL-166 for the time being.

In order to enable operation with such lower speed FLASH-EPROM devices the controller generates WAIT states when accessing external memory. The number of WAIT states can be configured via user software. Inserting one WAIT state increases the access time by 50 ns at an oscillator frequency of 40 MHz.

PHYTEC tries to achieve a compromise between speed and deliverability in our standard products. This compromise consists of the following:

- For applications with EPROM (LCC32) devices offering access times of about 70..90 ns, 0..1 WAIT states (0..50 ns) are required.

- For applications with FLASH-EPROM (PLCC32) devices offering access times of 150 ns, one or two WAIT states (50..100 ns) are required.

Due to the high performance of the controller, addition of up to two WAIT states is not a problem for most applications.

2.2 Application Fields

In developing the miniMODUL-166, we strove to achieve an optimized space/efficiency ratio. The new FLASH technology was also taken into consideration. The available memory space has been expanded in order to support applications with very specific requirements on the memory model. Use of flexible PLDs with an additional control input allows memory banking functions. Applications where a download of resident software is desired are also possible with this module. Such application software can be permanently stored in the module‘s FLASH-EPROM without the need of an additional buffer battery when the power supply is shut off. This enables, for example, software updates via a modem. A more detailled description of these new features is porvided in various sections of this manual.

2.2.1 Bus Modes

The miniMODUL-166 supports all 16-bit bus modes. These are:

- Single chip mode of the SAB80C166 (mask-programmed)
- 16/18-bit address bus, 16-bits data bus multiplexed. The microcontroller address remains P1 and free for use. It is available at the connection port X[0..15].
- 16/18-bit address bus, 16-bits data bus non-multiplexed. The microcontroller address P1 for the address bus is occupied. The address latch U2/U3 is available in this case address X[0..15] at the connection field. Address latch and P1 are available at X[0..15] alternatively.

Note:
The 8-bit mode is not supported.

The mode of operation can be selected by setting appropriate solder jumpers. This is set as the default at the factory, and can later be changed by the solderable Jumpers J1, J2, J3 and J6.

2.2.2 Memory Configuration

Memory configuration is variable within certain limits by using a PLD as an address decoder. The PLD has two additional control inputs (/BOOT, MODE), with which dynamic switching of the memory model or the selection of alternative models are possible while the program is running.

The relatively large number of memory devices available to the controller allows for considerable memory expansion, since the controller itself is only capable of addressing 256 kBytes. There is a maximum of two 64 kByte EPROM (LCC32) devices on U6/U7, optionally two of each 32...256 kByte PLCC FLASH-EPROM or OTPROM on U8/U9 and a total of 256 kByte RAM on U4/U5. The possibility of memory expansion in conjunction with the control inputs (/BOOT, MODE) of the decoder leaves additional combination options open during memory configuration. For applications with extensive application code the RAM can be divided into four 64 kByte blocks each controlled by port signals.

Configuration examples:

- Normal operation with 128 kByte EPROM and 256 kByte RAM, switchable in 128 kByte blocks
- The same also with PLCC FLASH EPROM for resident software download.
- Optional operation without EPROM via the *Download* option over the serial interface (starting from controller mask CB) in RAM.
- Operation of FLASH-EPROM with BOOT sector (64...256 kByte) and RAM utilizing the BOOT option from the BOOT sector of the FLASH-EPROM. User-specific BOOT programs can be loaded via any available interface. Separate erasure of the main program and resident reprogramming. The BOOT program can be maintained, but can be changed if desired.

- Operation of EPROM (LCC32) and smaller FLASH-EPROM for "reloading" and "exchange" of resident subroutines.
- In this case small RAM area of 64 kByte, but with a maximum of four banks selectable by two port pins.

The assignment to the different memory banks occurs depending upon the application with the special address decoder PLD, if the blocks are not to small, and the number of logical equations within the PLD is sufficient. A software controlled switching of the PLD mode over a port pin is also possible.

The RAM address inputs A15 and A16 can be connected alternatively to any available port lines, whereby the possibility for bank switching remains available (for example, applications collecting measuring data up to 256 kByte).

2.2.3 Power-On Jump Mode

With the Power-On Jump function the start of user programs in higher addresses (e.g. 10000H, 20000H) is possible. This is especially useful when utilizing a monitor program to download a user program.
For the Power-On Jump mode the assembly of a suitable PLD U15 is necessary.

The PLD U15 is programmable to customer specifications. The desired memory model should always be indicated when purchasing the module.

2.2.4 Booting and Downloading Resident Programs

A) Booting with an optional FLASH-EPROM

When using FLASH-EPROMs, e.g. NTEL 28F001BX-B a program start is possible via a jump indicator in the BOOT-sector at address 0000H. In the BOOT sector an additional BOOT program can be accommodated, which permits the deletion of the FLASH EPROMs in the program sector and the reprogramming of a new resident user program, which remains in powered down state. For downloading, an RS-232 interface or a parallel port are possible options. When using the RS-485 interface, downloads are also possible within interlaced controller boards.

The BOOT function can be generated thereby from the main program or with RESET via a request from a port line or a serial interface. An appropriate routine can be a firm component of the software in the BOOT sector of the FLASH-EPROMs. The BOOT sector is likewise reprogrammable with appropriate Jumpering.
This data refers particularly to the FLASH-EPROM 28F001BX-B from INTEL. With components of other manufacturers similar proceedings are possible, if these have at least two separated erasable memory areas.
The assembly with 28F001BX-B is optional and results in a surcharge.

B) BOOT with the controller‘s internal BOOT function from Infineon

Starting from mask version CB of the SAB80C166 the controller itself provides a BOOT function, which is released under certain conditions for hardware after RESET. With this boot function it is possible to load 32 Byte of a user program over the serial interface into the controller’s internal RAM.

This procedure is generated by RESET and /NMI, as soon as the ALE output of the module is held to GND level via external circuitry.

3 Initial Startup

The most important connection elements and the minimum circuitry requirements are represented in the following figures.

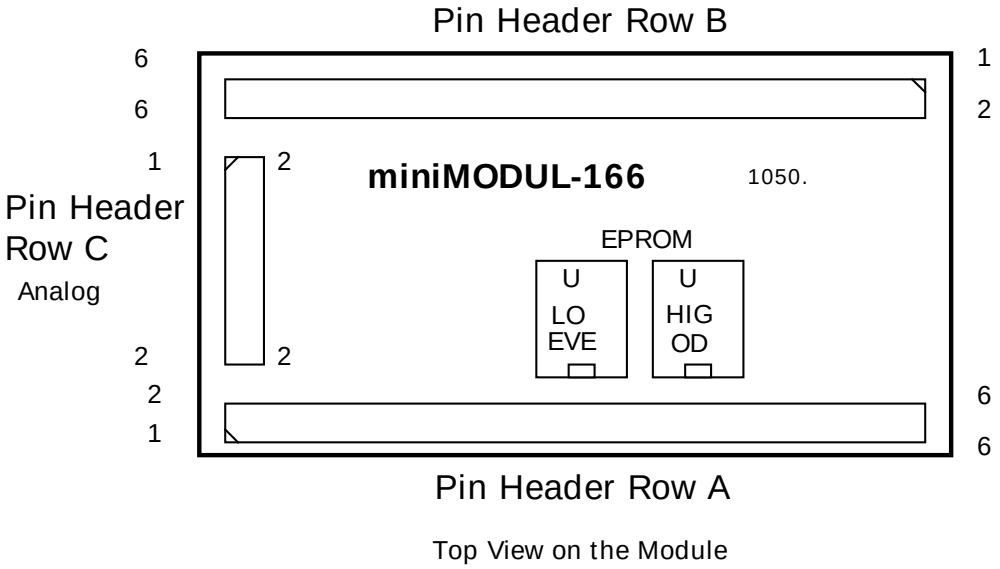


Figure 1: Connection Elements of the miniMODUL-166

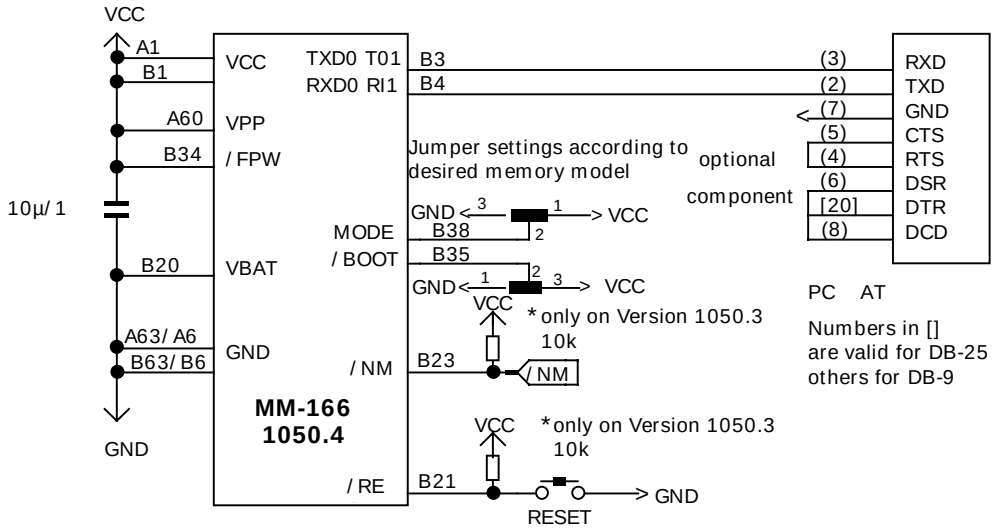


Figure 2: Minimum Circuitry Requirements for the miniMODUL-166

3.1 Jumper Settings

The miniMODUL-166's jumpers are located on the component side in the standard version. If software is included with the module, the jumpers are set according to the software requirements.

If software is not included with the module, the jumpers will be preset according to requirements for module testing. In this case, it may be necessary to make adjustments according to instructions in *section 6*.

Note:
In particular it is important to make sure that Jumper J9 is set corresponding to the EPROM capacity.

3.2 Connecting the Supply Voltage

The regulated supply voltage VCC (5 V) is connected to the corners of the connector field shown above.

A1, A2	+ 5 V linear regulated
B1, B2	+ 5 V linear regulated
A63, A64	GND
B63, B64	GND

The power input is below 250 mA with 25C during normal operation. During the programming of FLASH EPROM it is at least 60 mA higher. Only a regulated supply voltage may be used. Reverse polarity or temporary overvoltage will destroy the miniMODUL-166.

Caution:
Do not use laboratory power supplies with adjustable output voltage. These can deliver overvoltage during a power failure or power down. We recommend the use of standard, linear 5 V voltage regulator. If a switching regulator must be used, we recommend the installation of a suppressor diode between VCC and GND. The switching regulator should not generate any spikes during a power on or power off.

If no battery is attached to the miniMODUL-166, the battery voltage input VBAT (B20) should be connected to GND.

If FLASH-EPROM are connected but are not to be programmed, inputs /FPWD (B34) and VPP (A60) must be connected to VCC.

3.3 Connection to the PC Interface COM1 or COM2

The miniMODUL-166 comes with an RS-232 serial interface on the connector field (B3, B4). This interfaces only uses signals TXD (TO1, B3), RXD (RI1, B4) and GND, no handshake signals. The RS-232 interface is delivered fully functional. The additional handshake signals on the PC-connector shown in *Figure 2* are only optional and are not required with standard software.

With a correctly attached interface there is a constant negative voltage between -6 and –12 V connected to ground.

The function of the interface requires an executable program in the program memory of the miniMODUL-166, for example a monitor program, as well as a suitable PC program for communication between the PC keyboard and the PC's serial interface. Additional information on installed programs should be included in appropriate software manuals.

3.4 Circuitry for MODE and /BOOT Contoller Inputs

The miniMODUL-166 is usually eqipped with an address decoder that has multiple memory models available. A specific model is selected via the MODE (B38) and /BOOT (B35) input circuitry.

Since the setting depends on the PLD's programming and the applied software, refer to the *Memory Model Supplement* and separate software description for additional information.

3.5 Operation with Factory-Installed Software

The MODE and /BOOT control inputs should be switched according to supplemental information or the software description. Other than the minimum circuitry requirements given above, no additional settings or precautions are necessary. The program is active after a /RES signal has been generated. Refer to the software manual for additional information on the software.

3.6 Operation with User Software

The miniMODUL-166 comes without standard software. All software has to be installed by the user. It is important to be aware of the following points which will be discussed more detailled in subsequent sections.

- The controller bus mode is preset with J3 on 16-bit, non-multiplexed.
- The source of address signal is preset at P1 with Jumpers J1 and J2, non-multiplexed.
- Adjust the Jumper J9 according to EPROM types used.
- Select the memory model, as in *section 5* or in *Supplemental Information Memory Model*, by wiring the signal inputs / BOOT (B35) and MODE (B38) with GND or VCC.
- Link your program accordingly and connect the programmed EPROM to U6/U7.

3.7 Mounting the Program Memory

This section can be skipped if the miniMODUL-166 came with fully operational software. After control inputs MODE (B38) and /BOOT (B35) have been correctly switched and an /RES signal (B21) has been generated, the miniMODUL-166 is ready for use. Consult the manual for the installed software for additional information.

The miniMODUL-166 requires two EPROMs in LCC32 packaging with 32 or 64 kByte capacity each on U6/U7 or two FLASH-EPROMs U8/U9, 32, 64 or 128 kBytes each as programming memory. If the miniMODUL-166 comes with standard software (monitor program), the program is already located in EPROM or FLASH-EPROM. In this case the miniMODUL-166 is fully operational, as long as the PLD control inputs and serial interfaces are connected correctly, as shown in *Figure 2*. Open control inputs automatically carry a logic HIGH level. Please refer to the appropriate software manual and additional address decoder information before start up.

The miniMODUL-166 is preset to 64 kByte EPROM for U6 and U7. The EVEN-EPROM (even-numbered address, low order code byte) needs to be inserted in the socket at U6. U6 is located next to the controller U1.

4 Description of the Module Connectors

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

The digital module connections are located on the pin header rows A and B. The analog signals extend to header row C (*see Figure 3*). The connections are arranged in the 2.54 mm pitch. A dimensional drawing can be found at the end of this manual. Correct pin assignment is shown in the figure below:

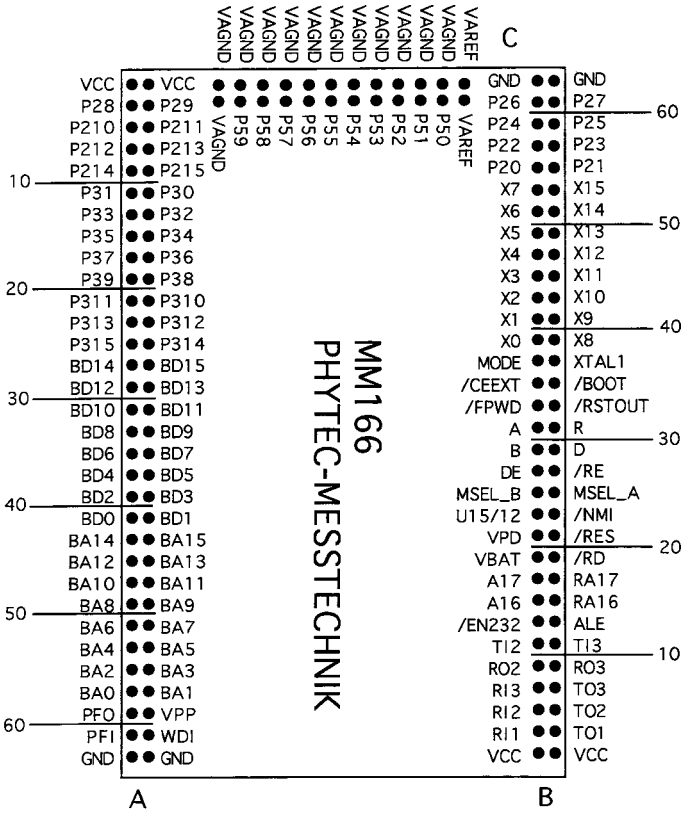


Figure 3: Pinout of the miniMODUL-166

4.1 The Pin Header Rows A and B

The pin header rows have 64 connectors each. The odd-numbered connections are in the outer row. All even-numbered connections are on the inner row. Header numbers increase from left to right. The connectors are organized in a logical fashion. The individual signal functions are listed below.

Module Supply Voltage

A1, A2, B1, B2:	VCC (5 V, approx. 250 mA)
A63,A64,B63,B64:	GND

P20..P215 (B55..B62, A3... A10)

Controller port P2. Data from the controller manual applies.

P30..P315 (A11..A25)

Controller port P3. Data from the controller manual applies. This port generates the following signals:

/ WR	P313 (A23)
/ READY	P314 (A26)
TXD0	P310 (A22)
RXD0	P311 (A21)
TXD1	P38 (A20)
RXD1	P39 (A19)

Buffered Data Bus BD0..BD15 (A27..A42)

External circuit expansions can be attached only to the buffered data bus. The Data buffer U10/U11 (74HCT245) is bi-directional and is activated by the control signal / CEEXT. Refer to the *Supplemental Memory Model Sheet* for detailled information about the address range in which the buffer is active.
The electrical specifications from the buffered data bus BD0..BD15 are located in the 74HCT245 data sheet.

Buffered Address Bus BA0..BA15 (A43..A58)

External circuit expansions can be attached only to the buffered address bus. It is important to note that address bits A16 and A17 are not buffered.
The electrical specifications from the buffered data bus BD0..BD15 are located in the 74HCT245 data sheet.

Power-Fail Input PFI (A61) and output PFO (A59)

PFO and PFI belong to the monitoring component U17.
The output PFO goes to low level, as soon as the voltage on the input PFI dropss below the reference threshold. This output's function is described in more detail in *section 8*. Before establishing user target circuitry with PFI/PFO, we recommend consulting the appropriate component manufacturer's data sheet.

Watchdog Input WDI (A62)

The Watchdog input WDI is connected to the supervisory IC at U17. In addition, it also controls the Watchdog timer on U17, which has a time constant of 1.6 seconds. The timer is inactive as long as the input is not connected. Additional information can be found in *section 8* or in the manufacturer's data sheet for this device.

Programming Voltage Input VPP (A60)

The programming voltage input VPP is supplied with either 12 V or 5 V as needed for programming of the FLASH-EPROM U8/U9. In an inactive state this connection should carry VCC level. It is recommended to connect a block capacitor between VPP and GND directly on the module.

RS-232 Interface RI1, TO1 (B4, B3)

This is the activated serial interface SERIAL0. RI1 (RXD0) is the RS-232 input, TO1 (TXD0) is the RS-232 output. These connections are protected against temporary overvoltages up to at least 2 kV. The manufacturer data for the specific U16 device is applicable.

RS-232 Transmitters/Receivers RI2, RO2, TO2, TI2, RI3, RO3, TI3, TO3

RIx Receiver input x, RS-232 level
ROx Receiver output x, TTL-level
TIx Transmitter input x, TTL-level
TOx Transmitter output x, RS-232 level

It is recommended to connect unused TTL-inputs TIx to a defined potential.

RS-232 Transceiver Shutdown / EN232 (B14)

The RS-232 Transmitter/Receiver can be switched off with this input, if VCC is connected. U16 is active if this signal is in an open state or at low level.

Address Signals A16 (B16), A17 (B18)

The unbuffered address signals A16 and A17 are derived from port 4 of the controller. Specifications in the controller manual are applicable.

RAM Address Inputs RA16 (B15), RA17 (B17)

The RAM address inputs RA16 and RA17 are provided to allow bank switching of RAM in two 128 kByte or four 64 kByte blocks. In the standard configuration of the module, these inputs are pre-connected via solder jumpers to A16 and A17 on the component side of the module.

Battery Voltage Input VBAT (B20)

VBAT can be connected to a battery. Common vales for a battery supply is 3 V. The battery voltage is available to the VPD (B22) output when the module is not powered.
This connector doesn't have a load function for connected batteries. If no battery is connected, this input has to be connected to GND.

RESET Connector /RES (B21)

This connector is bi-directional. After turning on the supply voltage VCC, the RESET signal is held to GND potential for 50 ms. If the supply voltage is too low, the signal is held at GND potential all the time. An external push button can be connected to this "open drain" signal for a manual RESET.

Battery Voltage Output VPD (B22)

If a battery is connected to VBAT (B20), the output VPD generates the 3 V battery voltage if the supply voltage VCC is not available. Otherwise this output provides VCC level. However only currents up to 50 mA are permitted. Additional information is available in *section 8* or in the manufacturer's manual for the device populating U17.

Controller Signals /NMI (B23), /RD (B19), ALE (B13)

These control signals are provided directly from the controller. The data in the controller manual applies.

Memory Selection Signals MSEL_A and MSEL_B (B25, B26)

These signals are generated by the module's address decoder. They control selection of RAM, ROM and FLASH EPROM.
With special versions of the address decoder U15 an external decoder can be attached.

RS-485 Transceiver A (B32), B (B30), R (B31), D (B29),/ RE, (B27), DE (B28)

The bi-directional data lines A and B can be attached to an existing RS-485 network. The control inputs /RE and DE are short circuited by a solder bridge and connected to GND by a resistor. This renders the transceiver into reception mode. The receiver output R as well as the transmission data input D generate TTL-levels.

RESET Output /RSTOUT (B33)

The clock-synchronous RESET signal of the controller is available on this output. The data in the controller manual is applicable.

Clock Output XTAL1 (B37)

The clock signal of the quarz oscillator is available on this output. The standard clock frequency is 40.00 MHz.

FLASH Input /FPWD (B34)

This module connection should be connected to VCC. Only when using special INTEL FLASH-EPROM (28F001BX-B) devices it is possible to switch the FLASH-EPROM into Power-Down mode with this control input.

Decoder Control Inputs MODE(B38) and / BOOT (B35)

The classification of these two control inputs for the decoder-PLD U15 is more or less insignificant. They contribute to the selection of memory models, as far as there are various memory models programmed in the PLD. These inputs can also be used for other purposes when using special PLDs. They can also be programmed as additional /CE outputs. Refer to the PLD functional description in the *Supplemental Memory Model Sheet* for specific information.

AUX Port X[0..15] (B39..B53)

The function of this port depends on the setting of the bus mode selected by Jumper J1 and J2.

In non-multiplexed bus mode this is an additional output port, for which the specification of the components U2/U3 (74HCT573) is applicable. The address of this port can be found in the *Supplemental Memory Model Sheet* (signal name LACLK).

In multiplexed bus mode the AUX port X0..15 is connected to the controller port P1. In this case the specifications in the controller manual apply.

4.2 The Pin Header Row C – Analog Signals

The pin header connector C covers the analog ports P5.0 through P5.9, as well as the analog reference voltages VAGND and VAREF, as shown in *Figure 3*. If the analog port remains unused, it is recommended to connect all input pins, including the reference voltage inputs, to defined potential. The values in the controller manual apply.

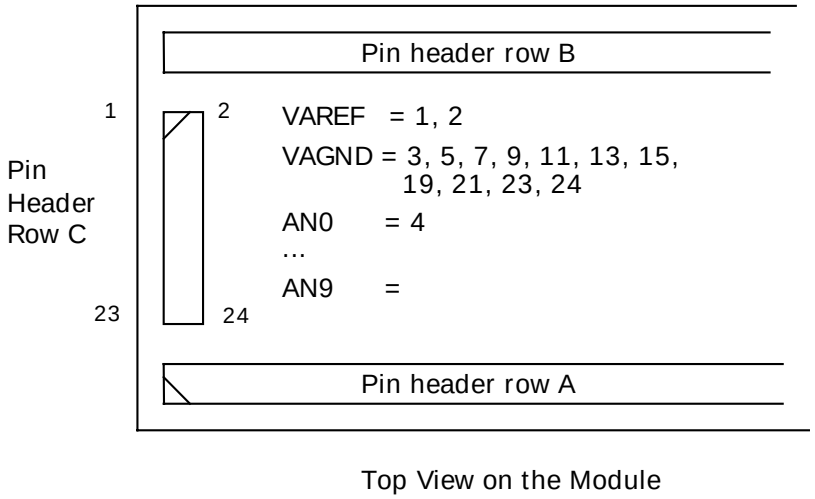


Figure 4: Pin Assignment of the Analog Connector C

5 Memory Model and Address Decoding

The memory model depends on the devices mounted on positions U6/U7 and U8/U9 with EPROM or FLASH-EPROM and the program included in the decoder-PLD U15.

The miniMODUL-166 can be populated with memory devices providing more capacity than the 256 kBytes address space of the controller. Combined with the software controlled PLD decoder and the banking option of the RAM U4/U5, this expanded board memory enables a series of combinations of EPROM and/or FLASH-EPROM including RAM.

The following description is only a general overview based on choosen memory model examples that support a series of applications. Refer to the *Supplemental Memory Model Sheet* for the applicable memory model of your module. As an option, the miniMODUL-166 can be delivered with special PLD configuration.

5.1 The Decoder-PLD U15

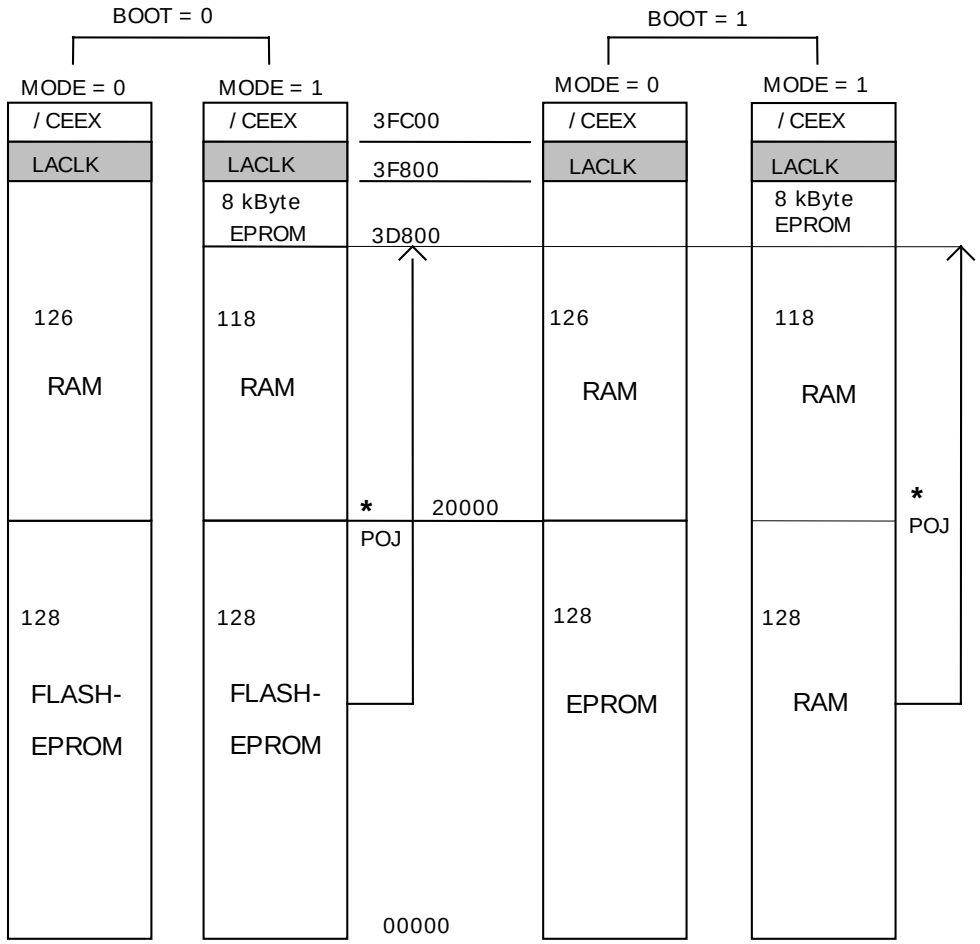
The memory model of the miniMODUL-166 is determined by U15.

U15 generates the control signals MSEL_A and MSEL_B for memory, for the data bus transceiver U10/U11 and for the U2/U3 latches in non-multiplexed mode. The PLD is available in various versions. Refer to the *Supplemental Memory Model Sheet* for information on the populated PLD. Customer specific PLDs can be provided upon request. Be aware of increased lead time, since the PLD has to be programmed before the module is assembled.

The control inputs MODE (B38) and /BOOT (B35) are used for selection of possible memory models, as long as multiple possibilities are realized in the PLD. These inputs can be used for various purposes with special PLD versions. For example, it is possible to use them as additional Chip-Select outputs.

5.2 The Standard Memory Models

The following figure shows the standard memory models on the miniMODUL-166. FLASH-EPROM on U8/U9 is only addressable if available on the miniMODUL-166.



* EPROM also mapped to 00000H during Power-On-Jump.
RAM not selected at this time

/ CEEX
Area for externally decoded / CE signals 3FC00H...3FFFFH

LACLK
Optional for writing to the LATCH. This area is shared with the memory area. 3F800H..3FBFFH

Figure 5: The Standard Memory Models on the miniMODUL-166 (P300)

We reserve the right to make changes to the standard model, or to offer alternate PLDs based on new technological standards or upon customer request. Therefore, when ordering, it is important to always give the PLD number to avoid incompatibility errors.

The following description is valid for boards populated with a PLD P300, as standard on all miniMDOUL-166 with PCB number 1050.4 and higher.

Caution:
The redesigned miniMODUL-166 (PCB-No. 1136.x) is populated with a different address decoder (P508). The memory model for this version of the module is described in *AII Revision History"*.

The PLD P300 provides four different memory models. The selection of a current memory model is done by configuration of the control inputs /BOOT und MODE with a GND level during power on. These two control signals are available on the pin header connector (/BOOT = B35, MODE = B38). Both inputs have an internal pull-up resistor, providing a logical high potential when unconnected.

Two modes support operation with LCC32-EPROM and RAM (/BOOT=1). The two other modes allow operation with FLASH-EPROM (/BOOT=0). In each of both modes the Power-On Jump to code memory at address 20000H is possible. More details on the Power-On Jump feature can be found in the following section of this manual.

In one of the modes EPROM/FLASH-EPROM and RAM are selected. This mode (/BOOT=0, MODE=1) can be used for initial programming of the FLASH-EPROM.

Please note, that a maximum of 128 kByte of RAM is directly addressable with this type address decoder. The user can enable use of the second half of the RAM by bank switching (using RA17) with software. Other memory models are available on request.

5.3 The Power-On Jump Mode

Under certain circumstances the PLD U15 has a Power-On-Jump mode.

The Power-On Jump mode enables a program start at an address different from 00000H, for example on 10000H or 20000H after a reset. It simplifies the test of a user program under the control of a monitor program, since the user's Assembler- and C-programs can be allocated in the address area from 00000H on. This thereby eliminates problems with interrupt vector applicability as well as possible errors incurred when resetting the user program to 00000H, which is otherwise required.

The Power-On-Jump mode requires a Flip-Flop, which is realized in the PLD. This sets the decoding process in a wait state after a reset. In this wait state EPROM or FLASH-EPROM are selected simultaneously at address 10000H or 20000H. Its contents are "mirrored" in blocks throughout the entire memory space. The program in EPROM has to be linked for the address space starting at 10000H or 20000H, and has to contain jump instructions to the main program's starting address. The Flip-Flop is set as soon as the jump is performed and the address decoding procedure is brought to its end state. In this end state, the EPROM is only selected starting at 10000H or 20000H, the memory space is allocated to RAM starting at 00000H.

Note:
A user program in EPROM, which should be executable in the Power On Jump mode, must provide the following characteristics:

- With the Linker in address spaces starting at 10000H or 20000H or higher, in every case allocated page for page according to EPROM size.
- Absolute jump instruction to the starting point of the program at the beginning of the program.
- but programmed in EPROM to the physical address 00000H

The selection of the program start address effected in the power on Jump mode via the programming of the PLD U15. usually is used for A17 whereby addresses are applicable starting from 20000H.

5.4 Device Options for the EPROM sockets U6/U7

The EPROM sockets U6/U7 are suitable for population with EPROM devices in LC32-packaging on standard versions of the board. Devices in PLC32-packaging are **NOT** supported. Make sure to not mismatch the EVEN-EPROM and the ODD-EPROM when mounting the EPROM devices. The socket for the EVEN-EPROM is located directly next to controller at U1 (SAB80C166).

When populating the EPROM make sure that the devices are fully inserted into the socket. This is usaully indicated by an well audibly sound. Afterward secure the EPROM with the metal clamps to prevent from unintended removal.

5.5 Device Options for the FLASH-Pads U8/U9

Depending on the miniMODUL-166 order option FLASH EPROM might be mounted on the board. FLASH-EPROMs can also be populated on the board with an appropriate tool at a later point.

The positions U8 and U9 can house memory devices in PLC32-packaging with megabit pinout. They are designed for permanent soldering of FLASH-EPROM. FLASH-EPROMs can be programmed on-board, assuming the required programming voltage has been connected to VPP (A60). Be sure to connect the appropriate programming voltage. FLASH-EPROMs are available as 5 Volt types and 12 Volt types. Refer to the corresponding FLASH-EPROM data sheet for the appropriate voltage. You also may contact PHYTEC with questions about the availalable FLASH-EPROM types.

If FLASH EPROM are mounted, the module connection / FPWD (B34) should be externally connected with VCC.

5.6 Bank Switching for RAM on U4/U5

The RAM devices on U4 and U5 are connected with the address bus A[1..17] on a miniMODUL-166 in the standard configuration. If other memory types are mounted on U6/U7 or U8/U9, parts of the RAM can not be used.

For applications requiring the use of the entire RAM capacity, RAM can be divided into two 128 kByte banks or four 64 kByte banks. The two upper address lines of the RAM U4/U5 RA16 and RA17 are available on the connector field (B15..B17). RA16 and RA17 are pre-connected to A16 and A17 by default with a solder bridge on the top side of the module. In order to realize the bank switching, these connections have to be opened carefully and RA16 or RA17 have to be externally connected to a free port pin of choice.

6 Jumper Settings

For configuration purposes, the miniMODUL-166 has various solder jumpers, some of which have been installed prior to delivery. Removal or reconfiguration of the solder jumpers should be done with special precaution given the compact nature of the module. Use only appropriate SMD tools for any solder work on the board. Please ensure that the board as well as surrounding components and sockets, remain undamaged while desoldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable.

Changing the default jumper settings allows the user to modify specific functions of the module such as:

- the bus mode of the controller,
- the function of the serial interface lines TXD0 and RXD0,
- the configuration of EPROM capacity and
- the programming mode for FLASH EPROM.

The miniMODUL-166 comes with pre-configured jumper settings, which result from test procedures or are established by installed software:

- bus mode 16-bits, non multiplexed,
- latch U2/U3 usable as output port X[0...15],
- serial interface RI1, TO1 (TXD0/RXD0) active,
- serial interface 1 not connected, and
- EPROM capacity undefined (refer to Jumper J9).

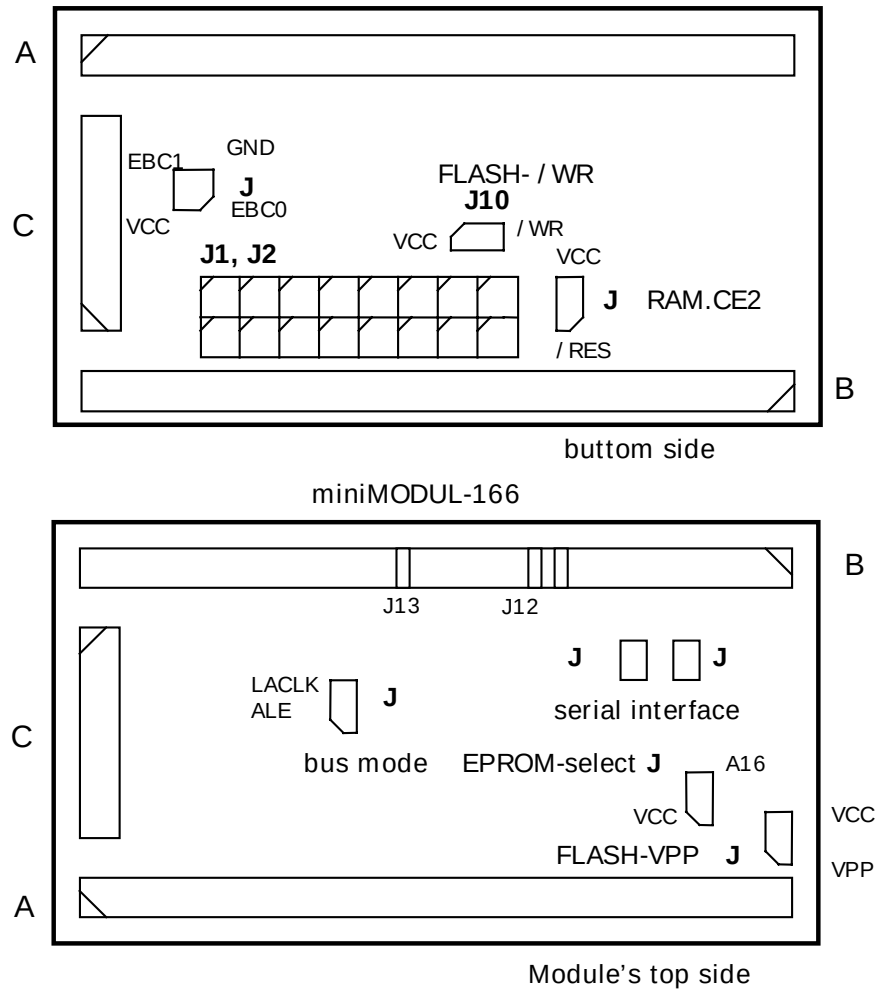


Figure 6: Location of the Jumpers on the miniMODUL-166

Changing the default jumper settings allows the user to modify specific functions of the module such as:

- the bus mode of the controller,
- the function of the serial interface lines TXD0 and RXD0,
- the configuration of EPROM capacity and
- the programming mode for FLASH EPROM.

The miniMODUL-166 comes with pre-configured jumper settings, which result from test procedures or are established by installed software:

- bus mode 16-bits, non multiplexed,
- latch U2/U3 usable as output port X[0...15],
- serial interface RI1, TO1 (TXD0/RXD0) active,
- serial interface 1 not connected, and
- EPROM capacity undefined (*refer to Jumper J9*).

Detailled description on the individual jumpers is provided in the following section.

6.1 Selection Multiplexed/Non-Multiplexed Mode: J1 and J2

The controller is set to multiplexed or non-multiplexed mode with J1/J2. The address latch U2/U3, which becomes free in non-multiplexed mode, can be used as an output port on connector pins X[0..15]. P1 delivers the address signal then. In the other case the latch delivers the address signals, P1 is then connected with X[0..15].

Non-multiplexed mode is enabled by bridging the jumper fields J1, J2 parallel to the connection port B. In this mode:

- P1 is address port and
- U2/U3 is output port at X[0..15].

Multiplexed mode is enabled by bridging the Jumper fields J1, J2 vertical to the connection port B. In this mode:

- P1 is connected to X[0..15] and
- U2/U3 is address port.

6.2 Clock for Address Latch U2/U3: J3

In non-multiplexed mode the address latch is not needed by the controller. It is available as an output port at X[0..15]. In this case clock input of the address latch must be adjusted to the signal LACLK. J3 in position 2 - 3.

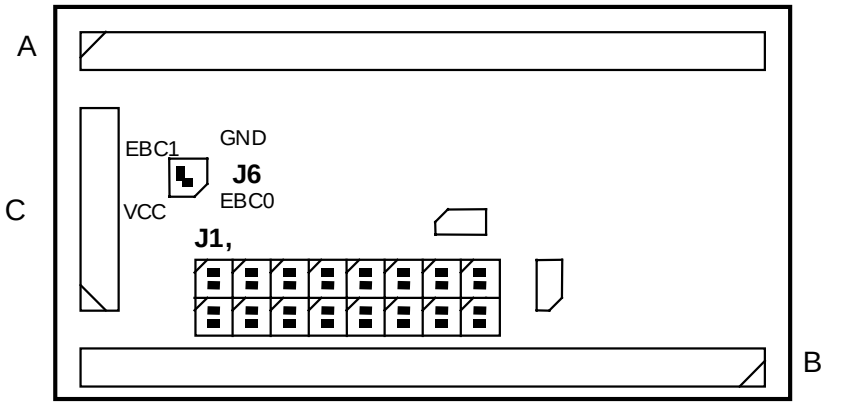
In multiplexed mode the address latch U2/U3 generates the address signals. P1 is connected to X[0..15] in this case. The address latch needs the controller signal ALE as a clock. J3 in position 1 - 2.

6.3 Connection of the Serial Interface with RS-232 Transceiver: J4 and J5

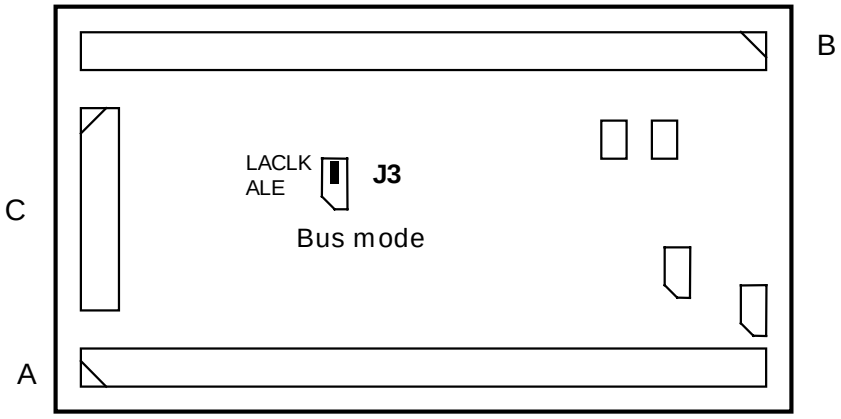
If the serial interface 0 (TXD0, RXD0) of the controller is required as an RS-232 interface, both of these jumpers must be closed. The jumpers are already closed for testing purposes.

6.4 Bus Mode Configuration: J6

The SAB80C166 sets the address bus mode during the initialization phase. The setting of J6 selects one of the four possible modes. Jumpers J1, J2 and J3 have to be configured corresponding to this setting. The following figure illustrates the settings for 16-bit, non-multiplexed and for 16-bit multiplexed modes.

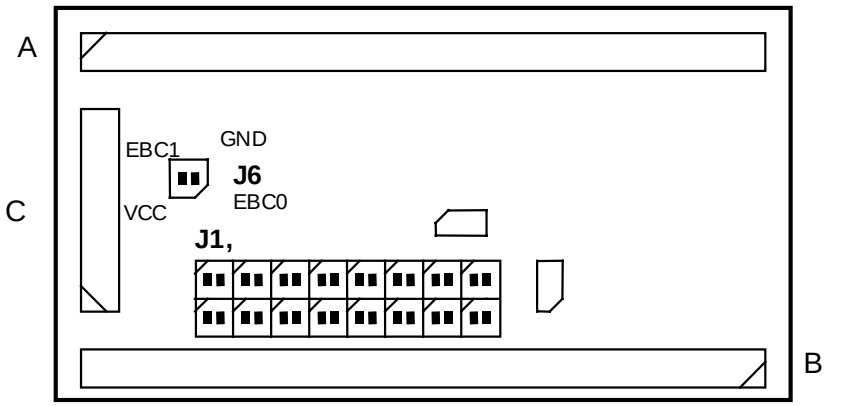


non-multiplexed mode

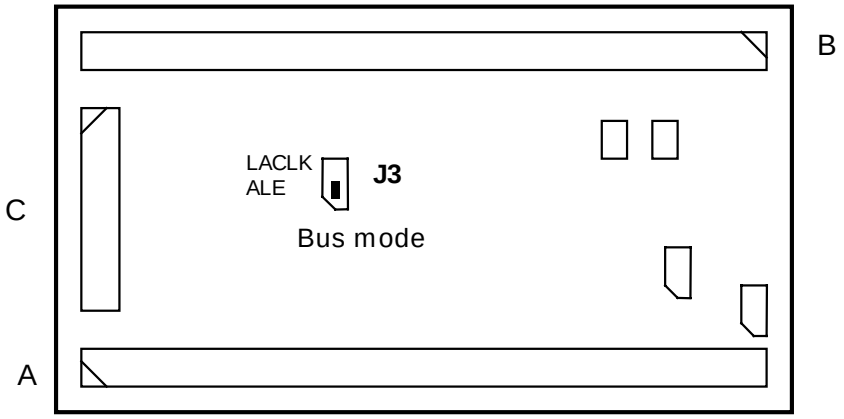


non-multiplexed mode

Figure 7: Setting of the Bus Mode Jumpers J1, J2, J3 and J6 (non-multiplexed mode)



multiplexed mode



multiplexed mode

Figure 8: Setting of the Bus Mode Jumpers J1, J2, J3 and J6 (multiplexed mode)

6.5 Supply Voltage for FLASH Programming: J7

If FLASH-EPROM needs to be programmed with a programming voltage of 12 V, Jumper J7 must be set at position 1 - 2. Otherwise the jumper should be set at position 2 - 3. This also enables programming of 5 Volt types.

6.6 Selection CE2 for RAM on U4/U5: J8

On RAM devices with a CE2 input at pin 30, this input can be connected to the /RES. This is advisable if the RAM device needs to be buffered with a battery. Set Jumper J8 to position 1 - 2 to enable this function.

For RAM devices without a CE2 input, pin 30 should be connected to VPD. In this case, set Jumper J8 to position 2 - 3.

For reasons of operating safety, please be advised that despite the battery buffer, changes in the data content within the RAM can occur given disturbances. The battery buffer does not completely remove the danger of data destruction.

6.7 Selection of EPROM Size: J9

The address input A15 can be connected to either A16 or VCC with configuration of Jumper J9. When using EPROM devices with a capacity of 32 kByte, the jumper should be set to position 1 - 2. For 64 kByte EPROM it should be set to position 2 - 3.

6.8 Configuration of / WR for U8/U9: J10

If FLASH-EPROM is populated at U8/U9 and on-board programming is required, the write signal /WR must be connected ot the devices. In this case, set Jumper J8 to position 2 - 3. If write access is not intended or OT-PROMs are used, J8 should be set to position 1 - 2.

7 The Serial Interfaces

The controller is populated with two serial interfaces: SERIAL 0 with signals TXD0 and RXD0, as well as SERIAL 1 with signals TXD1 and RXD1.

7.1 SERIAL0

The miniMODUL-166 has an RS-232 interface on connector row B (B3 = TXD0, B4 = RXD0). Jumpers J4 and J5, located on the component side, must be closed for operation of this interface. If the RXD0 signal on P3.11 needs to be used for other purposes, J5 has to be opened.

The RS-232 interface is intended for use in applications requiring short cable extensions with low electromagnetic interference. The transceiver devices used on the miniMODUL-166 allow protection against electrostatic overvoltage up to 2 to 3 kV. For use in outdoor environments that are not typically suitable for RS-232 applications, we recommend special precautionary measures to prevent damage from lightning or potential variances.

7.2 SERIAL1

The second serial interface SERIAL 1 of the miniMODUL-166 can be used as an RS-232 interface or optional as an RS-485 interface. Selection between RS-232 and RS-485 is determined via external module circuitry. The desired transceiver device need to be connected to signals TXD1 (A20) and RXD1 (A19).

In contrast to the RS-232 interface, the RS-485 interface is only in either “Send” or “Receive” mode at a given time. This means that both control inputs /RE485 (B31) and DE485 (B29) can be connected together to a free port pin in the most simple case. With this port pin, direction of the RS-485 interface can be switched under software control.

The RS-485 transfer in a closed system with defined potential is not critical even without galvanic separation. RS-485 data transfer is possible over hundreds of meters even with higher baud rates (with a cable with appropriate resistance). The following should be noted:

It is the user's responsibility to determine the necessity of a galvanically separated RS-485 interface. This decision has to be based on specific application requirements.

An important criteria is the degree of electromagnetic interference in the cabling environment as well as the condition that the maximum difference in potential among nodes in the RS-485 network must not exceed + 7 Volt over VCC and – 7 V under GND. These potential differences can be avoided by a GND connection. However, problems caused by ground loops may occur in this later case.

8 The Watchdog IC on U17

The Watchdog device MAX690 is described briefly in the following section. For complete description of the component's features, refer to the manufacturer's data sheet.

The Watchdog device U17 (MAX690) generates the RESET signal / RES during the power on sequence. After the supply voltage rises to over 4,6 V, /RES remains active for approximately 50 ms. If the supply voltage VCC drops below 4.6 V, /RES connects statically to GND.

For generation of a manual RESET the open drain output /RES (B21) is connected externally with a push button to GND. It is recommended to mount a 10..100nF capacitor on C11 to reduce contact bouncing of the button. Higher value capacitors should not be connected to /RES.

The battery voltage input VBAT (B20) does not effect the basic operation of the module. It should however be connected externally to GND when not used. The battery voltage input is intended for use with 3 Volt batteries.

The voltage output VPD (B22) supplies the RAM U4/U5 and can also be used for external circuitry expansions. VPD is switched to battery power as soon as VCC drops below 4.6 V. Otherwise it carries the VCC supply voltage. Only minimal currents up to approximately 50 mA can be drawn. Battery buffering of the RAM U4/U5 is theoretically possible, however not a guaranteed characteristic of the module. All necessary precautionary measures remain therefore the responsibility of the user.

The Watchdog input WDI (A62) generates the /RES signal, as long as it is not open and has not experienced a change in its state within 1.6 seconds. This input can also be used to generate an external RESET free of any bouncing characteristics.

However, this requires the push button connected to the WDI input to be active for more than 1.6 seconds to render /RES active.

The Power-Fail input PFI (A61) can be used for recognition of a power failure. The connected voltage is compared to an internal reference of 1.3 V. If the connected voltage drops below the reference voltage PFO (A59) changes to low level.

9 Programming the FLASH-EPROM

The miniMODUL-166 can be populated with FLASH-EPROM devices in PLCC32-packaging at positions U8/U9. FLASH-EPROM is on-board programmable.

Caution:
Only 5 Volt FLASH-EPROM devices can be used!

9.1 FLASH EPROM Types and Hardware Precautions

If necessary the programming voltage can be connected to the module header pin VPP. In normal operation mode, this header pin has to be connected to VCC. Programming capability of FLASH-EPROM devices is configured with Jumpers J7 and J10.

Jumper J10 configures selection between VCC and /WR on the write input of the FLASH-EPROM. Jumper J10 should be set at position 2 - 3 to enable programming the FLASH-EPROM.

Jumper J7 can be used as programming barrier for 12 Volt types. With this Jumper the VPP input of the FLASH-EPROM can be solely connected to VCC. This jumper should be set at position 1 - 2 for programming a 12 Volt FLASH-EPROM.

To generate a 12 Volt programming voltage at A60, f.e. an LT1109 device can be externally connected to the miniMODUL-166. This IC generates a programming voltage of sufficient accurancy directly from the VCC supply voltage. It can be powered on via software. When switched off it carries VCC to the output.

9.2 Software Driver for FLASH EPROM

For the FLASH-EPROM already tested in-house, a diskette with software drivers including examples for erase and programming routines for various FLASH-EPROM types is available. These software examples are translated using A166 and C166 from KEIL. More specific information on use of these drivers can be found in the documentation file on the utility diskette. PHYTEC reserves the right to revise and expand this diskette without further notice.

10 Booting Application Software

With the possibility of on-board programming of FLASH-EPROM devices on the miniMODUL-166 without manual access, certain applications are enabled, for which a “remote controlled” software download over one of the serial interfaces can be utilized. The FLASH-EPROM offers a high degree of data security over a long period of time. These devices can be used to store easily reprogrammable user programs without the risk of data loss.

The miniMODUL-166 could also be used in applications with distributed networked controllers that receive process data or programs over a dual cable RS-485 connection from a master. Applications where a remote software update is carried out via a modem is also possible.

The exact sequence of such a BOOT process varies from application to application. It depends on the FLASH-EPROM and memory model type. In any case there is a minimum program that guarantees a minimal function of the miniMODUL-166 after a RESET. This is the minimal function of a BOOT program, with which it is possible to read the new user program via one of the serial interfaces and store it in FLASH-EPROM.

For this purpose, the miniMODUL-166 offers different possibilities:

- Use of FLASH EPROM with separate BOOT sector e.g. 28F001BX-B of INTEL (optional).
- Use of FLASH EPROM with several, separately erasable address spaces.
- Use of separate BOOT EPROM on U6/U7 and at the same time of a (not necessarily large) FLASH EPROM on U8/U9.

The free mode inputs of the address decoder give the additional possibility to differentiate between a normal mode and a Boot mode under software control using a port pin.

PHYTEC offers a utility diskette for the miniMODUL-166, which contains a variety of example programs, such as booting software. This diskette is not included with the miniMODUL-166.

10.1 Booting with the Help of EPROM or FLASH EPROM

The usually consistent BOOT program is located in the address space starting at 00000H in the Boot sector of a separately erasable, larger FLASH-EPROM or in a small EPROM.

The application program is programmed into FLASH-EPROM in another address space and subsequently executed. The BOOT program can be reprogrammed as well if desired. However, with some FLASH memory types (INTEL) that have a special BOOT sector, this is only possible with a manual setting on the board.

In any case the miniMODUL-166 design guarantees, that a new general programming of the device after a total data loss, for example after a communication interruption or power failure, is possible without any soldering work.

10.2 Booting with the BOOT function of the SAB80C166

Starting with the mask version CB of the SAB80C166, the controller has its own BOOT function, with which it is possible to load software via the serial interface SERIAL 0.

Invoking the Bootstrap Loader

The controller is rendered into a special Bootstrap mode, under the following conditions:

- The controller's ALE output is held at VCC level, so that this state is saved during a rising edge of the /RSTIN signal.
- /NMI is generated within 5ms after /RSTIN rises.
- ALE is released.

If this sequence is not initiated, the controller generates an internal RESET and begins to work normally.

Loading the BOOT program

After the Bootstrap procedure is carried out, the controller enters a loop to initialize the serial interface.

In addition a zero byte (00H) must be sent to RXD0. The used transmission mode is 8 bits, one stop bit, maximum baud rate is 9600 baud.

After successful initialization of the serial interface the SAB80C166 sends the byte 55H over TXD0 to indicate confirmation.

Subsequently, the SAB80C166 expects exactly 32 bytes, which are stored in the controller‘s internal RAM starting at address 0FA40H and which are interpreted as machine code. After receipt of the 32nd byte the controller begins program execution at address 0FA40H.

For programs of less than 32 bytes in size, dummy bytes need to be attached.

With a software RESET (SRST) the boot procedure is terminated.

11 Circuitry Expansions

For the connection of additional periphery the buffered, bi-directional data bus BD[0..15] and the buffered address bus BA[0..15] can be used. Both busses extend to the pin header rows A and B. The address lines A16 and A17 as well as the control signals /WR and /RD are exceptions , as they are not buffered.

The release of the bidirectional data bus buffer is caused by the control signal /CEEXT. The address space, in which external access via the U10/U11 data buffers is possible, depends on the program stored in the address decoder PLD. More information is available in the *Supplemental Memory Model Sheet*.

Since the decoder is soldered on the PCB, precise specifications on the internal program have to be given before board production.

12 The AUX Port

The AUX port X[0..15] has two different functions, determined by the controller's bus mode.

In non-multiplexed mode the controller port P1 provides the address signals. The address latches U2 and U3 are free and can therefore be used as an additional output port. The AUX port X[0..15] covers a 1 kByte memory space in the standard version address decoder. Additional information can be found in the *Supplemental Memory Model Sheet* under the signal description LACLK.

In multiplexed mode the controller provides the address signals over the data bus P0 and stores them in the address latch U2/U3. The controller port P1 is free and extends to the AUX port X[0..15].

13 Programming Hints for Unexperienced Users

In order to prevent you from stumbling into pitfalls (such as the EINIT instruction and the controller-internal Watchdog) during your first attempts with the SAB80C166, follow the instructions below:

- When programming in Assembler, give the controller the EINIT instruction at the beginning of the program, otherwise errors will occur.
- Also issue the DISWDT instruction to the controller before the EINIT instruction, otherwise the Watchdog timer will interrupt the program after 6 ms.
- Don't be alarmed if the data- and address bus come to a sudden stop. There is most likely a program loop that is running within the instruction queue of the controller. Typical case: waiting for input from the serial interface.
- To test whether the program is functioning correctly at all, look at the /RD-Signal with the oscilloscope. If there is a noticeable pause (high level) every 6 ms, the controller's Watchdog timer hits. The program is most likely not running at all. Questions you should ask yourself: Is the program compatible with the selected memory model? Has the EVEN-EPROM been mismatched with the ODD-EPROM?
  EVEN = Lowbyte, ODD = Highbyte!
- If the serial interface 0 (TXD0, RXD0) is not functioning, make sure that both Jumpers J4 and J5 are closed. Questions you should ask yourself: Did I accidentally reverse RXD and TXD? The miniMODUL-166's RXD has to be connected to TXD on the PC and vice versa.
- Before using a port pin, remember that it has to be programmed explicitely as an input or output pin. This even applies to the /WR signal on port P3.13.

Appendice A

AI Mechanical Dimensions

The mechanical dimensions of the miniMODUL-166 are represented in *Figure 9*.

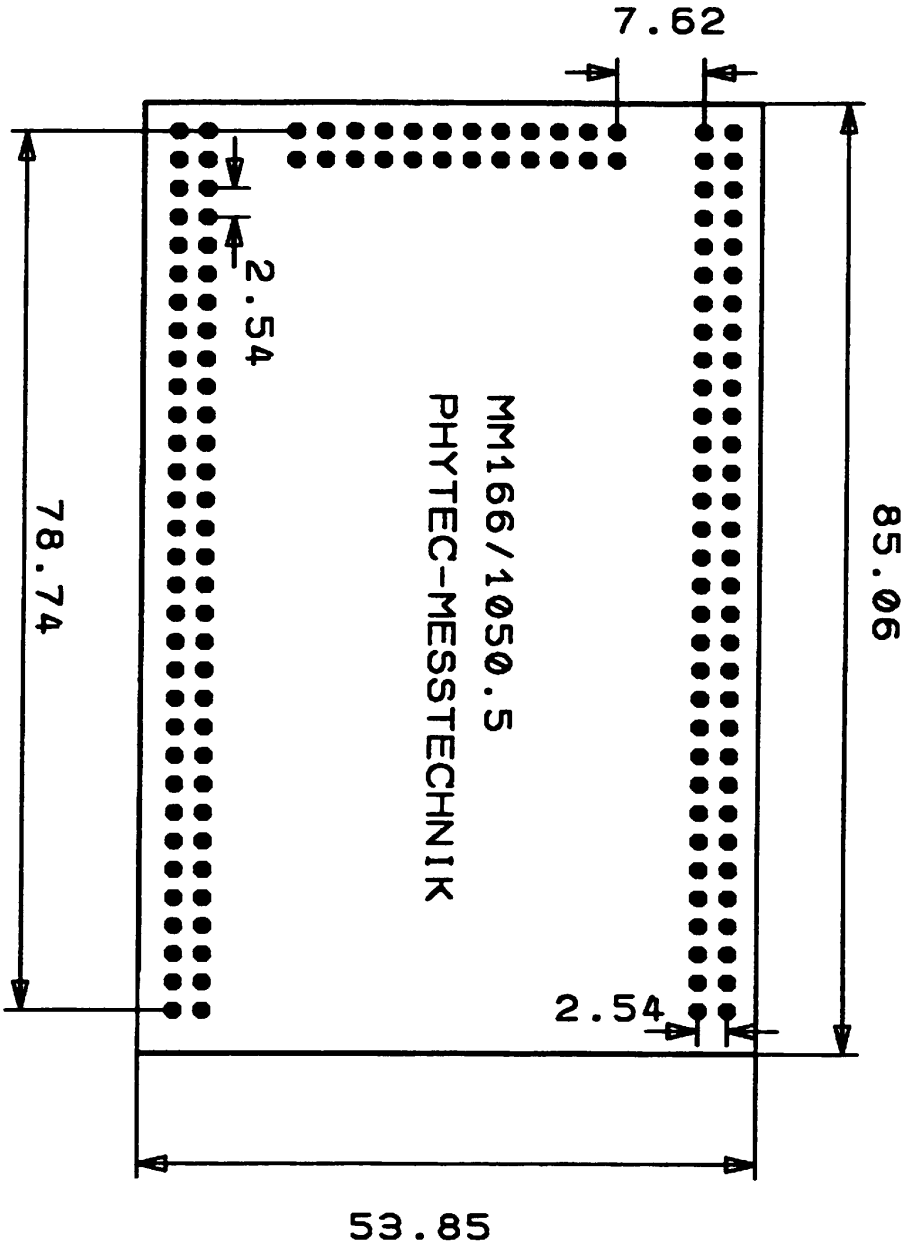


Figure 9: Mechanical Dimensions and Location of the Pin Header Rows

AII Revision History

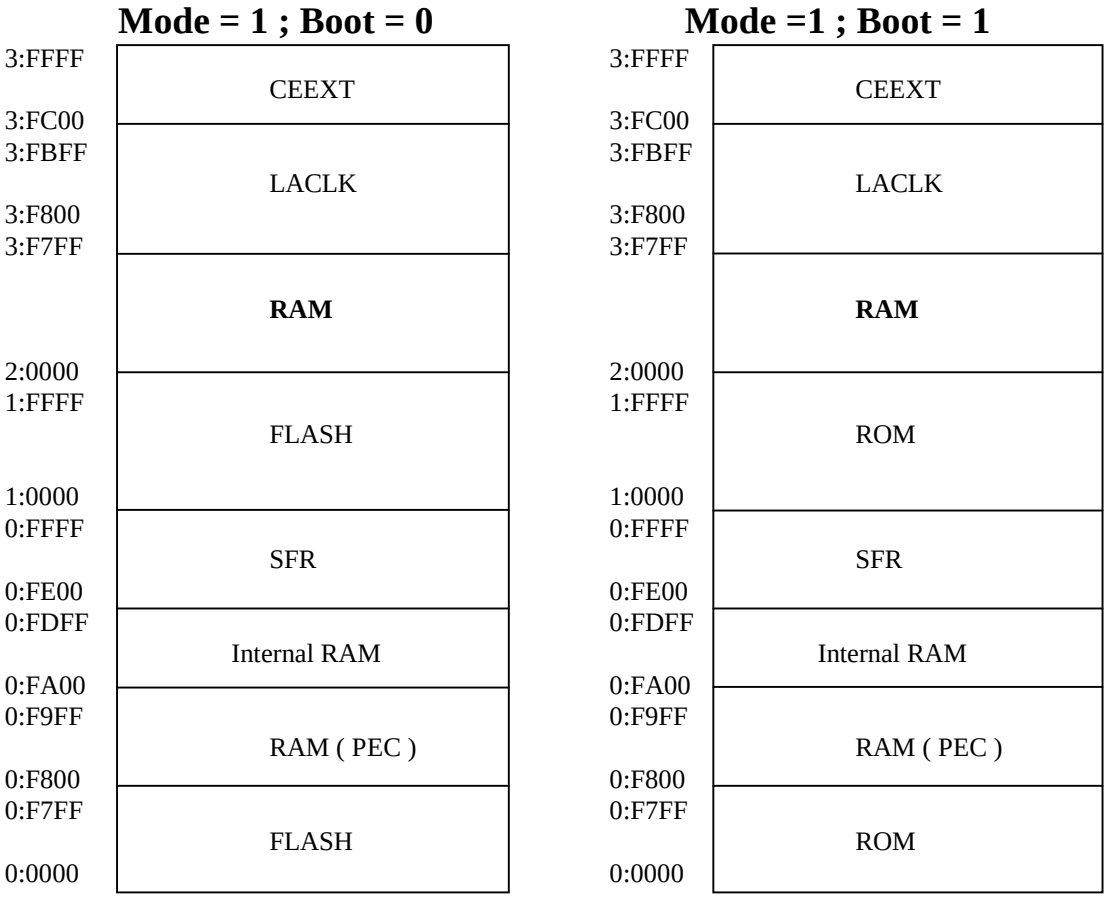
Certain changes in jumper functions have resulted from revisions to the miniMODUL-166. In addition, a different PLD and corresponding memory model are used. The type of board you are using can be determined by the PCB number (old: 1050.x, new: 1136.x). This number is located on the module as well as on the circuit diagram.

The following table shows the changes in jumper descriptions:

Jumper	Old Description (PCB #. 1050.7)	New Description (PCB #. 1136.1)
J1A-J1H	1-2,3-4 non-Mux/Mux	1-2, 3-4 non-Mux/Mux
J2A-J2H	1-2,3-4 non-Mux/Mux	1-2, 3-4 non-Mux/Mux
J3	1-2 multiplexed 2-3 non-multiplexed	1-2 multiplexed 2-3 non-multiplexed
J4	closed. P3.10 extends to RS-232 open. P3.10 extends to pin headers	closed. P3.10 extends to RS-232 open. P3.10 extends to pin headers
J5	closed. P3.11 extends to RS-232 open. P3.11 extends to pin headers	closed. P3.11 extends to RS-232 open. P3.11 extends to pin headers
J6	1-2 EBC0 = VCC 1-3 EBC0 = GND 2-4 EBC1 = VCC 3-4 EBC1 = GND	1-2 EBC0 = GND 2-3 EBC0 = VCC EBC1 extends accross R13 on VCC
J7	2-3 VPP on FLASH = VCC 1-2 VPP on FLASH = VPP	No longer necessary because only 5 V Flash are used
J8	1-2 VPD = /RES 2-3 VPD = VPD	1-2 VPD = /RES 2-3 VPD = VPD
J9	1-3 OTP with 32 kB 2-3 OTP with 64 kB	1-2 OTP with 32 kB 2-3 OTP with 64 kB
J10	1-2 Flash write protected 2-3 Flash not write protected.	1-2 Flash write protected 2-3 Flash not write protected.
J11	closed. A16 connected to RA16 open A16 not connected to RA16	closed. A16 connected to RA16 open A16 not connected to RA16
J12	closed A17 connected to RA17 open A17 not connected to RA17	closed A17 connected to RA17 open A17 not connected to RA17
J13	closed /RE connected to DE. open /RE connected to transceiver /DE connected to transceiver.	closed. /RE connected to DE open /RE connected to transceiver. /DE connected to transceiver
J14	----	closed. EBC1 connected to VPP open EBC1 not connected to VPP
J15	---- (always connected to GND)	1-2 BUSACT connected to VCC 2-3 BUSACT connected to GND
J16 RTC	----	RTC /INT connected to P20
J17 RTC	----	RTC SCL connected to P21
J18 RTC	----	RTC SDA connected to P22
J19	----	VAREF connected to VCC
J20	----	VAGND connected to GND

Table 1: Changes in the Jumpers after Revision of the miniMODUL-166

Memory Models of the Address Decoder P508



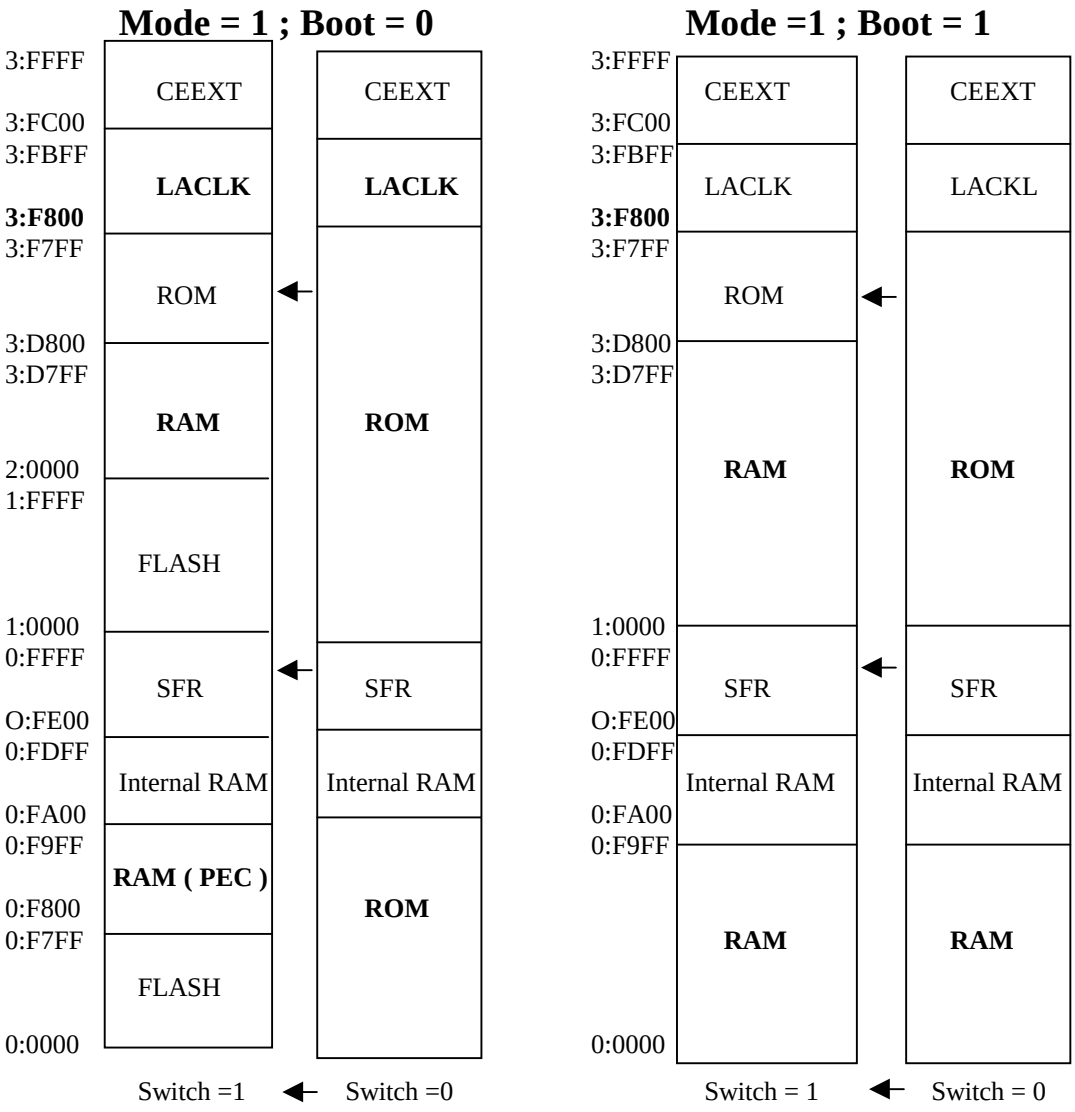


Figure 10: Memory Models of the Address Decoder P508

Switch is a decoder-internal signal which becomes active when accessing memory located above the address 3:D800H.

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