phyCORE-MPC5554

(with MPC5567 extension)

Hardware Manual

Edition December 2008

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Preface

This phyCORE-MPC5554 Hardware Manual describes the board's design and functions. Precise specifications for the Freescale MPC55xx microcontroller series can be found in the MPC55xx microcontroller Data Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal. The MSB and LSB of the data and address busses shown in the circuit diagram are based on the conventions of Freescale. Accordingly, D31 and A31 represent the LSB, while D0 and A0 represent the MSB. These conventions are also valid for the parallel I/O signals.

Declaration regarding Electro Magnetic Conformity of the PHYTEC phyCORE-MPC5554

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Note:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header rows or connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-MPC5554 is one of a series of PHYTEC Single Board Computers that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports common 8-, 16- and selected 32-bit controllers on two types of Single Boards Computers:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform
(2) as insert-ready, fully functional phyCORE OEM modules, which can be embedded directly into the user's target design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market.

1 Introduction

The phyCORE-MPC5554 belongs to PHYTEC's phyCORE Single Board Computer module family. The phyCORE SBCs represent the continuous development of PHYTEC Single Board Computer technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a sub-miniature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments the phyCORE board design features an increased pin package. The increased pin package allows dedication of approximately 20 % of all pin header connectors on the phyCORE boards to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD and laser-drilled Microvias components are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCORE-MPC5554 is a subminiature (84 x 57 mm) insert-ready Single Board Computer populated with Freescale's PowerPC MPC5554 microcontroller. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to high-density (0.635 mm) Molex pin header connectors aligning two sides of the board, allowing it to be plugged like a "big chip" into a target application.

Precise specifications for the controller populating the board can be found in the applicable controller User's Manual or Data Sheet. The descriptions in this manual are based on the MPC5554 controller. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCORE-MPC5554.

The phyCORE-MPC5554 offers the following features:

- Single Board Computer in subminiature form factor (84 x 57 mm) according to phyCORE specifications
- all applicable controller and other logic signals extend to two high-density 200-pin Molex connectors
- processor: Freescale embedded PowerPC MPC5554 (up to 132 MHz clock)

Internal Features of the MPC5554:

- 32-bit PowerPC core, up to 132 MHz CPU speed
- 32 kByte Cache memory
- SPE Signal Processing Extention (Single Precison FPU, MAC Unit)
- Memory Management Unit (MMU)
- Direct Memory Access (DMA) controller
- Interrupt latency <70ns @132MHz
- 64 kByte SRAM; 32 kByte capable of battery buffering
- 2 MByte Flash (read while write functionality)
- two UART's (eSCI), LIN support
- four SPI interfaces (DSPI)
- three CAN 2.0B interfaces
- two Time Processing Units (TPU) with 32 channels (pins) each
- 24 channels (pins) timer system (eMIOS) for PWM etc.
- dual 12-bit ADC with 40 (65) channels (ext. MUX)
- multi-purpose I/O signals
- JTAG/OnCE/Nexus test/debug port

Memory Configuration[1]:

- SRAM: 2 MByte to 16 MByte Synchronous Flow-Through Burst-RAM, 32-bit access, 0 wait states, 2-1-1-1 burst mode
- Flash: 2 MByte to 8 MByte asynchronous standard Flash, 32-bit access
- I^2C Memory: 4 kByte EEPROM (up to 32 kByte, alternatively I^2C FRAM, I^2C SRAM)

Other Board-Level Features:

- UART: two RS-232 transceivers for channel A and B (RxD/TxD), also configurable as TTL
- CAN: two 82C250-compatible CAN transceivers for channels A and B; also configurable as TTL
- Ethernet: 10/100 Mbit/s LAN91C111
- FPGA: Lattice XP FPGA XP6/10/15 or XP20 device for
  IP cores: e.g. I^2C Master, 1-Wire-Master, UART, SPI etc.
  programmable bus bridge (simple address-/data bus, PCI bus, DDR-RAM etc.)
  84 external GPIO with programmable characteristics (TTL, CMOS, differential logic, LVDS etc.)
  application specific control logic and clock generation (PLL)
  embedded memory: single-/dual-port SRAM, FIFO etc.
  in-system programmable over JTAG emulation
- I^2C Real-Time Clock with calendar and alarm function
- JTAG/OnCE/Nexus test/debug port
- industrial temperature range (-40…+85°C)

Other CPU configurations:

The phyCORE-MPC5554 is also available equipped with Freescale's embedded PowerPC MPC5567.

1: Please contact PHYTEC for more information about additional product configurations.

1.1 Block Diagram

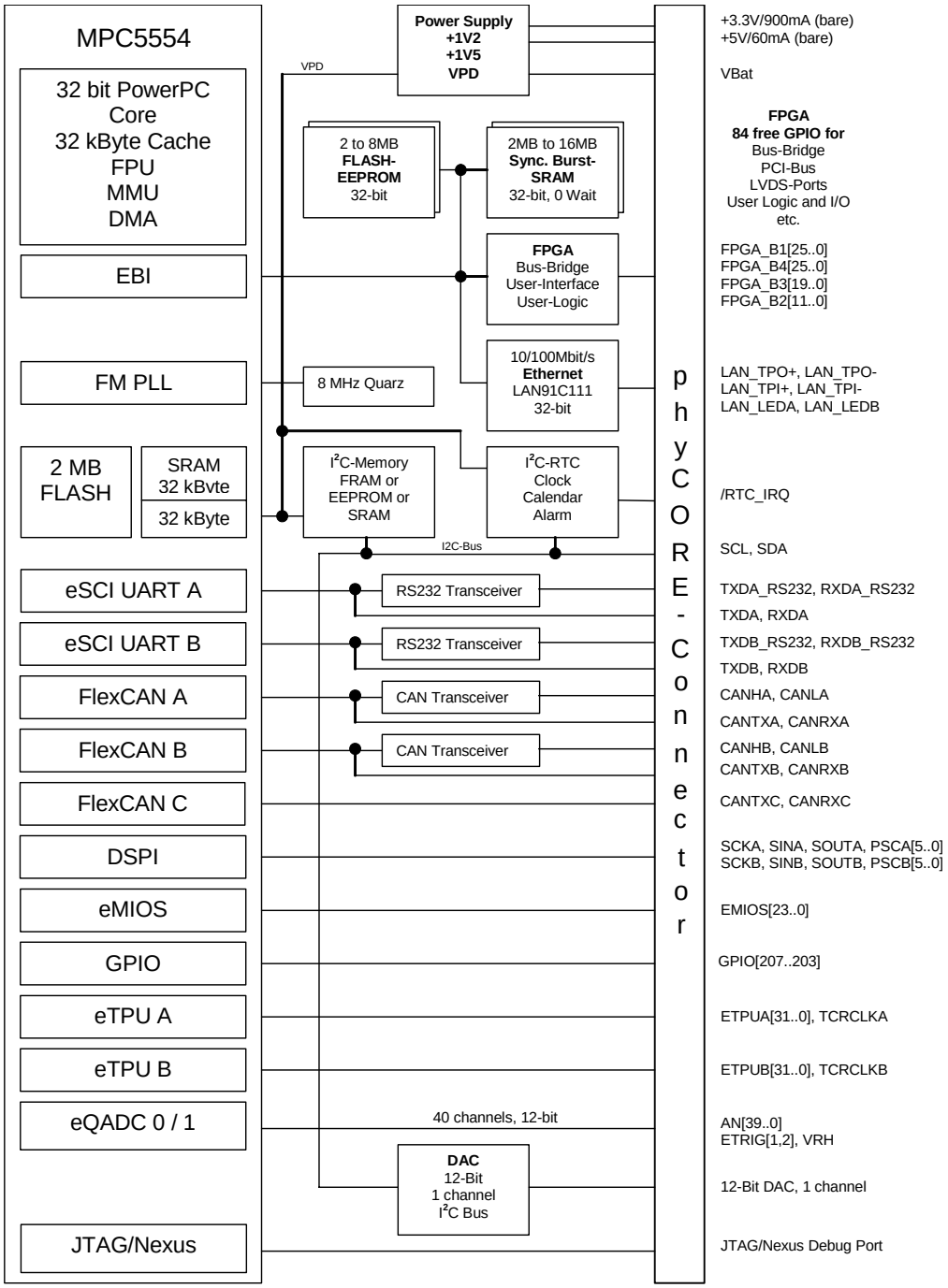

Figure 1: Block Diagram phyCORE-MPC5554

1.2 View of the phyCORE-MPC5554

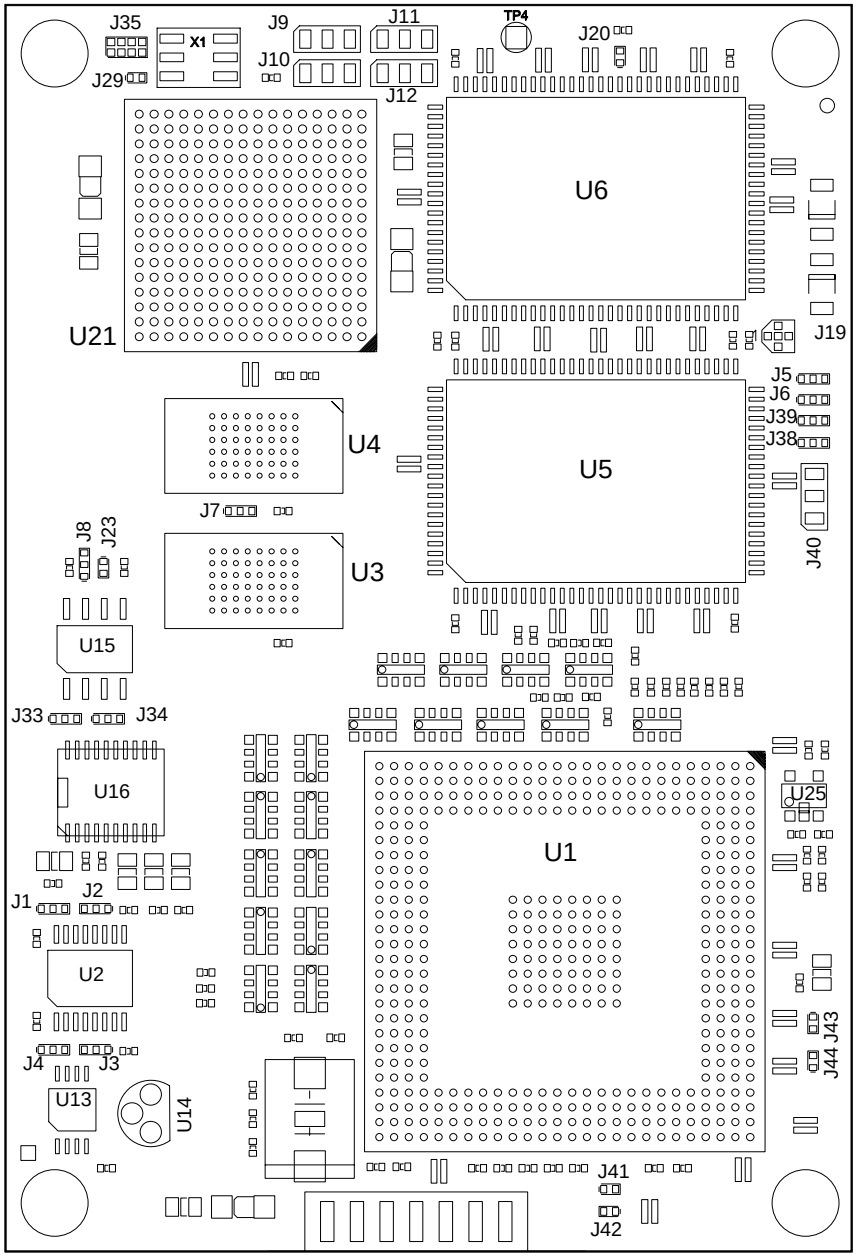

Figure 2: Top View of the phyCORE-MPC5554 Revision 1239.3

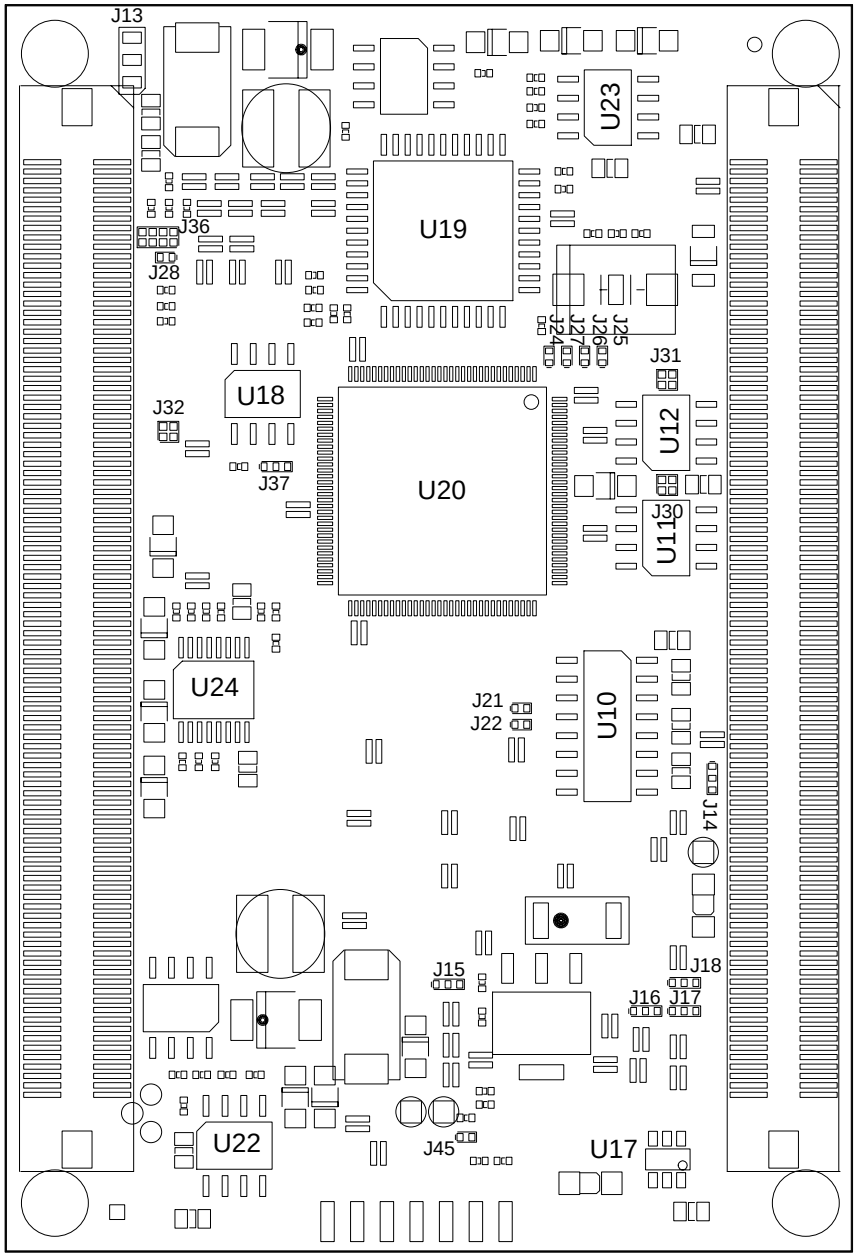

Figure 3: Bottom View of the phyCORE-MPC5554 Revision 1239.3

1.3 Minimum Requirements to Operate the phyCORE-MPC5554

Basic operation of the phyCORE-MPC5554 only requires a +3V3 and a +5 V input voltage and the corresponding DGND connections.

These supply pins are located at the phyCORE-connector X2:

+3V3	X2	1C, 2C, 1D, 2D, 4D, 5D
+5 V	X2	4C, 5C
GND	X2	3C, 3D, 7C, 9D, 12C, 14D

Caution:
We recommend connecting all available +3V3 and +5 V input pins to the power supply system on a custom carrier board housing the phyCORE-MPC5554 and at least the matching number of DGND pins neighboring the +3V3 and +5 V pins.

In addition, proper implementation of the phyCORE module into a target application also requires connecting all GND pins neighboring signals that are being used in the application circuitry.

If no further external configuration is attached, the system will start with reading the Reset Configuration Half Word (RCHW) from the internal MPC5554 Flash memory. In order to force starting from the external (on-board) Flash memory at U3/4, the /RSTCFG signal located at X2C9 must be pulled to DGND for at least the duration of the /RESET phase.

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 4* indicates, all controller signals extend to surface mount technology (SMT) connectors (0.635 mm) lining two sides of the module (referred to as phyCORE-connector; *refer to section 12*). This allows the phyCORE-MPC5554 to be plugged into any target application like a "big chip".

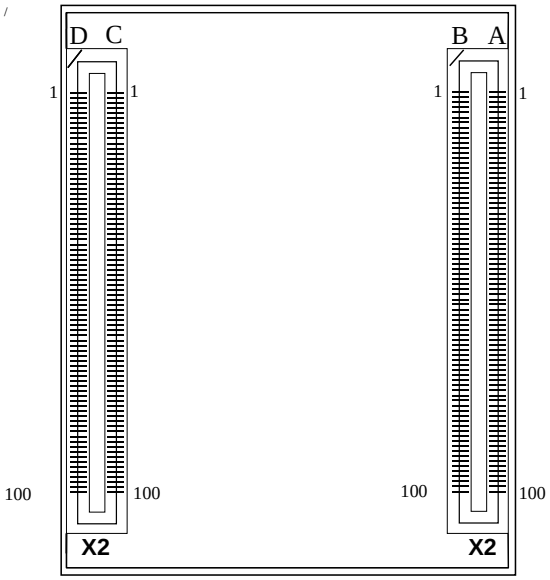

Figure 4: Pinout of the phyCORE-MPC5554 (Bottom View)

Many of the controller port pins accessible at the edges of the board have been assigned alternate functions that can be activated via software.

2.1 phyCORE equipped with MPC5554

Table 1 provides an overview of the pinout of the phyCORE-connector , as well as descriptions of possible alternative functions. *Please refer to the Freescale MPC5554 User Manual/Data Sheet for details on the functions and features of controller signals and port pins.*

Pin Number	Signal	I/O	Comments
Pin Row X2A			
1A	EXTCLK	I	Optional external clock input of the MPC5554
2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A, 82A, 87A, 92A, 97A	DGND	-	Ground 0 V
3A	IRQ4	I	IRQ4 interrupt of the MPC5554 Alternative: GPIO208
4A	IRQ5	I	IRQ5 interrupt of the MPC5554 Alternative: GPIO209
5A 6A 8A 9A 10A 11A 13A 14A 15A 16A 18A 19A 20A 21A	FPGA_B1_IO0 FPGA_B1_IO1 FPGA_B1_IO6 FPGA_B1_IO7 FPGA_B1_IO8 FPGA_B1_IO9 FPGA_B1_IO14 FPGA_B1_IO15 FPGA_B1_IO16 FPGA_B1_IO17 FPGA_B1_IO22 FPGA_B1_IO23 FPGA_B1_IO24 FPGA_B1_IO25	I/O	FPGA GPIO Top Side Bank 1 Functionality depends on the loaded FPGA firmware. The signals of a blank device are inputs with an internal weak pull-up. FPGA_VDDIO1 (Jumper J9)
23A 24A 25A 26A 28A 29A 30A 31A 33A 34A 35A 36A	FPGA_B4_IO4 FPGA_B4_IO5 FPGA_B4_IO6 FPGA_B4_IO7 FPGA_B4_IO12 FPGA_B4_IO13 FPGA_B4_IO14 FPGA_B4_IO15 FPGA_B4_IO20 FPGA_B4_IO21 FPGA_B4_IO22 FPGA_B4_IO23	I/O	FPGA GPIO Bottom Side Bank 4 Functionality depends on the loaded FPGA firmware. The signals of a blank device are inputs with an internal weak pull-up. FPGA_VDDIO4 (Jumper J10)

38A 39A 40A 41A 43A	FPGA_B2_IO0 FPGA_B2_IO1 FPGA_B2_IO2 FPGA_B2_IO3 FPGA_B2_IO8	I/O	FPGA GPIO Right Side Bank 2 Functionality depends on the loaded FPGA firmware. The signals of a blank device are inputs with an internal weak pull-up. FPGA_VDDIO2 (Jumper J11)
44A 45A 46A 48A 49A 50A 51A	FPGA_B2_IO9 FPGA_B2_IO10 FPGA_B2_IO11 FPGA_B2_IO16 FPGA_B2_IO17 FPGA_B2_IO18 FPGA_B2_IO19		
53A 54A 55A 56A	FPGA_B3_IO4 FPGA_B3_IO5 FPGA_B3_IO6 FPGA_B3_IO7	I/O	FPGA GPIO Right Side Bank 3 Functionality depends on the loaded FPGA firmware. The signals of a blank device are inputs with an internal weak pull-up.
58A	FPGA_VDDIO_B2	I	FPGA VCCIO2 of Right Side Bank 2 Alternative: FPGA_B2_IO20 (J28)
59A	FPGA_VDDIO_B3	I	FPGA VCCIO2 of Right Side Bank 3 Alternative: FPGA_B3_IO12 (J29)
60A	ETPUB30	I/O	eTPU B channel 30 Alternative: GPIO177
61A	TCRCLKB	I	eTPU B TCR clock Alternative: IRQ6, GPIO146
63A	ETPUB28	I/O	eTPU B channel 28 Alternative: GPIO175
64A	ETPUB26	I/O	eTPU B channel 26 Alternative: GPIO173
65A	ETPUB24	I/O	eTPU B channel 24 Alternative: GPIO171
66A	ETPUB22	I/O	eTPU B channel 22 Alternative: GPIO169
68A	ETPUB20	I/O	eTPU B channel 20 Alternative: GPIO167
69A	ETPUB18	I/O	eTPU B channel 18 Alternative: PCSA3, GPIO165
70A	ETPUB16	I/O	eTPU B channel 16 Alternative: PCSA1, GPIO163
71A	ETPUB14	I/O	eTPU B channel 14 Alternative: ETPUB30, GPIO161
73A	ETPUB12	I/O	eTPU B channel 12 Alternative: ETPUB28, GPIO159
74A	ETPUB10	I/O	eTPU B channel 10 Alternative: ETPUB26, GPIO157
75A	ETPUB8	I/O	eTPU B channel 8 Alternative: ETPUB24, GPIO155
76A	ETPUB6	I/O	eTPU B channel 6 Alternative: ETPUB22, GPIO153
78A	ETPUB4	I/O	eTPU B channel 4 Alternative: ETPUB20, GPIO151

79A	ETPUB2	I/O	eTPU B channel 2 Alternative: ETPUB18, GPIO149
80A	ETPUB0	I/O	eTPU B channel 0 Alternative: ETPUB16, GPIO147
81A	ETPUA30	I/O	eTPU A channel 30 Alternative: PCSC3, GPIO144
83A	ETPUA28	I/O	eTPU A channel 28 Alternative: PCSC1, GPIO142
84A	ETPUA26	I/O	eTPU A channel 26 Alternative: IRQ14, GPIO140
85A	ETPUA24	I/O	eTPU A channel 24 Alternative: IRQ12, GPIO138
86A	ETPUA22	I/O	eTPU A channel 22 Alternative: IRQ10, GPIO136
88A	ETPUA20	I/O	eTPU A channel 20 Alternative: IRQ8, GPIO134
89A	ETPUA18	I/O	eTPU A channel 18 Alternative: PCSD3, GPIO132
90A	ETPUA16	I/O	eTPU A channel 16 Alternative: PCSD1, GPIO130
91A	ETPUA14	I/O	eTPU A channel 14 Alternative: PCSB4, GPIO128
93A	ETPUA12	I/O	eTPU A channel 12 Alternative: PCSB1, GPIO126
94A	ETPUA10	I/O	eTPU A channel 10 Alternative: ETPUA22, GPIO124
95A	ETPUA8	I/O	eTPU A channel 8 Alternative: ETPUA20, GPIO122
96A	ETPUA6	I/O	eTPU A channel 6 Alternative: ETPUA18, GPIO120
98A	ETPUA4	I/O	eTPU A channel 4 Alternative: ETPUA16, GPIO118
99A	ETPUA2	I/O	eTPU A channel 2 Alternative: ETPUA14, GPIO116
100A	ETPUA0	I/O	eTPU A channel 0 Alternative: ETPUA12, GPIO114
Pin Number	**Signal**	**I/O**	**Comments**
Pin Row X2B			
1B	CLKOUT	O	Processor clock of the MPC5554
2B	IRQ2	I	IRQ2 interrupt request of the MPC5554 Alternative: GPIO211
3B	IRQ3	I	IRQ3 interrupt request of the MPC5554 Alternative: GPIO212
4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B, 84B, 89B, 94B, 99B	DGND	-	Ground 0 V

5B	FPGA_B1_IO2	I/O	FPGA GPIO Top Side Bank 1
6B	FPGA_B1_IO3	I/O	
7B	FPGA_B1_IO4	I/O	Functionality depends on the loaded FPGA firmware.
8B	FPGA_B1_IO5	I/O	
10B	FPGA_B1_IO10	I/O	The signals of a blank device are inputs with an internal weak pull-up.
11B	FPGA_B1_IO11	I/O	
12B	FPGA_B1_IO12	I/O	
13B	FPGA_B1_IO13	I/O	
15B	FPGA_B1_IO18	I/O	
16B	FPGA_B1_IO19	I/O	
17B	FPGA_B1_IO20	I/O	
18B	FPGA_B1_IO21	I/O	
20B	FPGA_B4_IO0	I/O	FPGA GPIO Bottom Side Bank 4
21B	FPGA_B4_IO1	I/O	
22B	FPGA_B4_IO2	I/O	Functionality depends on the loaded FPGA firmware.
23B	FPGA_B4_IO3	I/O	
25B	FPGA_B4_IO8	I/O	
26B	FPGA_B4_IO9	I/O	The signals of a blank device are inputs with an internal weak pull-up.
27B	FPGA_B4_IO10	I/O	
28B	FPGA_B4_IO11	I/O	
30B	FPGA_B4_IO16	I/O	
31B	FPGA_B4_IO17	I/O	
32B	FPGA_B4_IO18	I/O	
33B	FPGA_B4_IO19	I/O	
35B	FPGA_B4_IO24	I/O	
36B	FPGA_B4_IO25	I/O	
37B	FPGA_VDDIO_B1	I	FPGA VCCIO1 of Top Side Bank 1
38B	FPGA_VDDIO_B4	I	FPGA VCCIO4 of Bottom Side Bank 2
40B	FPGA_B2_IO4	I/O	FPGA GPIO Right Side Bank 2
41B	FPGA_B2_IO5	I/O	
42B	FPGA_B2_IO6	I/O	Functionality depends on the loaded FPGA firmware.
43B	FPGA_B2_IO7	I/O	
45B	FPGA_B2_IO12	I/O	
46B	FPGA_B2_IO13	I/O	The signals of a blank device are inputs with an internal weak pull-up.
47B	FPGA_B2_IO14	I/O	
48B	FPGA_B2_IO15	I/O	
50B	FPGA_B3_IO0	I/O	FPGA GPIO Right Side Bank 3
51B	FPGA_B3_IO1	I/O	
52B	FPGA_B3_IO2	I/O	Functionality depends on the loaded FPGA firmware.
53B	FPGA_B3_IO3	I/O	
55B	FPGA_B3_IO8	I/O	
56B	FPGA_B3_IO9	I/O	The signals of a blank device are inputs with an internal weak pull-up.
57B	FPGA_B3_IO10	I/O	
58B	FPGA_B3_IO11	I/O	
60B	ETPUB31	I/O	eTPU B channel 31 Alternative: GPIO178
61B	ETPUB29	I/O	eTPU B channel 29 Alternative: GPIO176
62B	ETPUB27	I/O	eTPU B channel 27 Alternative: GPIO174

63B	ETPUB25	I/O	eTPU B channel 25 Alternative: GPIO172
65B	ETPUB23	I/O	eTPU B channel 23 Alternative: GPIO170
66B	ETPUB21	I/O	eTPU B channel 21 Alternative: GPIO168
67B	ETPUB19	I/O	eTPU B channel 19 Alternative: PCSA4, GPIO166
68B	ETPUB17	I/O	eTPU B channel 17 Alternative: PCSA2, GPIO164
70B	ETPUB15	I/O	eTPU B channel 15 Alternative: ETPUB31, GPIO162
71B	ETPUB13	I/O	eTPU B channel 13 Alternative: ETPU29, GPIO160
72B	ETPUB11	I/O	eTPU B channel 11 Alternative: ETPU27, GPIO158
73B	ETPUB9	I/O	eTPU B channel 9 Alternative: ETPU25, GPIO156
75B	ETPUB7	I/O	eTPU B channel 7 Alternative: ETPU23, GPIO154
76B	ETPUB5	I/O	eTPU B channel 5 Alternative: ETPU21, GPIO152
77B	ETPUB3	I/O	eTPU B channel 3 Alternative: ETPU19, GPIO150
78B	TCRCLKA	I	eTPU A TCR clock Alternative: IRQ7, GPIO113
80B	ETPUB1	I/O	eTPU B channel 1 Alternative: ETPU17, GPIO148
81B	ETPUA31	I/O	eTPU A channel 31 Alternative: PCSC4, GPIO145
82B	ETPUA29	I/O	eTPU A channel 29 Alternative: PCSC2, GPIO143
83B	ETPUA27	I/O	eTPU A channel 27 Alternative: IRQ15, GPIO141
85B	ETPUA25	I/O	eTPU A channel 25 Alternative: IRQ13, GPIO139
86B	ETPUA23	I/O	eTPU A channel 23 Alternative: IRQ11, GPIO137
87B	ETPUA21	I/O	eTPU A channel 27 Alternative: IRQ9, GPIO135
88B	ETPUA19	I/O	eTPU A channel 19 Alternative: PCSD4, GPIO133
90B	ETPUA17	I/O	eTPU A channel 17 Alternative: PCSD2, GPIO131
91B	ETPUA15	I/O	eTPU A channel 15 Alternative: PCSB5, GPIO129
92B	ETPUA13	I/O	eTPU A channel 13 Alternative: PCSB3, GPIO127
93B	ETPUA11	I/O	eTPU A channel 11 Alternative: ETPUA23, GPIO125
95B	ETPUA9	I/O	eTPU A channel 9 Alternative: ETPUA21, GPIO123

96B	ETPUA7	I/O	eTPU A channel 7 Alternative: ETPUA19, GPIO121
97B	ETPUA5	I/O	eTPU A channel 5 Alternative: ETPUA17, GPIO119
98B	ETPUA3	I/O	eTPU A channel 3 Alternative: ETPUA15, GPIO117
100B	ETPUA1	I/O	eTPU A channel 1 Alternative: ETPUA13, GPIO115
Pin Number	**Signal**	**I/O**	**Comments**
Pin Row X2C			
1C, 2C	VDD3V3	I	Supply voltage +3.3 VDC
3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 72C	DGND	-	Ground 0 V
4C, 5C	VDD5V	I	Supply voltage +5 VDC
6C	VBAT	I	Connection for external battery (+) 2.4-3.3 V
8C	PWRGOOD	O	Power Good logic output signal
9C	/RSTCFG	I	Reset Configuration Input of the MPC5554 Alternative: GPIO210
10C	/RESET	I/O	Reset signal of the phyCORE. /Reset is controlled by the on-board voltage supervisor circuitry (open-drain driver). The voltage supervisor monitors the input voltages VDD3V3, VDD5V and the on-board generated voltages. The reset delay amounts to 200 ms after all voltages reach a valid level. /RESET has a 10kOhm pull-up.
11C	/RSTOUT	O	Reset output of the MPC5554. /RSTOUT reflects the /RESET signal and can be asserted by software without internal MPC5554 reset.
13C	EMIOS1	I/O	eMIOS channel 1 of the MPC5554. Alternative: ETPUA1, GPIO180
14C	EMIOS3	I/O	eMIOS channel 3 of the MPC5554. Alternative: ETPUA3, GPIO182
15C	EMIOS5	I/O	eMIOS channel 5 of the MPC5554. Alternative: ETPUA5, GPIO184
16C	EMIOS7	I/O	eMIOS channel 7 of the MPC5554. Alternative: ETPUA7, GPIO186
18C	CANHB	I/O	CANH signal of the CAN transceiver of the MPC5554 FlexCAN B. Alternative: PCSC3, GPIO85
19C	RXDB	I	Receive line of the MPC5554 eSCI channel B. Alternative: PCSD5, GPO92 When the alternative function is used, the solder jumper J22 must be open in order to disconnect the receive output of the RS-232 transceiver.
20C	TXDB	O	Transmit line of the MPC5554 eSCI channel B. Alternative: PCSD1, GPIO91

21C	RXDB_RS232	I	RxD input of the RS-232 transceiver for the MPC5554 eSCI channel B. J22 must be closed in order to use this interface.
23C	TXDB_RS232	O	TxD output of the RS-232 transceiver for the MPC5554 eSCI channel B.
24C	CNRXC	I	FlexCAN C receive line of the MPC5554. Alternative: PCSC4, GPIO86
25C	CNTXC	O	FlexCAN C transmit line of the MPC5554. Alternative: PCSC3, GPIO87
26C	EMIOS9	I/O	eMIOS channel 9 of the MPC5554. Alternative: ETPUA9, GPIO188
28C	EMIOS11	I/O	eMIOS channel 11 of the MPC5554. Alternative:GPIO190
29C	EMIOS13	O	eMIOS channel 13 of the MPC5554. Alternative:SOUTD, GPIO192
30C	EMIOS15	O	eMIOS channel 15 of the MPC5554. Alternative:IRQ1, GPIO194
31C	SCL	I/O	I^2C bus clock signal connected to the RTC, the serial memory and the DAC: The signal can be generated with the FPGA signal at ball E2 (I^2C bus master IP core)..
33C	LAN_LEDA	O	Ethernet LED output signal of the LAN91C111 controller.
34C	LAN_LEDB	O	Ethernet LED output signal of the LAN91C111 controller.
35C	LAN_TPI-	I	Ethernet negative receive input of the LAN91C111 controller.
36C	LAN_TPO-	O	Ethernet negative transmit output of the LAN91C111 controller.
38C	EMIOS17	I/O	eMIOS channel 17 of the MPC5554. Alternative:ETPU1, GPIO196
39C	EMIOS19	I/O	eMIOS channel 19 of the MPC5554. Alternative:ETPU3, GPIO198
40C	EMIOS21	I/O	eMIOS channel 21 of the MPC5554. Alternative:ETPU5, GPIO200
41C	EMIOS23	I/O	eMIOS channel 23 of the MPC5554. Alternative:ETPU7, GPIO202
43C	GPIO204	I/O	GPIO204 of the MPC5554 Alternative: EMIOS15 – caution EMIOS is primary function (O)
44C	GPIO206	I/O	GPIO206 of the MPC5554. Alternative: ETRIG0
45C	SINA	I	DSPI A data input of the MPC5554. Alternative: PCSC2, GPIO94
46C	SOUTA	O	DSPI A data output of the MPC5554. Alternative: PCSC5, GPIO95
48C	PCSA1	O	DSPI A chip select 1 of the MPC5554. Alternative: PCSB2, GPIO97
49C	PCSA3	O	DSPI A chip select 3 of the MPC5554. Alternative: SIND, GPIO99
50C	PCSA5	O	DSPI A chip select 5 of the MPC5554. Alternative: PCSB3, GPIO101

51C	SINB	I	DSPI B data input of the MPC5554 Alternative: PCSC2, GPIO103
53C	SOUTB	O	DSPI B data output of the MPC5554. Alternative: PCSC5, GPIO104
54C	PCSB1	O	DSPI B chip select 1 of the MPC5554. Alternative: PCSD0, GPIO106
55C	PCSB3	O	DSPI B chip select 3 of the MPC5554. Alternative: SINC, GPIO108
56C	PCSB5	O	DSPI B chip select 5 of the MPC5554. Alternative: PCSC0, GPIO110
58C	/TEST	I	Test mode select of the MPC5554. /TEST has a 10kOhm pull-up.
59C	JCOMP	I	JTAG TAP controller enable of the MPC5554. JCOMP has a 10kOhm pull-down.
60C	MPC_TDI	I	JTAG test data input of the MPC5554. MPC_TDI has a 10kOhm pull-up.
61C	MPC_TCK	I	JTAG test clock input of the MPC5554. MPC_TCK has a 10kOhm pull-down.
63C	MPC_TMS	I	JTAG test mode select input of the MPC5554. MPC_TMS has a 10kOhm pull-up.
64C 65C	MSEO0 MSEO1	O O	Nexus message start/end out of the MPC5554.
66C 68C 69C 70C 71C	MDO0 MDO2 MDO4 MDO6 MDO8	O O O O O	Nexus message data out of the MPC5554
73C	DAC0	O	Analog output of the 12-bit DAC device U19. Vout = VDD3V3 x D/4096
74C	ETRIG1	I	eQADC trigger input 1 of the MPC5554. Alternative: GPIO112
75C	ETRIG0	I	eQADC trigger input 0 of the MPC5554. Alternative: GPIO111
76C 78C 79C 80C 81C 83C 84C 85C 86C 88C 89C 90C	AN38 AN36 AN34 AN32 AN30 AN28 AN26 AN24 AN22 AN20 AN18 AN16	I I I I I I I I I I I I	eQADC analog input of the MPC5554.
77C, 82C, 87C, 92C, 97C	AGND	-	Analog Ground 0 V
91C	AN14	I	eQADC analog input 14 of the MPC5554. Alternative: MA2, SDI
93C	AN12	I	eQADC analog input 12 of the MPC5554. Alternative: MA0, /SDS

94C	AN10	I	eQADC analog input 10 of the MPC5554. Alternative: ANY
95C	AN8	I	eQADC analog input 8 of the MPC5554. Alternative: ANW
96C	AN6	I	eQADC analog input 6 of the MPC5554. Alternative: DAN3+
98C	AN4	I	eQADC analog input 4 of the MPC5554. Alternative: DAN2+
99C	AN2	I	eQADC analog input 2 of the MPC5554. Alternative: DAN1+
100C	AN0	I	eQADC analog input 0 of the MPC5554. Alternative: DAN0+
Pin Number	**Signal**	**I/O**	**Comments**
Pin Row X2D			
1D, 2D, 4D, 5D	VDD3V3	I	Supply voltage +3.3 VDC
3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D	DGND	-	Ground 0 V
6D	VPD	O	Power-down supply voltage VPD is generated by VBAT or VDD3V3 using a diode switcher. VPD serves as supply voltage for the MPC5554 internal SRAM, the Real-Time Clock and the serial memory device at U15.
7D	/WDO	O	Watchdog timeout signal. A logic rising or falling edge must occur on WDI within a time-out period of 940 ms to prohibit a high-to-low transition of the /WDO signal. /WDO has a 10kOhm pull-up.
8D	WDI	I	Watchdog trigger input signal. WDI has a 10kOhm pull-up to VDD3V3.
10D	NC	-	Not connected. Do not use this pin!
11D	EMIOS0	I/O	eMIOS channel 0 of the MPC5554. Alternative: ETPUA0, GPIO179
12D	EMIOS2	I/O	eMIOS channel 2 of the MPC5554. Alternative: ETPUA2, GPIO181
13D	EMIOS4	I/O	eMIOS channel 4 of the MPC5554. Alternative: ETPUA4, GPIO183
15D	EMIOS6	I/O	eMIOS channel 6 of the MPC5554. Alternative: ETPUA6, GPIO185
16D	RXDA	I	Receive line of the MPC5554 eSCI UART A. Alternative: GPIO90 If the alternative function is used, the solder jumper J21 must be opened in order to disconnect the receive output of the RS-232 transceiver.
17D	TXDA	O	Transmit line of the MPC5554 eSCI UART A. Alternative: GPIO89

18D	CANLB	I/O	CANL signal of the CAN transceiver of the MPC5554 FlexCAN B interface. Alternative: PCSC4, GPIO86
20D	CANLA	I/O	CANL signal of the CAN transceiver of the MPC5554 FlexCAN A interface. Alternative: GPIO84
21D	CANHA	I/O	CANH signal of the CAN transceiver of the MPC5554 FlexCAN A. Alternative: GPIO83
22D	RXDA_RS232	I	RxD input of the RS-232 transceiver for the MPC5554 eSCI channel A. J21 must be closed in order to use this interface.
23D	TXDA_RS232	O	TxD output of the RS-232 transceiver for the MPC5554 eSCI channel A.
25D	EMIOS8	I/O	eMIOS channel 8 of the MPC5554. Alternative: ETPUA8, GPIO187
26D	EMIOS10	I/O	eMIOS channel 10 of the MPC5554. Alternative: GPIO189
27D	EMIOS12	I/O	eMIOS channel 12 of the MPC5554. Alternative: SOUTC, GPIO191
28D	EMIOS14	I/O	eMIOS channel 14 of the MPC5554. Alternative: IRQ0, GPIO193
30D	EMIOS16	I/O	eMIOS channel 16 of the MPC5554. Alternative: ETPUB0, GPIO195
31D	EMIOS18	I/O	eMIOS channel 18 of the MPC5554. Alternative: ETPUB2, GPIO197
32D	SDA	I/O	Data line of the I^2C bus connected to the RTC, the serial memory and the DAC. The signal can be generated with the FPGA signal at ball G4 (I^2C bus master IP core).
33D	/RTC_IRQ	O	Interrupt output of the RTC.
35D	LAN_TPI+	I	Ethernet positive receive input of the LAN91C111 controller.
36D	LAN_TPO+	O	Ethernet positive transmit output of the LAN91C111 controller.
37D	DQ1WIRE	I/O	1-Wire bus signal. This signal can be generated with the FPGA signal at ball E1 (1-Wire Bus Master IP core).
38D	EMIOS20	I/O	eMIOS channel 20 of the MPC5554. Alternative: ETPUB4, GPIO199
40D	EMIOS22	I/O	eMIOS channel 22 of the MPC5554. Alternative: ETPUB6, GPIO201
41D	GPIO203	I/O	GPIO203 of the MPC5554 Alternative: EMIOS14 – caution EMIOS is primary function (O)
42D	GPIO205	I/O	GPIO205 of the MPC5554
43D	GPIO207	I/O	GPIO207 of the MPC5554. Alternative: ETRIG1
45D	SCKA	I/O	DSPI A clock of the MPC5554. Alternative: PCSC1, GPIO93
46D	PCSA0	O	DSPI A chip select 0 of the MPC5554. Alternative: PCSD2, GPIO96

47D	PCSA2	O	DSPI A chip select 2 of the MPC5554. Alternative: SCKD, GPIO98
48D	PCSA4	O	DSPI A chip select 4 of the MPC5554. Alternative: SOUTD, GPIO100
50D	SCKB	I/O	DSPI B clock of the MPC5554. Alternative: PCSC1, GPIO102
51D	PCSB0	O	DSPI B chip select 0 of the MPC5554. Alternative: PCSD2, GPIO105
52D	PCSB2	O	DSPI B chip select 2 of the MPC5554. Alternative: SOUTC, GPIO107
53D	PCSB4	O	DSPI B chip select 4 of the MPC5554. Alternative: SCKC, GPIO109
55D	FPGA_TMS	I	JTAG test mode select input of the FPGA. FPGA_TMS has a 10kOhm pull-up to VDD3V3.
56D	FPGA_TDI	I	JTAG test data input of the FPGA. FPGA_TDI has a 10kOhm pull-up to VDD3V3.
57D	FPGA_TDO	O	JTAG test data output of the FPGA.
58D	FPGA_TCK	I	JTAG test clock input of the FPGA. MPC_TCK has a 10kOhm pull-down.
60D	MPC_TDO	O	JTAG test data output of the MPC5554.
61D	/EVTO	O	Nexus event output signal of the MPC5554.
62D	/EVTI	I	Nexus event input signal of the MPC5554.
63D	/RDY	O	Nexus ready output signal of the MPC5554.
65D	MCKO	O	Nexus message clock output of the MPC5554.
66D 67D 68D 70D 71D 72D 73D	MDO1 MDO3 MDO5 MDO7 MDO9 MDO10 MDO11	O O O O O O O	Nexus message data out of the MPC5554
74D, 79D, 84D, 89D, 94D, 99D	AGND	-	Analog Ground 0 V
75D 76D 77D 78D 80D 81D 82D 83D 85D 86D 87D 88D	AN39 AN37 AN35 AN33 AN31 AN29 AN27 AN25 AN23 AN21 AN19 AN17	I I I I I I I I I I I I	eQADC analog input of the MPC5554.
90D	AN15	I	eQADC analog input 15 of the MPC5554. Alternative: FCK
91D	AN13	I	eQADC analog input 13 of the MPC5554. Alternative: MA1, SDO
92D	AN11	I	eQADC analog input 11 of the MPC5554. Alternative: ANZ

93D	AN9	I	eQADC analog input 9 of the MPC5554. Alternative: ANX
95D	AN7	I	eQADC analog input 7 of the MPC5554. Alternative: DAN3-
96D	AN5	I	eQADC analog input 5 of the MPC5554. Alternative: DAN2-
97D	AN3	I	eQADC analog input 3 of the MPC5554. Alternative: DAN1-
98D	AN1	I	eQADC analog input 1 of the MPC5554. Alternative: DAN0-
100D	VRH	O	Reference voltage of the eQADC module.

Table 1: Pinout of the phyCORE-Connector X2 for MPC5554

2.2 phyCORE equipped with MPC5567

Most of the signals are equivalent to those are listed in *Table 1* for the MPC5554. *Table 1* shows only the pins those are different. *Please refer to the Freescale MPC5567 User Manual/Data Sheet for details on the functions and features of controller signals and port pins.*

Pin Number	Signal	I/O	Comments
Pin Row X2A			
60A	FEC_TXD3	O	Ethernet Transmit Data Bit 3
61A	NC		Not connected
63A	FEC_TXD1	O	Ethernet Transmit Data Bit 1
64A	FEC_TX_EN	O	Ethernet Transmit Enable
65A	FEC_TX_CLK	I	Ethernet Transmit Clock
66A	NC		
68A	VDDE13	I	Power Supply Input 1,8..3,3V
69A	NC		
70A	NC		
71A	FEC_RX_DV	I	Ethernet Receive Data Valid
73A	FEC_MDC	O	Ethernet Management Clock
74A	VDDE12	I	Power Supply Input 1,8..3,3V
75A	FEC_RXD2	I	Ethernet Receive Data Bit 2
76A	REC_MDIO	I/O	Ethernet Management Data I/O
78A	NC		Not connected
79A	NC		Not connected
80A	NC		Not connected
96A	FRB_RX	I	FlexRay B Reveive Data Alternative: GPIO120
98A	FRB_TX	O	FlexRay B Transmit Data Alternative: GPIO118
Pin Number	**Signal**	**I/O**	**Comments**
Pin Row X2B			
60B	FEC_TXD0	O	Ethernet Transmit Data Bit 0

61B	VDDE13	I	Power Supply Input 1,8..3,3V
62B	FEC_TX_ER	O	Ethernet Transmit Error
63B	FEX_TXD2	O	Ethernet Transmit Data Bit 2
65B	FEC_CRS	I	Ethernet Carrier Detect
66B	NC		Not connected
67B	NC		Not connected
68B	FEC_COL	I	Ethernet Collision Detect
70B	FEC_RX_ER	I	Ethernet Receive Error
71B	VDDE12	I	Power Supply Input 1,8..3,3V
72B	FEC_RXD3	I	Ethernet Receive Data Bit 3
73B	FEC_RX_CLK	I	Ethernet Receive Clock
75B	FEC_RXD1	I	Ethernet Receive Data Bit 1
76B	FEC_RXD0	I	Ethernet Receive Data Bit 0
77B	NC		Not connected
80B	NC		Not connected
97B	FRB_TX_EN	O	FlexRay B Transmit Enable Alternative: GPIO119
Pin Number	**Signal**	**I/O**	**Comments**
Pin Row X2C			
18C	FRA_TX	O	FlexRay A Transmit Data Alternative: GPIO85
Pin Number	**Signal**	**I/O**	**Comments**
Pin Row X2D			
18D	FRA_RX	I	FlexRay A Receive Data Alternative: GPIO86
52D	FRA_TX_EN	O	FlexRay A Transmit Enable Alternative: GPIO107

Table 2: Pinout of the phyCORE-Connector X2 for MPC5567

3 Jumpers

For configuration purposes, the phyCORE-MPC5554 has 37 solder jumpers, some of which have been installed prior to delivery. *Figure 5* illustrates the numbering of the jumper pads, while *Figure 6* and *Figure 7* indicate the location of the jumpers on the board.

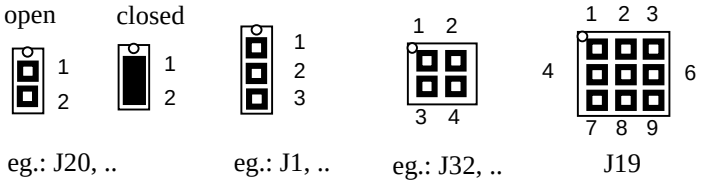

Figure 5: Numbering of the Jumper Pads

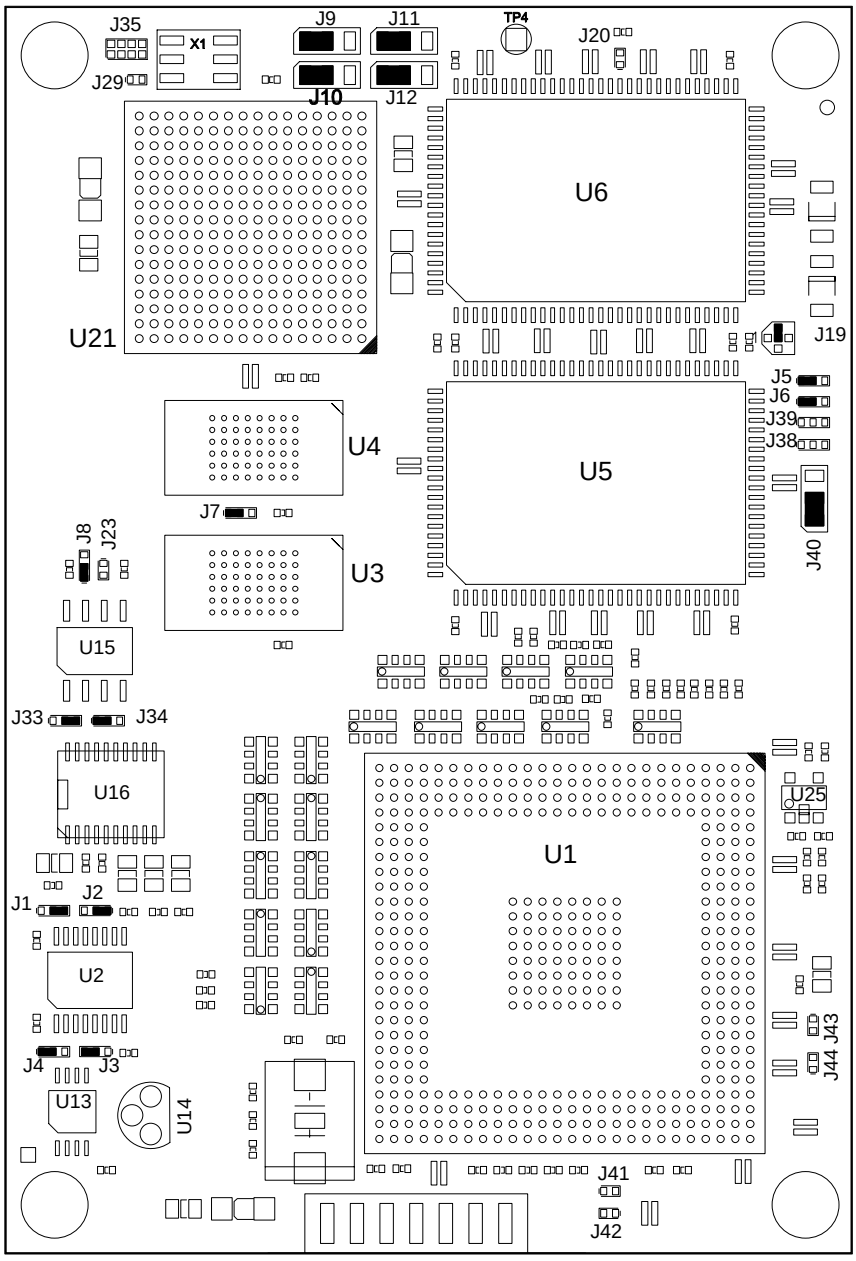

Figure 6: Location of the Jumpers (Controller Side) and Default Settings (phyCORE-MPC5554 Standard Version)[1]

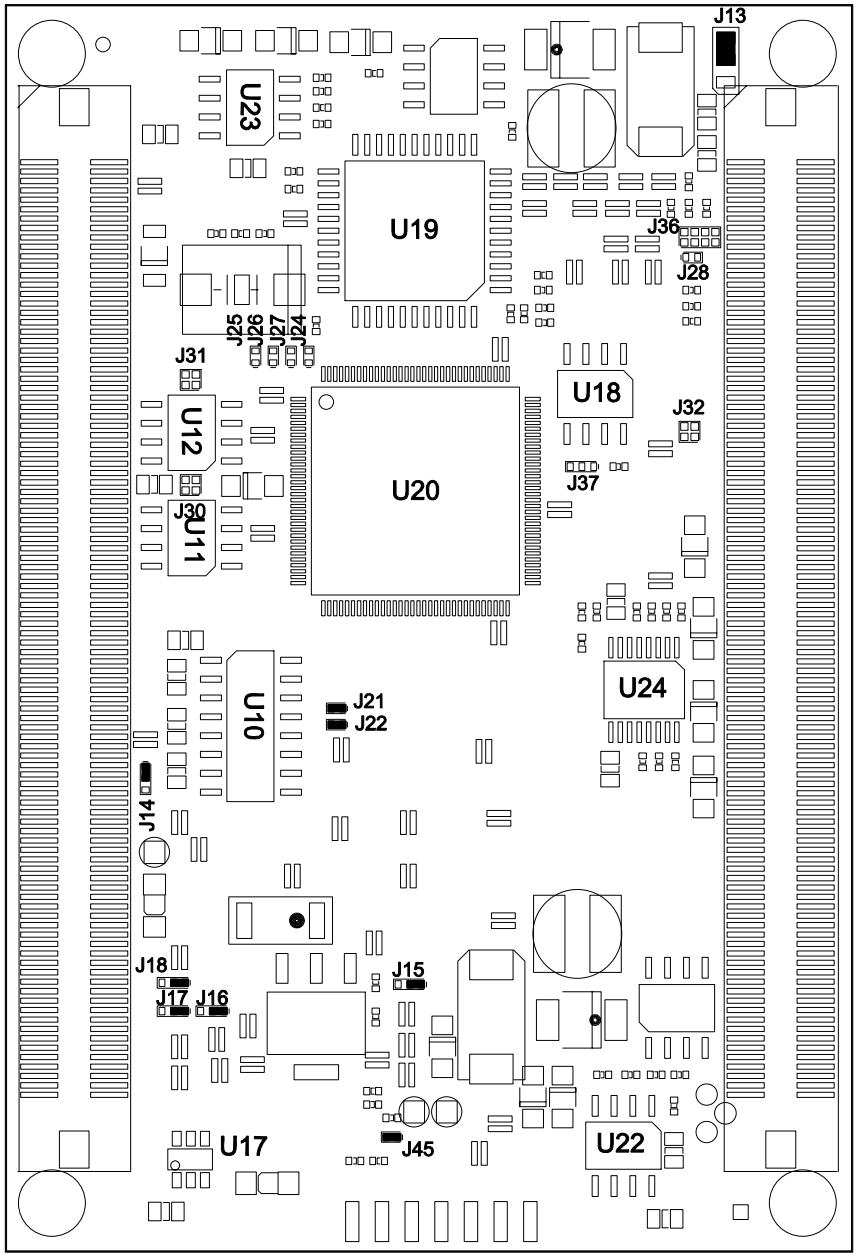

Figure 7: Location of the Jumpers (Connector Side) and Default Settings (phyCORE-MPC5554 Standard Version)[1]

[1]: Jumper J19 may have different settings according to the purchased memory configuration of the phyCORE-MPC5554.

The jumpers (J = solder jumper) have the following functions:

Jumper	Default	Comment
J1, J2		PLLCFG[1..0] selects the clock configuration.
2 + 3, 1 + 2	X	Crystal reference mode.
Package Type		0R in SMD 0402
J3, J4		BOOTCFG[1..0] selects the boot configuration for the mode /RSTCONF=0 (external memory boot mode).
2 + 3, 1 + 2	X	Configures the MCU to start from external Flash devices U3/4 controlled by /CS0.
Package Type		0R in SMD 0402
J5, J6		J5 and J6 configure the CAN transceivers of FlexCAN channels A and B provided by the MPC5554. 82C250 compatible devices are used as transceivers. Using a resistor tied to DGND, the rise time of the CAN signal edge can be configured. With a 0R solder jumper against VDD3V3, the transceivers are switched to stand-by.
1 + 2	X	0R resistor: minimal rise time
1 + 2		To reduce electromagnetic interference (EMI), a suitable resistor can populate the module in support of a lower baud rates.
2 + 3		0R resistor: Stand-by
Package Type		SMD 0402
J7		J7 selects the source of the Flash memory (U3/4) Chip Select signal.
1 + 2	X	Selects the MPC5554 /CS0.
2 + 3		Selects the CPLD driven /FLASH_CS.
Package Type		0R in SMD 0402
J8		J8 selects the supply voltage (VPD or VDD3V3) of the serial memory. VPD is used in the case that a serial SRAM, which requires buffering of its memory contents, populates the module. For EEPROM and FRAM memory, VDD3V3 is used, as these memory devices are non volatile.
1 + 2	X	The serial memory is supplied with VDD3V3.
2 + 3		The serial memory is supplied with VPD.
Package Type		0R in SMD 0402
Jumper	**Default**	**Comment**
J9		J9 selects the Bank 1 I/O voltage of the FPGA device U21B for the Top Side Bank 1.
1 + 2	X	Connected to on-board voltage VDD3V3.
2 + 3		Selects the external supplied FPGA_VDDIO_B1 from the

Jumper	Default	Comment
		module connector X2 pin 37B.
Package Type		0R in SMD 0805
J10		J10 selects the Bank 4 I/O-voltage of the FPGA device U21E for the Bottom Side Bank 4.
1 + 2	X	Connected to on-board voltage VDD3V3.
2 + 3		Selects the external supplied FPGA_VDDIO_B4 from the module connector X2 pin 38B.
Package Type		0R in SMD 0805
J11		J11 selects the Bank 2 I/O voltage of the FPGA device U21C for the Right Side Bank 2.
1 + 2	X	Connected to on-board voltage VDD3V3.
2 + 3		Selects the external supplied FPGA_VDDIO_B2 from the module connector X2 pin 58A.
Package Type		0R in SMD 0805
J12		J12 selects the Bank 1 I/O-voltage of the FPGA device U21D for the Right Side Bank 3.
1 + 2	X	Connected to on-board voltage VDD3V3.
2 + 3		Selects the external supplied FPGA_VDDIO_B3 from the module connector X2 pin 59A.
Package Type		0R in SMD 0805
J13		J13 selects the core voltage for the FPGA device U21.
1 + 2		Connects VDDFPGA to the on-board power supply circuitry U23 that generates a local FPGA core voltage. Depending on the resistors (R107-109) of the voltage feedback path, 1V2, 1V8 or 2V5 can be configured. The factory default configuration is 1V2 to support the Lattice XP "E" devices.
2 + 3	X	Connects VDDFPGA to the board voltage VDD3V3. This is applicable only for the Lattice XP "C" devices.
Package Type		0R in SMD 0805
J14		J14 selects the input voltage for the MPC5554 VDDEH1 power input.
1 + 2	X	VDDEH1 is connected to VDD3V3.
2 + 3		VDDEH1 is connected to VDD5V.
Package Type		0R in SMD 0402

Jumper	Default	Comment
J15		J15 selects the input voltage for the MPC5554 VDDEH4 power input.
1 + 2 2 + 3	X	VDDEH4 is connected to VDD3V3. VDDEH4 is connected to VDD5V.
Package Type		0R in SMD 0402
J16		J16 selects the input voltage for the MPC5554 VDDEH6 power input.
1 + 2 2 + 3	X	VDDEH6 is connected to VDD3V3. VDDEH6 is connected to VDD5V.
Package Type		0R in SMD 0402
J17		J17 selects the input voltage for the MPC5554 VDDEH8 power input.
1 + 2 2 + 3	X	VDDEH8 is connected to VDD3V3. VDDEH8 is connected to VDD5V.
Package Type		0R in SMD 0402
J18		J18 selects the input voltage for the MPC5554 VDDEH9 power input.
1 + 2 2 + 3	X	VDDEH9 is connected to VDD3V3. VDDEH9 is connected to VDD5V.
Package Type		0R in SMD 0402
J19		J19 connects the memory bank address signal BA to the corresponding address lines of the processor. The configuration of these jumper is dependent on the memory size of the Synchronous Burst SRAM populating the module (U5 and U6). The factory setting of J19 is in accordance with the memory configuration of each individual module. The two memory banks are typically equipped with the same devices.
1 + 5 2 + 5 3 + 5 4 + 5		BA=A11: 8 MBit memory devices at U5/U6 BA=A10: 16 MBit memory devices at U5/U6 BA=A9: 32 MBit memory devices at U5/U6 BA=A8: 64 MBit memory devices at U5/U6
Package Type		0R in SMD 0402

Jumper	Default	Comment
J20		J20 connects the ZZ lines of all four SRAM memory devices U5-8 to the MPC5554 GPIO205. ZZ is also connected to ball L2 of the FPGAU21G. This enables the phyCORE SRAM banks to be switched to an energy saving state via software. During this state, the memory cannot be read or written to. ZZ has a pull-down resistor.
open	X	Disconnects ZZ from the MPC5554 GPIO205.
closed		Connects ZZ to the MPC5554 GPIO205.
Package Type		0R in SMD 0402
J21, J22		J21 and J22 disconnect the receive lines of MPC5554 UART from the RS-232 transceiver at U10. This makes the controller's SCI/UART TTL level signals available at pins X2D16 (RXDA) and X2C19 (RXDB). This is useful, for instance, for galvanic isolation of the RS-232 interface.
open		The SCI/UART receive signals RXDA and RXDB are disconnected from the RS-232 transceiver.
closed	X	The SCI/UART receive signals RXDA and RXDB are connected to the RS-232 transceiver.
Package Type		0R in SMD 0402
J23		J23 connects pin 7 of the serial memory at U15 to VDD3V3. On many memory devices pin 7 enables the activation of a write protect function. It is not guaranteed that the standard serial memory populating the phyCORE-MCF548x will have this write protection function. *Please refer to the corresponding memory data sheet for more detailed information.*
open	X	
closed		
Package Type		0R in SMD 0402
J24-27		J24-27 are for internal PHYTEC use only. Do not modify the configuration!
open	X	
closed		
Package Type		0R in SMD 0402

Jumper	Default	Comment
J28		J28 connects the signal FPGA_VDDIO_B2 with the GPIO FPGA_B2_IO20 signal. This alternative may be used to route the GPIO pin to the module connector X2A58 if the FPGA block 2 is supplied with the internal VDD3V3 (J11=1 + 2).
open	X	
closed		
Package Type		0R in SMD 0402
J29		J29 connects the signal FPGA_VDDIO_B3 with the GPIO FPGA_B3_IO12 signal. This alternative may be used to route the GPIO pin to the system connector X2A59 if the FPGA block 3 is supplied with the internal VDD3V3 (J12=1 + 2).
open	X	
closed		
Package Type		0R in SMD 0402
J30	open	J30 can be used to route the FlexCAN signals of port CANA to the module connector. This jumper must only be closed if the transceiver circuit U11 is removed. Useful for optical isolation of CAN signals.
1 + 2		Connects CANTXA with CANHA pin at X2D21.
3 + 4		Connects CANRXA with CANLA pin at X2D20.
Package Type		0R in SMD 0402
J31	open	J31 can be used to route the FlexCAN signals of port CANB to the module connector. This jumper must only be closed if the transceiver circuit U12 is removed. Useful for optical isolation of CAN signals.
1 + 2		Connects CANTXB with CANHB pin at X2C18.
3 + 4		Connects CANRXB with CANLB pin at X2D18.
Package Type		0R in SMD 0402
J32	open	J32 connects the MPC5554 signals GPIO203 and GPIO204 to the FPGA signals /FPGA_SLEEP and /FPGA_PROG.
1 + 2		Connects MPC5554 GPIO203 to /FPGA_SLEEP.
3 + 4		Connects MPC5554 GPIO204 to /FPGA_PROG.
Package Type		0R in SMD 0402

Jumper	Default	Comment
J33, J34		J33 and J34 define the slave addresses (A2 and A1) of the serial memory U15 on the I^2C bus. In the high-nibble of the address, I^2C memory devices have the slave ID 0xA. The low-nibble consists of A2, A1, A0, and the R/W bit. A0 is tied to DGND. It must be noted that the RTC at U16 is also connected to the I^2C bus. The RTC has the address 0xA2/ 0xA3 which can not be changed.
1 + 2, 2 + 3		A2= 0, A1= 0, A0= 0 (0xA0 / 0xA1)
1 + 2, 1 + 2		A2= 1, A1= 0, A0= 0 (0xA8 / 0xA9)
2 + 3, 2 + 3		A2= 0, A1= 1, A0= 0 (0xA4 / 0xA5)
2 + 3, 1 + 2	X	A2= 1, A1= 1, A0=0 (0xAC / 0xAD) I^2C slave address 0xAC for write operations and 0xAD for read access.
Package Type		0R in SMD 0402
J35	open	J35 connects the JTAG port signals of the CPLD U19 to GPIO signals of the FPGA U21. This function may used to implement in-system programming of the CPLD.
1 + 2		Connects FPGA_CPLD_TCK to CPLD_TCK.
3 + 4		Connects FPGA_CPLD_TMS to CPLD_TMS.
5 + 6		Connects FPGA_CPLD_TDO to CPLD_TDO.
7 + 8		Connects FPGA_CPLD_TDI to CPLD_TDI.
Package Type		0R in SMD 0402
J36	open	J36 connects the FPGA signals FPGA_B3_IO[13..16]. This jumper can act as test point for these signals or to configure a bit pattern to the FPGA. Each FGPA signal has a 10 kOhm pull-up resistor. If the jumper is left open, a high level is read from the FPGA input. Do not drive these signals if they are connected to DGND!
1 + 2		Connects FPGA_B3_IO13 to DGND.
3 + 4		Connects FPGA_B3_IO14 to DGND
5 + 6		Connects FPGA_B3_IO15 to DGND
7 + 8		Connects FPGA_B3_IO16 to DGND
Package Type		0R in SMD 0402
J37	open	J37 connects pin 6 of the LAN configuration memory U18 to DGND or VDD3V3. This pins may have different function depending on the memory device installed. *Please refer to the corresponding memory data sheet for more detailed information.*
1 + 2		Connects pin 6 to VDD3V3.
2 + 3		Connects pin 6 to DGND.
Package Type		0R in SMD 0402

Jumper	Default	Comment
J38, J39	open	J38 and J39 connects pin 5 of the CAN Transceivers U11 and U12 to GND or VDDCAN. *Please refer to the corresponding CAN Transceiver data sheet for more detailed information.*
1 + 2		Connects pin 5 to DGND.
2 + 3		Connects pin 5 to VDDCAN.
Package Type		0R in SMD 0402
J40	1+2	J40 selects the supply voltage for the CAN Transceivers U11 and U12. *Please refer to the corresponding CAN Transceiver data sheet for more detailed information.*
1 + 2		Selects VDD3V3
2 + 3		Selects VDD5V
Package Type		0R in SMD 0805
J41, J42, J43, J44	open	J41 to J44 connect the Signals ETPUB10, ETPU13, ETPU20 and ETPU29 to VDD3V3. This is needed for the MPC5567 family member. The MPC5567 features at this pins power supply inputs.
1 + 2		Selects VDD3V3
Package Type		0R in SMD 0402

Table 3: Jumper Settings

4 Power Requirements

The phyCORE-MPC5554 must be supplied with two different supply voltages:

Supply voltage VDD3V3	**+3.3 V ± 5 % with 1A ****
Pins at Connector X2	**1C, 2C, 1D, 2D, 4D, 5D**
Supply voltage VDD5V	**+5 V ± 10 % with 100mA ****
Pins at Connector X2	**4C, 5C**

** without external loads

Caution:
Both supply voltages are required for proper operation of the phyCORE-MPC5554. The module must **never** be put into operation whit only one of the supply voltages connected to the device! This might render the module inoperable.

Connect all power input pins to your power supply and at least the matching number of DGND pins neighboring the power pins.

As a general design rule we recommend connecting all GND pins neighboring signals which are being used in the application circuitry to guarantee proper function and Electro Magnetic Conformity (EMC).

The load of the supplies depends on the external periphery attached to the phyCORE module.

Optional supply input VBAT	**+3V**
Pin at Connector X2	**6C**

VBAT is the input pin that supplies the internal power down voltage VPD. VBAT is connected over two Schottky diodes (D3 and D5) to VPD. VPD is also connected over a Schottky diode (D4) to VDD3V3. As long as VDD3V3 is applied, VPD will be fed through VDD3V3. Do not apply any voltage source to the VPD pin.

This is an output signal. VPD is used to supply the Real-Time Clock U16 and the serial memory device U15 if J8 is closed at position 2+3. VBAT should be supplied from a 3 V source.

On-board generated voltages: VDD1V5, VDDFPGA

- VDD1V5 MPC5554 core voltage
- VDDFPGA Lattice XP FPGA core voltage

4.1 Voltage Supervision and Reset

The input voltages VDD3V3 and VDD5V as well as the on-board generated operation voltages VDD1V5 and VDDFPGA are monitored by a voltage supervisor device at U24. This circuitry is responsible for generation of the system reset signal /RESET. The voltage supervisor IC initiates a reset cycle if any operating voltage drops below its minimum threshold value. After all voltages reach their required value, the supervisor chip adds an additional 200 ms delay until the /RESET line will be inactive (high). /RESET connects to the processor reset input.

/RESET is a bi-directional (open-collector) signal that can be connected to more then one source. For instance, /RESET is also connected to the JTAG/OnCE connector of the phyCORE module. /RESET has a 10kOhm pull-up resistor.

5 System Start-Up Configuration

The phyCORE-MPC5554 supports four different software start-up modes:

- Internal Flash Memory
- External Memory controlled by /CS0
- SCI UART
- FlexCAN

Internal/External Memory Boot

The decision which mode is used after /RESET goes from active to inactive state is defined by the external signal /RSTCFG (X2C9). The default state of this signal is high configured by an on-board pull-up resistor to VDD3V3.

Internal Flash	/RSTCFG driven high (or left unconnected)
External Memory	/RSTCFG driven low (connected to DGND)

/RSTCFG should be valid during /RESOUT is active (low). /RESOUT is driven from the MPC5554 and reflects the status of the system reset signal /RESET.

After completing a /RESET cycle the MPC5554 always starts its internal **B**oot **A**ssist **M**odule (BAM) software. This software reads the boot configuration (internal or external memory). The next action of the BAM is to probe the configured boot memory. It reads the first location of this memory. This code pattern is called **R**eset **C**onfiguration **H**alf **W**ord (RCHW). A valid RCHW consists of the boot ID 0x5A and a collection of control bits that specify a minimum MCU configuration. If a valid RCHW is not found, a CAN/SCI boot is initiated.

The RCHW consists of the following bits:

RCHW															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
reserved					WTE	PS0	BOOTID = 0x5A								

WTE Watchdog timer enable
0 disable
1 enable

PS0 Port size for external memory controlled by /CS0
0 32-bit (use this option for the external Flash)
1 16-bit

BOOTID Boot identifier
A valid boot identifier is 0x5A. If the MCU does not read the value 0x5A, a CAN/SCI boot is initiated.

Example RCHW = 0x005A
Watchdog disabled, 32-bit port size, Boot-ID 0x5A

Serial Boot Modes via FlexCAN and SCI UART

In the event that the BAM does not found a valid BOOTID the serial boot modes as well as the internal watchdog are activated. The baud rate for serial communication is determined by the system clock.

Crystal Frequency	**System Clock**	**SCI UART baud rate**	**FlexCAN baud rate**	**Watchdog Timeout**
f_{xtal}	$f_{sys} = 1.5 * f_{xtal}$	$f_{sys} / 1250$	$f_{sys} / 60$	$2.5 * 2^{27} / f_{sys}$
8 MHz	12 MHz	9600 bps	200 kBaud	67.1 sec

Table 4: Serial Boot Mode Baud Rate

Refer to the MPC5554 reference manual for a detailed description of the boot modes.

Clock Configuration

The default clock configuration is set to "Crystal reference". For this setting jumper J1 and J2 are pre-configured at the time of assembly.

Clock Configuration MPC5567

The MPC5567 has an additionally PLL configuration input – PLLCFG2. For PLL configurations which uses a 40MHz input quartz oscillator, PLLCFG2 must be connected over R122 to VDD3V3.
R122 pre-configured at the time of assembly

Refer to the MPC5567 reference manual for a detailed description of the boot mode.

6 System Memory

The system memory consist of internal MPC5554 Flash memory, external standard Flash memory, Synchronous Burst SRAM and a small non-volatile memory device:

- 2 MByte internal MPC5554 Flash (read while write functionality)
- 2 MByte to 8 MByte asynchronous standard Flash-EEPROM, 32-bit access
- 1 MByte to 16 MByte flow-through synchronous Burst SRAM, 32-bit access, 0 wait states, 2-1-1-1 burst mode
- I^2C Memory: 4 kByte EEPROM (up to 32 kByte, alternatively I^2C FRAM, I^2C SRAM)

The external Flash and sync. SRAM are connected to the MPC5554 32-bit data bus. The Flash is controlled by /CS0 for boot operation.

The Synchronous Burst SRAM is controlled by /CS1 and supports the special synchronous burst modes that enables maximum data transfer rates.

Communication with the small non-volatile memory device (EPROM, FRAM or SRAM) is established over the I^2C bus. This memory device can be used for storage of system parameters or configuration data.

6.1 External Standard Flash Memory (U3, U4)

The Flash memory devices used on the phyCORE-MPC5554 operate in 16-bit mode and are organized in 32-bit data bus with. The device at U3 connects to the low data bus while device U4 connects to the high data bus.

Type	Size per device	Manufacturer	Device Code	Manufacturer Code
29LV800T/B	1 MByte	AMD	22DA/225B	01
29LV160T/B	2 MByte	AMD	22C4/2249	01
29LV320T/B	4 MByte	AMD	22F6/22F9	01
29DL800T/B	1 MByte	AMD	224A/22CB	01

Table 5: Choice of Standard Flash Memory Devices and Manufacturers

The access speed depends on the MPC5554 processor frequency and the speed grade of populated flash devices. The speed grade varies due to production deviations. To provide for a worst case scenario take the value for the highest access time into consideration. With assuming of 132 MHz processor frequency and 66 MHz bus speed take the following wait state values:

120 ns access time	**9 wait states**
100 ns access time	**7 wait states**
90 ns access time	**7 wait states**
70 ns access time	**5 wait states**

The Flash memory bank is controlled by the periphery Chip Select signal /CS0.

The BR0 and OR0 register has to be initialized to

```
BR0 = FLASH_BASE | 0x00000003;// no burst and valid
OR0 = 0xff000050;        16 MByte space; five Wait
```

Use of Flash memory enables in-circuit programming of the module. The Flash devices on the phyCORE-MPC5554 are programmable at 3.3 VDC. Consequently, no dedicated programming voltage is required. As of the printing of this manual, Flash devices generally have a life expectancy of at least 100,000 erase/program cycles.

6.2 Synchronous Burst SRAM (U5, U6)

Use of synchronous Flow-Through Burst SRAM supports the fastest mode of the MPC5554 memory interface. The memory is organized in 32-bit width and consists of two banks. These banks appear to the processor as linear address spaces and do not require special activation. The memory is generally accessed via /CS1 without wait states.

The phyCORE-MPC5554 can be populated with memory devices of various capacities. Generally, each memory bank can only be populated with memory devices of a consistent size. Solder jumper J19 is used to configure the memory capacity and pre-installed at time of delivery.

Table 6 shows all of the possible memory configurations.

Capacity	Type	Device	J19
1 MByte	256k x 32/36-bit	U5	1+5
2 MByte	256k x 32/36-bit	U5-6	1+5
	512k x 32/36-bit	U5	2+5
4 MByte	512k x 32/36-bit	U5-6	2+5
	1M x 32/36-bit	U5	3+5
8 MByte	1M x 32/36-bit	U5-6	3+5
	2M x 32/36-bit	U5	4+5
16 MByte	2M x 32/36-bit	U5-6	4+5

Table 6: Memory Options for the Synchronous Burst SRAM

The SRAM is controlled by /CS1 with 32-bit bus width.
The BR1 and OR1 register has to be initialized to

```
BR1 = SRAM_BASE | 0x00000041;  // 4 word burst and valid
OR1 = 0xff000000;         // 16 MByte space; zero Wait
```


6.3 Serial Memory (U15)

The phyCORE-MPC5554 features a non-volatile memory device with a serial I^2C interface. This memory can be used for storage of configuration data or operating parameters, that must not be lost in the event of a power interruption. Depending on the module's configuration, this memory can be in the form of an EEPROM, FRAM or SRAM. The available capacity ranges from 512 Byte to 32 kByte or more.

If SRAM is used, solder jumper J8 must be closed at position 2+3 to supply the memory device via VPD.

Because the MPC5554 does not provide an on-chip I^2C interface, the protocol has to be generated by software or by implementing an I^2C bus master IP core in the FPGA U21. Such IP cores are available free of charge[1]. In the case of a software generated I^2C protocol, two GPIO's of the MPC5554 have to be connected externally to the SDA (X2D32) and SCL (X2C31) signals. You can also use the balls G4 (SDA) and E2 (SCL) of the FPGA U21H if they are configured for GPIO for software controlled I^2C access.

Table 7 gives an overview of the possible devices for use at U15 as of the printing of this manual.

Type	Size	I^2C Frequency	Address Pins	Write Cycles	Life of Data	Device	Manufacturer
EEPROM	256/512 Byte	400 kHz	A2, A1, A0	1 000 000	100 yrs.	CAT24WC02/04	CATALYST
	1/2 kByte	400 kHz	A2, A1, A0	1 000 000	100 yrs.	CAT24WC08/16	CATALYST
	4/8 kByte	400 kHz	A2, A1, A0	1 000 000	100 yrs.	CAT24WC32/64	CATALYST
	32 kByte	1 MHz	A1, A0	100 000	100 yrs.	CAT24WC256	CATALYST
FRAM	512 Byte	1 MHz	A2, A1	10 billion	10 yrs.	FM24C04	RAMTRON
	8 kByte	1 MHz	A2, A1, A0	10 billion	10 yrs.	FM24C64	RAMTRON
SRAM	256 Byte	100 kHz	A2, A1, A0	-	-	PCF8570	PHILIPS

Table 7: Serial Memory Options for U15

1: Please contact PHYTEC for more information.

It is important to note that the RTC is also connected to the I^2C bus. The RTC can operate with a bus frequency up to 400 kHz. Therefore the use of high bus frequencies for accessing the serial memory is not recommended. The RTC has the I^2C bus slave address 0xA2 / 0xA3. The slave address of the serial memory must be selected accordingly using the solder jumpers J33 (A1) and J34 (A2), so that no collision occurs. The address input A0 is hardwired to DGND.

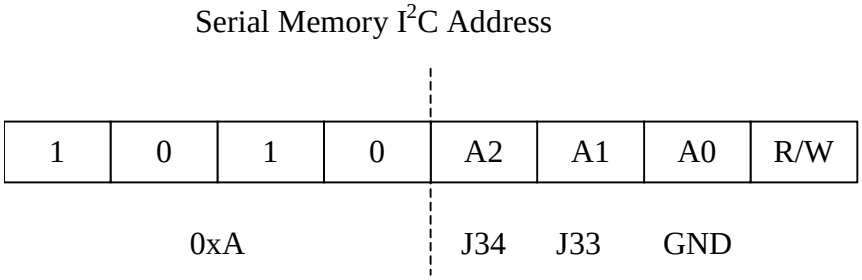

Figure 8: Serial Memory I^2C Slave Address

Possible configuration options are shown below:

I^2C Address	**J33 A1**	**J34 A2**
0xA0 / 0xA1	1 + 2	2 + 3
0xA4 / 0xA5	2 + 3	2 + 3
0xA8 / 0xA9	1 + 2	1 + 2
0xAC / 0xAD	2 + 3	1 + 2

Table 8: Serial Memory I^2C Address (Examples)

Address lines A1 and A2 are not always made available by certain serial memory types. This should be noted when configuring the I^2C bus slave address.

7 FPGA System Logic Device U21

The FPGA logic device U21, supplied by Lattice Semiconductor, is responsible for routing resources on the phyCORE-MPC5554 and provides a very flexibly way to connect and operate application-specific hardware components or interfaces in a target design. In general, the FPGA device is not part of the basic processor system as it is not needed to handle the Chip Select signal of the Flash memory or other basic functions. This allows reprogramming of the FPGA during runtime of the processor via the JTAG port. The FPGA JTAG port can be served by an external source (programming cable e.g.) or by the on-board PowerPC processor over general purpose I/O pins.

The FPGA is a member of the LatticeXP family provided by Lattice Semiconductor (http://www.latticesemi.com/).

- LatticeXP FPGA

LFXP6	6k logic elements
LFXP10	10k logic elements
LFXP15	15k logic elements
LFXP20	20k logic elements

Device Features:

- Reconfigurable SRAM-based logic combined with non-volatile Flash memory
- SRAM and non-volatile Flash memory programmable through JTAG port
- Supports background programming of Flash memory during runtime
- Embedded and distributed memory for dual-port SRAM, FIFO, Single SRAM, ROM etc.

- programmable I/O Buffer
  LVCMOS3.3/2.5/1.8/1.5/1.2
  LVTTL
  SSTL, HSTL
  PCI
  LVDS
- DDR memory interface support
- Two/four programmable PLL's; clock shifting capability

The FPGA is connected to the local processor bus with 32-bit bus width. The logic device acts as bridge for connecting external peripheral devices or interfaces to the PowerPC. A total of 84 I/O lines are available on the Molex connector X2 and can be used for application-specific features.

The following FPGA signals are available through the phyCORE-connector X2:

FPGA_B1_IO[25..0]	26 signals
FPGA_B4_IO[25..0]	26 signals
FPGA_B2_IO[19..0]	20 signals
FPGA_B3_IO[11..0]	12 signals
==========	==========
Number of user I/O	84 signals

7.1 FPGA Firmware Development

A basic firmware project with pin and signal assignment is provided by PHYTEC. This project is written in VHLD and can easily be extended with customer-specific functionality.

The required development tool is called ispLever and is provided by Lattice Semiconductor. The tool can be downloaded from www.latticesemi.com and is free in its basic version. This version is suitable to compile and create the programmable output file.

In-system programming of the FPGA through the MPC5554 is supported a JTAG engine project (ispVMEmbedded) available in C-source code provided by Lattice Semiconductor. This allows for reprogramming of the FPGA during runtime and requires connection of the FPGA JTAG port to four MPC5554 GPIO signals.

7.2 FPGA Basic Firmware

The basic firmware project implements a simple GPIO structure. The FPGA signals

FPGA_B7_IO[8..0]	9 signals
FPGA_B1_IO[25..0]	26 signals
FPGA_B4_IO[25..0]	26 signals
FPGA_B2_IO[20..0]	21 signals
FPGA_B3_IO[16..0]	17 signals

are programmable via a set of registers. To each pin correspondents a direction and a data bit. These bit are collected as following:

FPGA Signal	**FPGA Register**	**Address Offset**
FPGA_B7_IO[8..0] This are on-board signals and not available at the system connector.	FPGA_B7_IO_DATA[8..0] FPGA_B7_IO_DIR[8..0]	0x00 0x04
FPGA_B1_IO[25..0]	FPGA_B1_IO_DATA[25..0]	0x08

	FPGA_B1_IO_DIR[25..0]	0x12
FPGA_B4_IO[25..0]	FPGA_B4_IO_DATA[25..0] FPGA_B4_IO_DIR[25..0]	0x16 0x20
FPGA_B2_IO[20..0] FPGA_B2_IO[20] is a on-board signal and not available at the system connnector.	FPGA_B2_IO_DATA[20..0] FPGA_B2_IO_DIR[20..0]	0x24 0x28
FPGA_B3_IO[16..0] FPGA_B3_IO[16..12] is a on-board signal and not available at the system connnector.	FPGA_B3_IO_DATA[16..0] FPGA_B3_IO_DIR[16..0]	0x32 0x36

Table 9: Memory map FPGA register structure

The FPGA register structure is controlled by /CS3. The registers should be accessed in 32-bit width.

The BR3 and OR3 register has to be initialized to

```
BR3 = FPGA_BASE | 0x00000003;   // no burst and valid
OR3 = 0xff000020;          16 MByte space; two Wait
```

Reset default value of all registers is 0. A direction register bit of 0 means the corresponding pin is an input and vice versa. All FPGA pins have weak internal pull-up resistors. So if you read a raw input, you see a 1.

8 Serial Interfaces

8.1 RS-232 Interface

A dual-channel RS-232 transceiver is located on the phyCORE-MPC5554 at U10. This device adjusts the signal levels of the TXDA/RXDA and TXDB/RXDB lines (MPC5554 eSCI UART). The RS-232 interface enables connection of the module to a COM port on a host-PC or other peripheral devices. In this instance, the RXDA_RS232 or RXDB_RS232 line (X2D22/X2C21) of the transceiver is connected to the corresponding TXD line of the COM port; while the TXDA_RS232 or TXDB_RS232 line (X2D23/X2C23) is connected to the RXD line of the COM port. The ground circuitry of the phyCORE-MPC5554 must also be connected to the applicable ground pin on the COM port.

Furthermore it is possible to use the TTL signals of the eSCI UART channels externally. These signals are available at X2D16, X2D17 (RXDA, TXDA) and X2C19, X2C20 (RXDB, TXDB) on the phyCORE-connector. External connection of TTL signals is required for galvanic separation of the interface signals or for connection of different interface standards (RS485 etc.). Using the solder jumpers J21 and J22, the TTL transceiver outputs of the on-board RS-232 transceiver devices can be disconnected from the receive lines RXDA and RXDB. This is required so that the external transceiver does not drive signals against the on-board transceiver. The transmit lines TXDA / TXDB can be connected parallel to the transceiver input without causing any signal conflicts.

8.2 CAN Interface

Two CAN transceivers (SN65HV230) populate the phyCORE-MPC5554 module at U11 / U12.

The on-board transceivers enable transmission and receipt of CAN signals via CANTXA / CANRXA and CANTXB / CANRXB. The CAN transceivers support transmission speeds of up to 1 MBit/s and connection of up to 110 nodes on a single CAN network. Data transmission occurs with differential signals between CANH and CANL. A Ground connection between nodes on a CAN bus is not required, yet is recommended to better protect the network from electromagnetic interference (EMI). Additionally, the common mode voltage of both CAN transceivers must not exceed the specified threshold: -4 V / +16 V (recommended range –2 V to +7 V) for the SN65HV230. If the CAN bus system exceeds these limiting values galvanic isolation of the CAN signals is required. For larger CAN bus systems, an external de-coupler device should be implemented to optically isolate the CAN transceiver and the phyCORE-MPC5554.

To add external circuits for optical isolation, the CAN transceivers must be removed and the CAN bus signals bypassed by means of solder jumpers J30 and J31. Then the CAN TTL signals are routed to pins X2C18, X2D18 (CANTXB, CANRXB) and X2D21, X2D20 (CANTXA, CANRXA) of the phyCORE-connector.

For connection of the CANTx and CANRx lines to an external transceiver, we recommend using a Agilent HCPL06xx, Toshiba TLP113, Sharp PC410L0NIP or similar fast opto-coupler. Parameters for configuring a proper CAN bus system can be found in the DS102 norms from the CiA[1] (CAN in Automation) User and Manufacturer's Interest Group.

[1] CiA CAN in Automation -.Founded in March 1992, CiA provides technical, product and marketing information with the aim of fostering Controller Area Network's image and providing a path for future developments of the CAN protocol.

In order to ensure proper message transmission over the CAN bus, a 120 Ohm terminating resistor must be connected to each end of the CAN bus between the CANH and CANL signals.

Configuration of the On-Board Transceiver:

The transceivers at U11 and U12 can be switched to stand-by mode by populating jumpers J5 and J6 with a 0R resistor (position 2+3).

Furthermore, the signal rise time can be configured by closing both jumpers at 1+2 (leaving 2+3 open). This results in reduced interference from the CAN bus when using lower baud rates. *For additional information refer to the data sheet for the SN65HV230 CAN transceiver*.

8.3 JTAG/OnCE/Nexus Debug Interface

The MPC5554 offers an on-chip JTAG/OnCE/Nexus debug interface. This interface allows external debug access to the controller without requiring a service software or firmware, such as a Monitor program, running on the chip. This internal debug interface also contains hardware features supporting use with common cross development systems and debug environments, such as Metrowerks' CodeWarrior. For instance, the MPC5554 features internal breakpoint registers enabling debugging in Flash memory.

A reduced set of the on-chip JTAG/OnCE/Nexus interface extends from the MPC5554 to a 14-pin connector X3 (card edge) at which an external interface signal converter circuitry can be attached. Such signal converters enable connection of the MPC5554 to a host-PC for debugging purposes.

The footprint of X3 is designed for a 14-pin header with 2.0 mm pin spacing. The pin assignment is shown in *Figure 9*. Pin header X3 is not installed on the standard phyCORE-MPC5554 module.

Figure 9 shows the pin assignment for a 14-pin standard JTAG/OnCE interface connection.

phyCORE Pin X2	Signal	JTAG/OnCE Connector			Signal	phyCORE Pin X2
60C	MPC_TDI	**1**	**o o**	**2**	DGND	59D, 57C, 62C
60D	MPC_TDO	**3**	**o o**	**4**	DGND	59D, 57C, 62C
61C	MPC_TCK	**5**	**o o**	**6**	DGND	59D, 57C, 62C
-	NC	**7**	**o o**	**8**	NC	-
10C	/RESET	**9**	**o o**	**10**	MPC_TMS	63C
1C, 2C...	VDD3V3	**11**	**o o**	**12**	DGND	59D, 57C, 62C
63D	/RDY	**13**	**o o**	**14**	JCOMP	59C

Figure 9: 14-Pin JTAG/OnCE Connector (X3) and Corresponding Pins on the phyCORE-Connector (X2)

In order to connect a true Nexus port, an external 38-pin connector must be located on the customer application board. The PHYTEC phyCORE-MPC5554 Development Board (part number PCM-979) features such Nexus connector at X2 and can be used as an example.

9 LAN91C111 Ethernet Controller

Connection of the phyCORE-MPC5554 to the world wide web or a local network is possible if the optional LAN91C111 10/100 Mbit/s Ethernet controller populates the module at U20.

This section only describes the functional characteristics of the LAN91C111 as implemented on the phyCORE-MPC5554. *A detailed description of the Ethernet controller itself can be found in the corresponding datasheet for the "10/100 Non PCI Ethernet Single Chip MAC and PHY" from SMSC* (http://www.smsc.com/).

9.1 Addressing the Ethernet Controller

The Ethernet device LAN91C111 is controlled by the MPC5554 Chip Select signal /CS2. Prior to accessing the LAN device the Chip Select has to be initialized by the application software.

The address range for /CS2 should be configured to 16 MByte address range due to the address line A8 is used by the address decoder in the CPLD. LAN access is in the lower address range with A8=0 (first 8 MByte). In order to match the device's access speed 2 wait states are needed.

The BR2 and OR2 register has to be initialized to

```
BR2 = ETH_BASE | 0x00000003;     // no burst and valid
OR2 = 0xff000020;          16 MByte space; two Wait
```

9.2 Interrupt

The interrupt request output LAN_IRQ (U20, pin 29) of the Ethernet controller LAN91C111 connects to the MPC5554 interrupt input IRQ2 indirectly. The CPLD at U19 configures the signal routing according to the following logic equation:

IRQ2 = LAN_IRQ

The IRQ generation is high-active and level triggered driven by the LAN Chip. Take care of this for the interrupt service handling.

9.3 MAC Address

In a computer network such as a **L**ocal **A**rea **N**etwork (LAN), the **M**edia **A**ccess **C**ontrol (MAC) address is a ***unique*** node hardware number. For a connection to the Internet, a table is used to convert the assigned IP number to the hardware's MAC address.

In order to guarantee that the MAC address is unique, all addresses are managed in a central location. PHYTEC has acquired a pool of MAC addresses. The MAC address of the phyCORE-MPC5554 is located on the bar code sticker attached to the module. This number is a 12-position HEX value.

The MAC address has already been programmed into the Ethernet controller's EEPROM (U18), so that the MAC address is automatically loaded to the Ethernet controller following a reset (*refer to section 9.4*).

9.4 Ethernet EEPROM U18

The EEPROM U18 connected to the Ethernet controller can be used to store configuration data that are automatically loaded into the LAN91C111 following a hardware reset. The EEPROM can be programmed on-board via the Ethernet controller. *For detailed programming instructions please refer to the LAN91C111 data sheet*. The EEPROM is pre-programmed with the MAC address at time of delivery (*refer to section 9.3*).

9.5 10/100Base-T Interface

The phyCORE-MPC5554 has been designed for use in 10/100Base-T networks exclusively. The 10/100Base-T interface with its signals including two LED status signals extends to phyCORE-connector X2. In order to connect the module to an existing 10/100Base-T network only a minimal external transformer circuitry is required.

If you are using the applicable Development Board for the phyCORE-MPC5554 (part number PCM-979), the external circuitry mentioned above is already integrated on the board (*refer to section 11.2.1*).

10 Real-Time Clock RTC-8564 (U16)

For real-time or time-driven applications, the phyCORE-MPC5554 is equipped with an RTC-8564 Real-Time Clock at U16. This RTC device provides the following features:

Serial input/output bus (I^2C), address 0xA2
Power consumption
- Bus active (400 kHz): < 1 mA
- Bus inactive, CLKOUT inactive: < 1 µA

Clock function with four year calendar
Century bit for year 2000-compliance
Universal timer with alarm and overflow indication
24-hour format
Automatic word address incrementing
Programmable alarm, timer and interrupt functions

If the phyCORE-MPC5554 is equipped with a battery (VBAT), the Real-Time Clock runs independently of the board's power supply.

The Real-Time Clock is programmed via the I^2C bus (address 0xA2 / 0xA3). Because the MPC5554 does not provide an on-chip I^2C interface, the protocol has to be generated by software or by implementing an I^2C bus master IP core in the FPGA U21. Such IP cores are available free of charge. In the case of software generated I^2C protocol, two GPIO's of the MPC5554 have to be connected externally to the SDA (X2D32) and SCL (X2C31) signals. You can also use the balls G4 (SDA) and E2 (SCL) of the FPGA U21H if they are configured for GPIO for software controlled I^2C access (*refer also to section 6.3)*.

If the RTC interrupt should be used as a software interrupt via a corresponding interrupt input of the processor, the signal /IRTC must be connected externally with a processor interrupt input. *For more information on the features of the RTC-8564, refer to the corresponding Data Sheet.*

Note:
After connection of the supply voltage, or after a reset, the Real-Time Clock generates **no** interrupt. The RTC must first be initialized (*see RTC Data Sheet for more information*).

11 phyCORE Development Board PCM-979

PHYTEC Development Boards are fully equipped with all mechanical and electrical components necessary for the speedy and secure start-up and subsequent communication to and programming of applicable PHYTEC Single Board Computer (SBC) modules. Development Boards are designed for evaluation, testing and prototyping of PHYTEC Single Board Computers in laboratory environments prior to their use in customer designed applications.

11.1 Concept of the phyCORE Development Board PCM-979

The phyCORE Development Board PCM-979 provides a flexible development platform enabling quick and easy start-up and subsequent programming of the phyCORE-MPC5554 Single Board Computer module. The Development Board design allows easy connection of additional expansion boards featuring various functions that support fast and convenient prototyping and software evaluation.

The following sections contain specific information relevant to the operation of the phyCORE-MPC5554 mounted on the phyCORE Development Board PCM-979.

11.2 Development Board PCM-979 Overview

11.2.1 Connectors, Buttons, LED's

As shown in *Figure 10*, the following connectors, push buttons and LED's are available on the phyCORE Development Board PCM-979:

X1	phyCORE-connector enabling mounting of applicable phyCORE modules
X2	MPC5554 Nexus 38-pin Mictor connector
X3	MPC5554 JTAG/OnCE/Nexus 14-pin header
X4	FPGA JTAG 10-pin header
X5	socket for +5 Volt power supply connectivity
X6	shielding (PE) contact
X7	mating receptacle for expansion board connectivity
GND1	DGND connector (for connection of GND signal of measuring devices such as an oscilloscope)
L6	LAN port 10/100 Mbit/s Ethernet, RJ-45 socket
P1A	DB-9 plug (male) for FlexCAN A (bottom)
P1B	DB-9 plug (male) for FlexCAN B (top)
P2A	DB-9 socket (female) for RS-232 eSCI/UART A (bottom)
P2B	DB-9 socket (female) for RS-232 eSCI/UART B (top)
BAT1	receptacle for an optional battery
S1	IRQ push button
S2	Reset push button
D8	green power LED, monitors +5 V VDD-CAN
D9	green power LED, monitors +5 V VDD5V
D10	green power LED, monitors +3V3 VDD3V3
D6	red user LED, controlled by MPC5554 I/O line EMIOS0

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user‘s responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

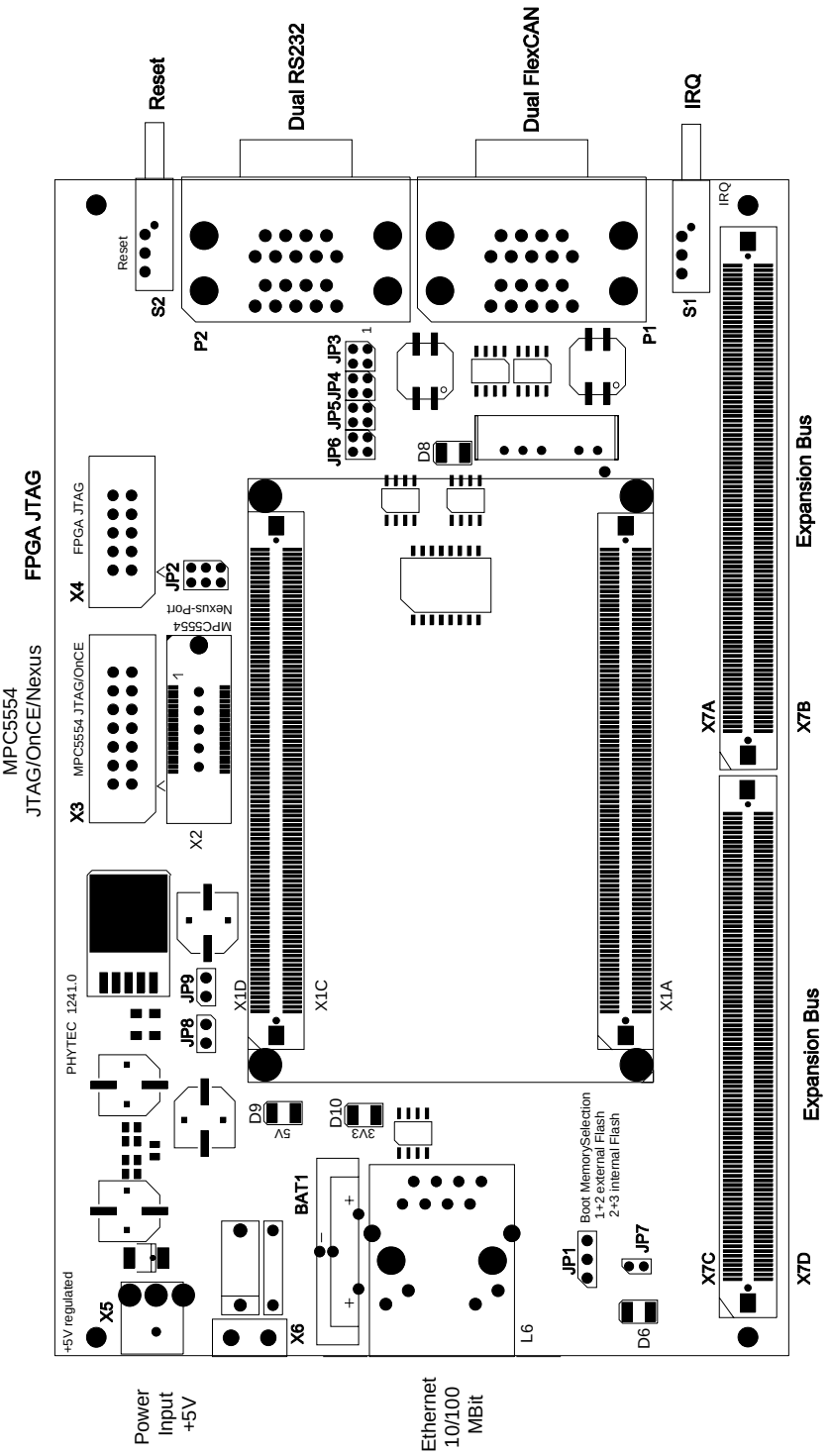

Figure 10: Location of Connectors, Buttons and LED's on the phyCORE Development Board PCM-979

11.2.2 Jumpers on the phyCORE Development Board PCM-979

Peripheral components of the phyCORE Development Board PCM-979 can be connected to the signals of the phyCORE-MPC5554 by setting the applicable jumpers.

The Development Board's peripheral components are configured for use with the phyCORE-MPC5554 by means of removable jumpers. If no jumpers are set, no signals are connected to the DB-9 connectors, the control and display units or the CAN transceivers. The Reset input on the phyCORE-MPC5554 directly connects to the Reset button (S2). *Figure 11* illustrates the numbering of the jumper pads, while *Figure 12* indicates the location of the jumpers on the Development Board.

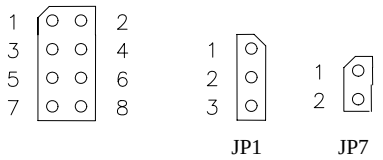

Figure 11: Numbering of Jumper Pads

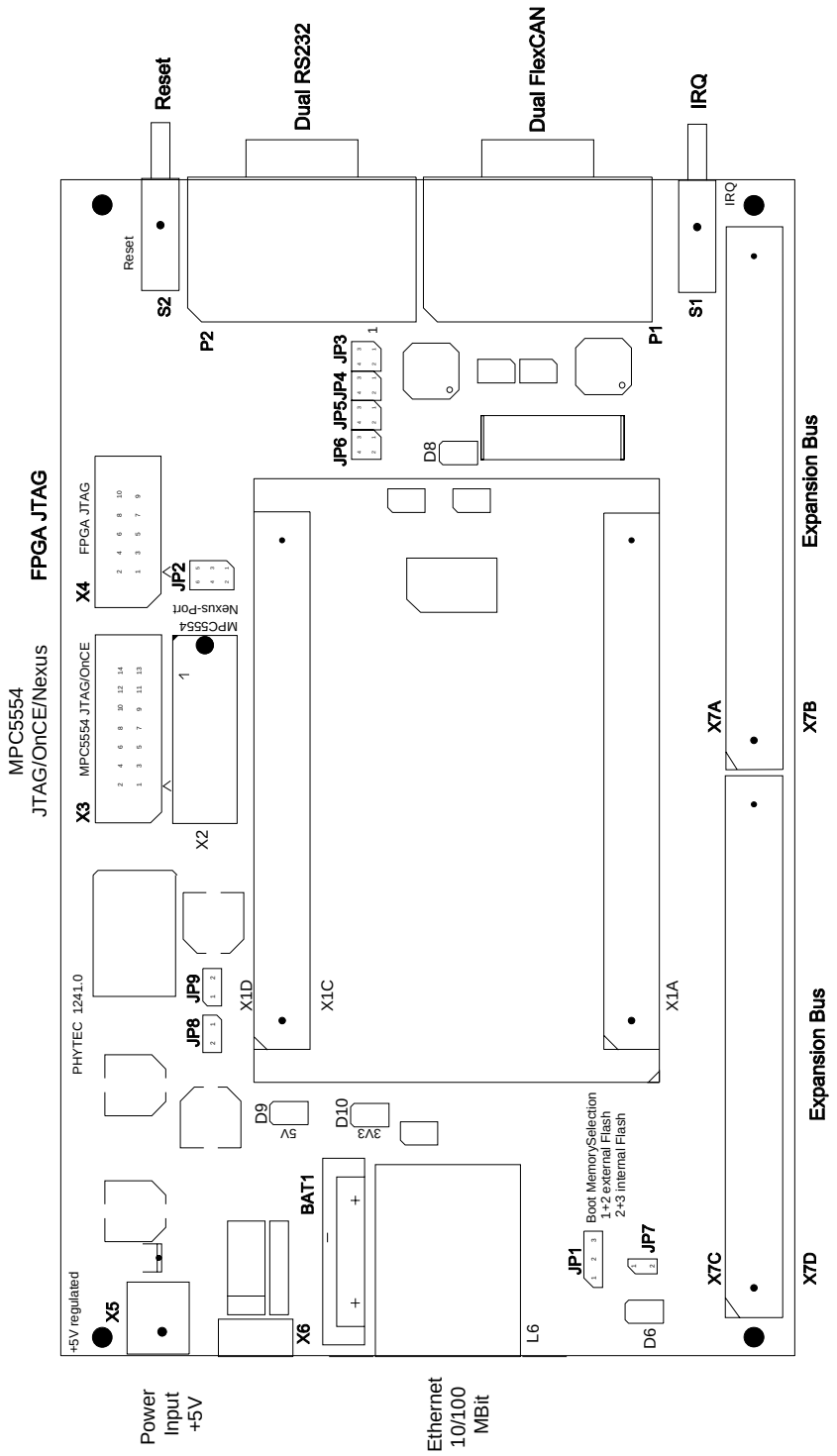

Figure 12: Location of the Jumpers (View of the Component Side)

Jumper	Default Setting	Description
JP1	2 + 3	Boot memory selection 1 + 2 external Flash memory U3/4 on phyCORE 2 + 3 internal MPC5554 Flash memory
JP2	*TBD*	*Jumper for compatibility between the different Nexus Probe vendors*
JP3-6	1 + 2	Isolation/non-isolation of the FlexCAN ports 1 + 3, 2 + 4 FlexCAN with optical isolation 1 + 2 FlexCAN w/o optical isolation
JP7	closed	Connects the user LED D6 to the MPC5554 EMIOS0 GPIO signal.
JP8	closed	Connects the +5V input supply voltage to the phyCORE-MPC5554 input voltage pins VDD5V.
JP9	closed	Connects the +3.3 V output voltage of the power regulator U7 to the phyCOREMPC-5554 input voltage pins VDD3V3.

Table 10: Development Board Jumper Overview

Caution
Do not operate the system with Jumpers JP8 or JP9 left open. This may damage the phyCORE module.

Figure 13 shows the factory default jumper settings for operation of the phyCORE Development Board PCM-979 with the standard phyCORE-MPC5554. Jumper settings for other functional configurations of the phyCORE-MPC5554 module mounted on the Development Board are described in *section 11.3*.

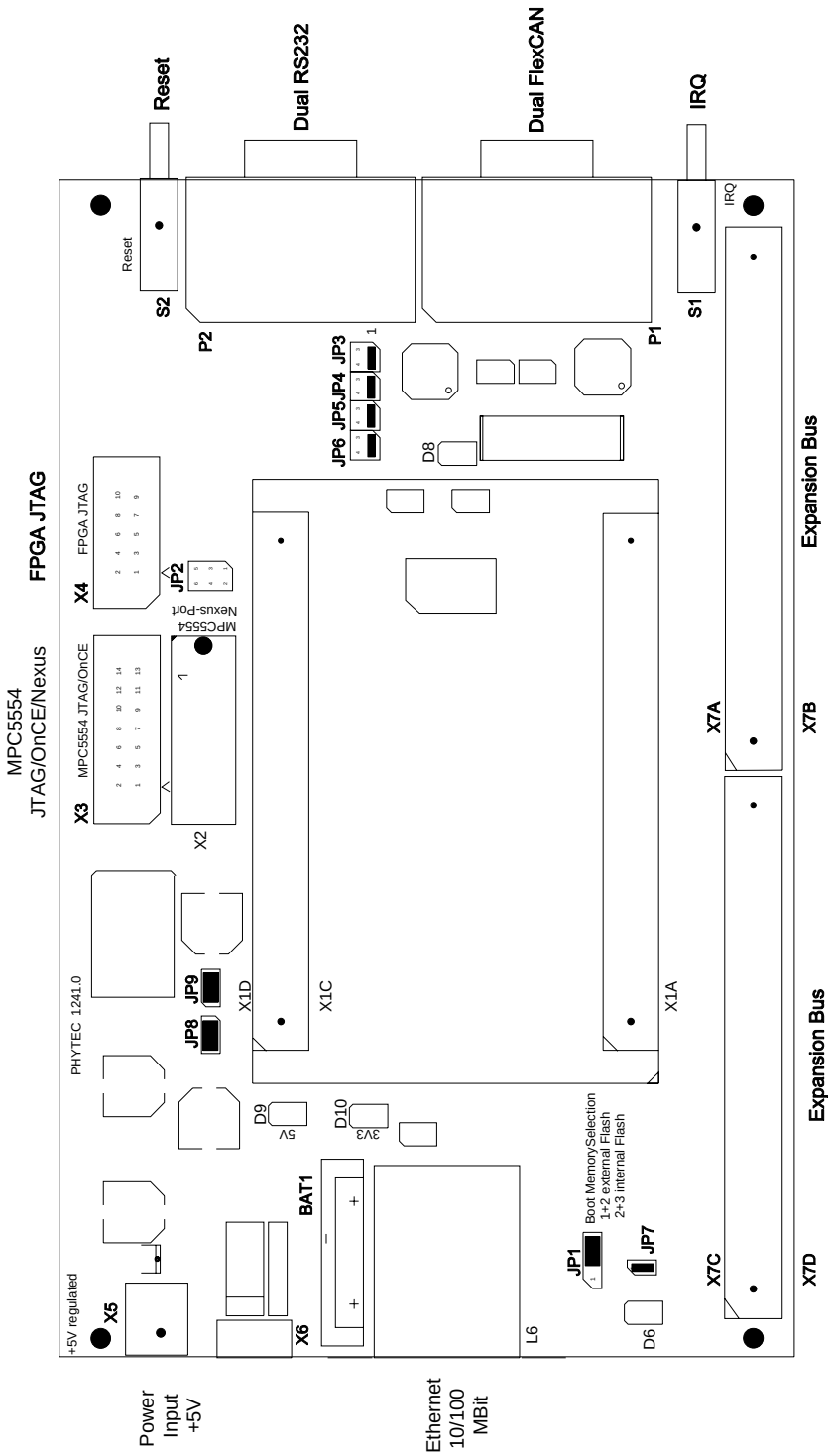

Figure 13: Default Jumper Settings of the phyCORE Development Board PCM-979 with phyCORE-MPC5554

11.3 Functional Components on the phyCORE Development Board PCM-979

This section describes the functional components of the phyCORE Development Board PCM-979 supported by the phyCORE-MPC5554 and appropriate jumper settings to activate these components. Depending on the specific configuration of the phyCORE-MPC5554 module, alternative jumper settings can be used. These jumper settings are different from the factory default settings as shown in *Figure 13* and enable alternative or additional functions on the phyCORE Development Board PCM-979 depending on user needs.

11.3.1 Power Supply at X5

Caution:
Do not change modules or jumper settings while the Development Board is supplied with power!

Permissible input voltage: +5 VDC regulated.

The required current load capacity of the power supply depends on the specific configuration of the phyCORE-MPC5554 mounted on the Development Board as well as whether an optional expansion board is connected to the Development Board. An adapter with a minimum supply of 1500 mA is recommended.

Jumper	Setting	Description
JP9	closed	Connects the +5 V input supply voltage to the phyCORE-MPC5554 input voltage pins VDD5V.
JP8	closed	Connects the +3.3 Voutput voltage of the power regulator U7 to the phyCORE-MPC5554 input voltage pins VDD3V3.

Table 11: JP8, JP9 Configuration of the Main Supply Voltages

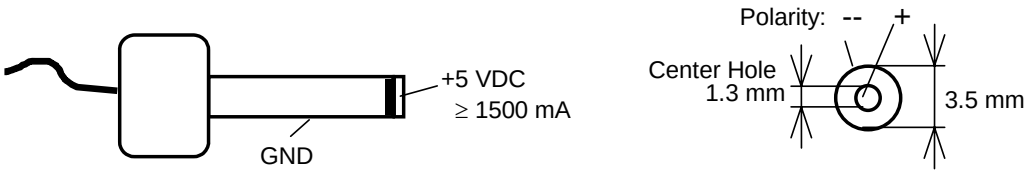

Figure 14: Connecting the Supply Voltage at X5

Caution:
Do not remove any of these jumpers and power the board. One missing main supply voltage can destroy the module!

11.3.2 First Serial Interface at Socket P2A

Socket P2A is the bottom socket of the double DB-9 connector at P2. The following description is based on a module configuration that utilizes the on-board RS-232 transceivers for the first serial interface.

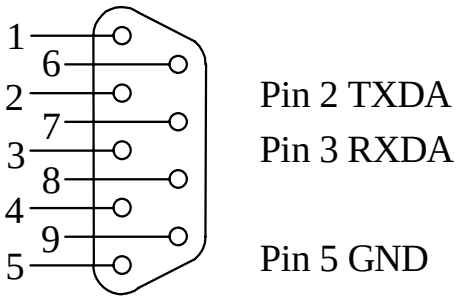

Figure 15: Pin Assignment of P2A as First RS-232 (Front View)

11.3.3 Second Serial Interface at Socket P2B

Socket P2B is the top socket of the double DB-9 connector at P2.

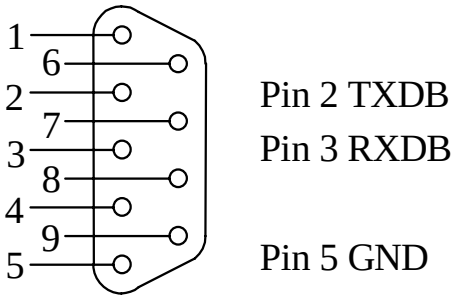

Figure 16: Pin Assignment of P2B as Second RS-232 (Front View)

11.3.4 First CAN Interface at Plug P1A

Plug P1A is the bottom plug of the double DB-9 connector at P1. P1A is connected to the first FlexCAN interface (FlexCAN A) of the phyCORE-MPC5554 via jumpers. Depending on the configuration of the CAN transceivers and their power supply, the following two configurations are possible:

1. CAN transceiver on the phyCORE- MPC5554 is populated and the CAN signals from the module extend directly to plug P1A.

Jumper	Setting	Description
JP3	1 + 2	Pin 7 of the DB-9 plug P1A is connected to CANHA from on-board transceiver on the phyCORE module
JP4	1 + 2	Pin 2 of the DB-9 plug P1A is connected to CANLA from on-board transceiver on the phyCORE module

Table 12: Jumper Configuration for CAN Plug P1A using the CAN Transceiver on the phyCORE- MPC5554

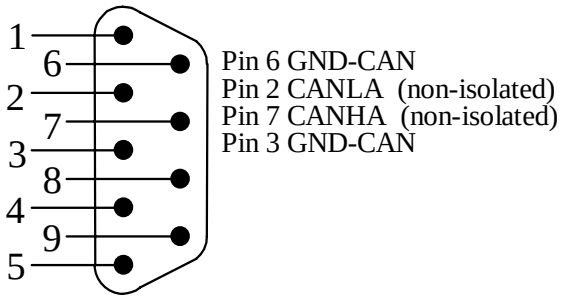

Figure 17: Pin Assignment of the DB-9 Plug P1A (CAN Transceiver on phyCORE- MPC5554, Front View)

2. The CAN transceiver on the phyCORE- MPC5554 is not populated and Jumper J30 on the module is closed at 1+2 and 3+4. CAN signals generated by the CAN transceiver (U2) on the Development Board extend to connector P1A **with galvanic separation.**

Jumper	Setting	Description
JP3	2 + 4	Pin 7 of the DB-9 plug P1A is connected to CANHA from on-board transceiver on the Development Board PCM-979.
	1 + 3[1]	Input at opto-coupler U1 on the phyCORE Development Board PCM-979 connected with CANHA (CAN_TX) of the phyCORE-MPC5554.
JP4	2 + 4	Pin 2 of the DB-9 plug P1A is connected to CANLA from on-board transceiver on the Development Board PCM-979.
	1 + 3[1]	Output at opto-coupler U1 on the phyCORE Development Board PCM-979 connected with CANLA (CAN_RX) of the phyCORE-MPC5554.

Table 13: Jumper Configuration for CAN Plug P1A Using Transceiver on the Development Board with Galvanic Separation

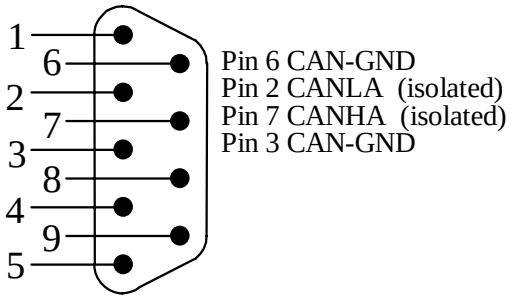

Figure 18: Pin Assignment of the DB-9 Plug P1A (CAN Transceiver on Development Board with Galvanic Separation)

[1]: Please make sure the CAN transceiver on the phyCORE-MPC5554 is not populated and Jumper J30 is closed at 1+2 and 3+4.

11.3.5 Second CAN Interface at Plug P1B

Plug P1B is the upper plug of the double DB-9 connector at P1. P1B is connected to the second FlexCAN interface (FlexCAN B) of the phyCORE-MPC5554 via jumpers. Depending on the configuration of the CAN transceivers and their power supply, the following three configurations are possible:

1. CAN transceiver populating the phyCORE-MPC5554 is populated and the CAN signals from the module extend directly to plug P1B.

Jumper	Setting	Description
JP5	1 + 2	Pin 7 of the DB-9 plug P1B is connected to CANHB from on-board transceiver on the phyCORE module
JP6	1 + 2	Pin 2 of the DB-9 plug P1B is connected to CANLB from on-board transceiver on the phyCORE module

Table 14: Jumper Configuration for CAN Plug P1B Using the CAN Transceiver on the phyCORE-MPC5554

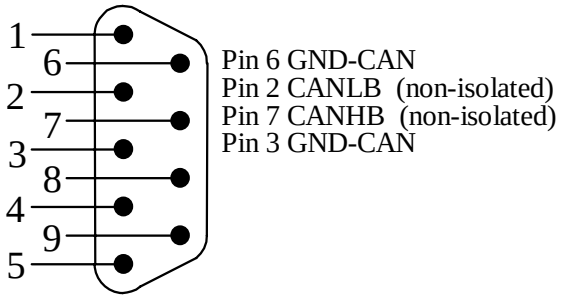

Figure 19: Pin Assignment of the DB-9 Plug P1B (CAN Transceiver on phyCORE-MPC5554, Front View)

2. The CAN transceiver on the phyCORE-MPC5554 is not populated and Jumper J31 on the module is closed at 1+2 and 3+4. CAN signals generated by the CAN transceiver (U3) on the Development Board extend to connector P1B **with galvanic separation.**

Jumper	Setting	Description
JP5	2 + 4	Pin 7 of the DB-9 plug P1B is connected to CANHB from on-board transceiver on the Development Board PCM-979.
	1 + 3[1]	Input at de-coupler U1 on the phyCORE Development Board PCM-979 connected with CANHB (CAN_TX) of the phyCORE-MPC5554.
JP6	2 + 4	Pin 2 of the DB-9 plug P1B is connected to CANLb from on-board transceiver on the Development Board PCM-979.
	1 + 3[1]	Output at de-coupler U1 on the phyCORE Development Board PCM-979 connected with CANLB (CAN_RX) of the phyCORE-MPC5554.

Table 15: Jumper Configuration for CAN Plug P1B using the CAN Transceiver on the Development Board PCM-979

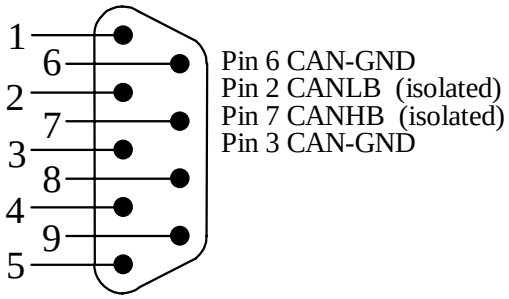

Figure 20: Pin Assignment of the DB-9 Plug P1B (CAN Transceiver on Development Board)

[1]: Please make sure the CAN transceiver on the phyCORE-MPC5554 is not populated and Jumper J31 is closed at 1+2 and 3+4.

11.3.6 Programmable LED D6

The phyCORE Development Board PCM-979 offers a programmable LED at D6 for user implementations. This LED can be connected to port pin EMIOS0 of the phyCORE-MPC5554 which is available with JP7 = closed. A low-level at port pin EMIOS0 causes the LED to illuminate, LED D6 remains off when writing a high-level to EMIOS0.

Jumper	Setting	Description
JP7	closed	Port pin EMIOS0 (GPIO0) of the MPC5554 controls LED D6 on the Development Board

Table 16: JP7 Configuration of the Programmable LED D6

11.3.7 Pin Assignment Summary of the phyCORE, the Expansion Bus and the Patch Field

As described in *section 11.1*, most signals from the phyCORE-MPC5554 extend to the expansion bus connector X7 on the Development Board. These signals, in turn, are routed in a similar manner to the patch field on an optional expansion board that mounts to the Development Board at X7.

A two dimensional numbering matrix similar to the one used for the pin layout of the phyCORE-connector is provided to identify signals on the expansion bus connector (X7 on the Development Board) as well as the patch field.

However, the numbering scheme for expansion bus connector and patch field matrices differs from that of the phyCORE-connector, as shown in the following two figures:

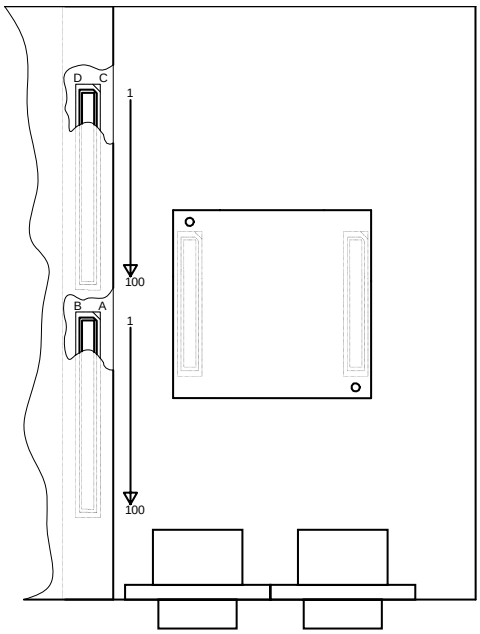

Figure 21: Pin Assignment Scheme of the Expansion Bus

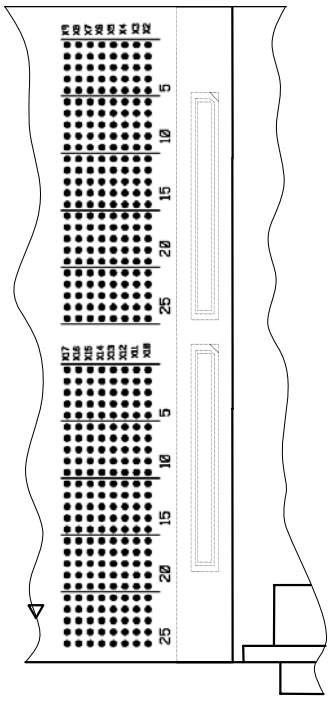

Figure 22: Pin Assignment Scheme of the Patch Field

The pin assignment on the phyCORE-MPC5554, in conjunction with the expansion bus (X7) on the Development Board and the patch field on an expansion board, is as follows:

11.3.7.1 Pin Assignment for phyCORE-MPC5554

phyCORE-MPC5554		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
1A	EXTCLK	EXTCLK	1A	BUS0	X10-1
3A	IRQ4	IRQ4	3A	BUS4	X14-1
4A	IRQ5	IRQ5	4A	BUS5	X15-1
5A	FPGA_B1_IO0	FPGA_B1_IO0	5A	BUS6	X16-1
6A	FPGA_B1_IO1	FPGA_B1_IO1	6A	BUS7	X17-1
8A	FPGA_B1_IO6	FPGA_B1_IO6	8A	BUS12	X14-2
9A	FPGA_B1_IO7	FPGA_B1_IO7	9A	BUS13	X15-2
10A	FPGA_B1_IO8	FPGA_B1_IO8	10A	BUS14	X16-2
11A	FPGA_B1_IO9	FPGA_B1_IO9	11A	BUS15	X17-2
13A	FPGA_B1_IO14	FPGA_B1_IO14	13A	BUS20	X14-4
14A	FPGA_B1_IO15	FPGA_B1_IO15	14A	BUS21	X15-4
15A	FPGA_B1_IO16	FPGA_B1_IO16	15A	BUS22	X16-4
16A	FPGA_B1_IO17	FPGA_B1_IO17	16A	BUS23	X17-4
18A	FPGA_B1_IO22	FPGA_B1_IO22	18A	BUS28	X14-5
19A	FPGA_B1_IO23	FPGA_B1_IO23	19A	BUS29	X15-5
20A	FPGA_B1_IO24	FPGA_B1_IO24	20A	BUS30	X16-5
21A	FPGA_B1_IO25	FPGA_B1_IO25	21A	BUS31	X17-5
23A	FPGA_B4_IO4	FPGA_B4_IO4	23A	BUS36	X14-6
24A	FPGA_B4_IO5	FPGA_B4_IO5	24A	BUS37	X15-6
25A	FPGA_B4_IO6	FPGA_B4_IO6	25A	BUS38	X16-6
26A	FPGA_B4_IO7	FPGA_B4_IO7	26A	BUS39	X17-6
28A	FPGA_B4_IO12	FPGA_B4_IO12	28A	BUS44	X14-7
29A	FPGA_B4_IO13	FPGA_B4_IO13	29A	BUS45	X15-7
30A	FPGA_B4_IO14	FPGA_B4_IO14	30A	BUS46	X16-7
31A	FPGA_B4_IO15	FPGA_B4_IO15	31A	BUS47	X17-7
33A	FPGA_B4_IO20	FPGA_B4_IO20	33A	BUS52	X14-9
34A	FPGA_B4_IO21	FPGA_B4_IO21	34A	BUS53	X15-9
35A	FPGA_B4_IO22	FPGA_B4_IO22	35A	BUS54	X16-9
36A	FPGA_B4_IO23	FPGA_B4_IO23	36A	BUS55	X17-9
38A	FPGA_B2_IO0	FPGA_B2_IO0	38A	BUS60	X14-10
39A	FPGA_B2_IO1	FPGA_B2_IO1	39A	BUS61	X15-10
40A	FPGA_B2_IO2	FPGA_B2_IO2	40A	BUS62	X16-10
41A	FPGA_B2_IO3	FPGA_B2_IO3	41A	BUS63	X17-10
43A	FPGA_B2_IO8	FPGA_B2_IO8	43A	BUS68	X14-11
44A	FPGA_B2_IO9	FPGA_B2_IO9	44A	BUS69	X15-11
45A	FPGA_B2_IO10	FPGA_B2_IO10	45A	BUS70	X16-11
46A	FPGA_B2_IO11	FPGA_B2_IO11	46A	BUS71	X17-11
48A	FPGA_B2_IO16	FPGA_B2_IO16	48A	BUS76	X14-12
49A	FPGA_B2_IO17	FPGA_B2_IO17	49A	BUS77	X15-12
50A	FPGA_B2_IO18	FPGA_B2_IO18	50A	BUS78	X16-12
51A	FPGA_B2_IO19	FPGA_B2_IO19	51A	BUS79	X17-12

phyCORE-MPC5554		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
53A	FPGA_B3_IO4	FPGA_B3_IO4	53A	BUS84	X14-14
54A	FPGA_B3_IO5	FPGA_B3_IO5	54A	BUS85	X15-14
55A	FPGA_B3_IO6	FPGA_B3_IO6	55A	BUS86	X16-14
56A	FPGA_B3_IO7	FPGA_B3_IO7	56A	BUS87	X17-14
58A	FPGA_VDDIO_B2	FPGA_VDDIO_B2	58A	BUS92	X14-15
59A	FPGA_VDDIO_B3	FPGA_VDDIO_B3	59A	BUS93	X15-15
60A	ETPUB30	ETPUB30	60A	BUS94	X16-15
61A	TCRCLKB	TCRCLKB	61A	BUS95	X17-15
63A	ETPUB28	ETPUB28	63A	BUS100	X14-16
64A	ETPUB26	ETPUB26	64A	BUS101	X15-16
65A	ETPUB24	ETPUB24	65A	BUS102	X16-16
66A	ETPUB22	ETPUB22	66A	BUS103	X17-16
68A	ETPUB20	ETPUB20	68A	BUS108	X14-17
69A	ETPUB18	ETPUB18	69A	BUS109	X15-17
70A	ETPUB16	ETPUB16	70A	BUS110	X16-17
71A	ETPUB14	ETPUB14	71A	BUS111	X17-17
73A	ETPUB12	ETPUB12	73A	BUS116	X14-19
74A	ETPUB10	ETPUB10	74A	BUS117	X15-19
75A	ETPUB8	ETPUB8	75A	BUS118	X16-19
76A	ETPUB6	ETPUB6	76A	BUS119	X17-19
78A	ETPUB4	ETPUB4	78A	BUS124	X14-20
79A	ETPUB2	ETPUB2	79A	BUS125	X15-20
80A	ETPUB0	ETPUB0	80A	BUS126	X16-20
81A	ETPUA30	ETPUA30	81A	BUS127	X17-20
83A	ETPUA28	ETPUA28	83A	BUS132	X14-21
84A	ETPUA26	ETPUA26	84A	BUS133	X15-21
85A	ETPUA24	ETPUA24	85A	BUS134	X16-21
86A	ETPUA22	ETPUA22	86A	BUS135	X17-21
88A	ETPUA20	ETPUA20	88A	BUS140	X14-22
89A	ETPUA18	ETPUA18	89A	BUS141	X15-22
90A	ETPUA16	ETPUA16	90A	BUS142	X16-22
91A	ETPUA14	ETPUA14	91A	BUS143	X17-22
93A	ETPUA12	ETPUA12	93A	BUS148	X14-24
94A	ETPUA10	ETPUA10	94A	BUS149	X15-24
95A	ETPUA8	ETPUA8	95A	BUS150	X16-24
96A	ETPUA6	ETPUA6	96A	BUS151	X17-24
98A	ETPUA4	ETPUA4	98A	BUS156	X14-25
99A	ETPUA2	ETPUA2	99A	BUS157	X15-25
100A	ETPUA0	ETPUA0	100A	BUS158	X16-25
1B	CLKOUT	CLKOUT	1B	BUS1	X11-1
2B	IRQ2	IRQ2	2B	BUS2	X12-1
3B	IRQ3	IRQ3	3B	BUS3	X13-1
5B	FPGA_B1_IO2	FPGA_B1_IO2	5B	BUS8	X10-2
6B	FPGA_B1_IO3	FPGA_B1_IO3	6B	BUS9	X11-2
7B	FPGA_B1_IO4	FPGA_B1_IO4	7B	BUS10	X12-2
8B	FPGA_B1_IO5	FPGA_B1_IO5	8B	BUS11	X13-2
10B	FPGA_B1_IO10	FPGA_B1_IO10	10B	BUS16	X10-4
11B	FPGA_B1_IO11	FPGA_B1_IO11	11B	BUS17	X11-4

phyCORE-MPC5554		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
12B	FPGA_B1_IO12	FPGA_B1_IO12	12B	BUS18	X12-4
13B	FPGA_B1_IO13	FPGA_B1_IO13	13B	BUS19	X13-4
15B	FPGA_B1_IO18	FPGA_B1_IO18	15B	BUS24	X10-5
16B	FPGA_B1_IO19	FPGA_B1_IO19	16B	BUS25	X11-5
17B	FPGA_B1_IO20	FPGA_B1_IO20	17B	BUS26	X12-5
18B	FPGA_B1_IO21	FPGA_B1_IO21	18B	BUS27	X13-5
20B	FPGA_B4_IO0	FPGA_B4_IO0	20B	BUS32	X10-6
21B	FPGA_B4_IO1	FPGA_B4_IO1	21B	BUS33	X11-6
22B	FPGA_B4_IO2	FPGA_B4_IO2	22B	BUS34	X12-6
23B	FPGA_B4_IO3	FPGA_B4_IO3	23B	BUS35	X13-6
25B	FPGA_B4_IO8	FPGA_B4_IO8	25B	BUS40	X10-7
26B	FPGA_B4_IO9	FPGA_B4_IO9	26B	BUS41	X11-7
27B	FPGA_B4_IO10	FPGA_B4_IO10	27B	BUS42	X12-7
28B	FPGA_B4_IO11	FPGA_B4_IO11	28B	BUS43	X13-7
30B	FPGA_B4_IO16	FPGA_B4_IO16	30B	BUS48	X10-9
31B	FPGA_B4_IO17	FPGA_B4_IO17	31B	BUS49	X11-9
32B	FPGA_B4_IO18	FPGA_B4_IO18	32B	BUS50	X12-9
33B	FPGA_B4_IO19	FPGA_B4_IO19	33B	BUS51	X13-9
35B	FPGA_B4_IO24	FPGA_B4_IO24	35B	BUS56	X10-10
36B	FPGA_B4_IO25	FPGA_B4_IO25	36B	BUS57	X11-10
37B	FPGA_VDDIO_B1	FPGA_VDDIO_B1	37B	BUS58	X12-10
38B	FPGA_VDDIO_B4	FPGA_VDDIO_B4	38B	BUS59	X13-10
40B	FPGA_B2_IO4	FPGA_B2_IO4	40B	BUS64	X10-11
41B	FPGA_B2_IO5	FPGA_B2_IO5	41B	BUS65	X11-11
42B	FPGA_B2_IO6	FPGA_B2_IO6	42B	BUS66	X12-11
43B	FPGA_B2_IO7	FPGA_B2_IO7	43B	BUS67	X13-11
45B	FPGA_B2_IO12	FPGA_B2_IO12	45B	BUS72	X10-12
46B	FPGA_B2_IO13	FPGA_B2_IO13	46B	BUS73	X11-12
47B	FPGA_B2_IO14	FPGA_B2_IO14	47B	BUS74	X12-12
48B	FPGA_B2_IO15	FPGA_B2_IO15	48B	BUS75	X13-12
50B	FPGA_B3_IO0	FPGA_B3_IO0	50B	BUS80	X10-14
51B	FPGA_B3_IO1	FPGA_B3_IO1	51B	BUS81	X11-14
52B	FPGA_B3_IO2	FPGA_B3_IO2	52B	BUS82	X12-14
53B	FPGA_B3_IO3	FPGA_B3_IO3	53B	BUS83	X13-14
55B	FPGA_B3_IO8	FPGA_B3_IO8	55B	BUS88	X10-15
56B	FPGA_B3_IO9	FPGA_B3_IO9	56B	BUS89	X11-15
57B	FPGA_B3_IO10	FPGA_B3_IO10	57B	BUS90	X12-15
58B	FPGA_B3_IO11	FPGA_B3_IO11	58B	BUS91	X13-15
60B	ETPUB31	ETPUB31	60B	BUS96	X10-16
61B	ETPUB29	ETPUB29	61B	BUS97	X11-16
62B	ETPUB27	ETPUB27	62B	BUS98	X12-16
63B	ETPUB25	ETPUB25	63B	BUS99	X13-16
65B	ETPUB23	ETPUB23	65B	BUS104	X10-17
66B	ETPUB21	ETPUB21	66B	BUS105	X11-17
67B	ETPUB19	ETPUB19	67B	BUS106	X12-17
68B	ETPUB17	ETPUB17	68B	BUS107	X13-17
70B	ETPUB15	ETPUB15	70B	BUS112	X10-19
71B	ETPUB13	ETPUB13	71B	BUS113	X11-19
72B	ETPUB11	ETPUB11	72B	BUS114	X12-19

phyCORE-MPC5554		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
73B	ETPUB9	ETPUB9	73B	BUS115	X13-19
75B	ETPUB7	ETPUB7	75B	BUS120	X10-20
76B	ETPUB5	ETPUB5	76B	BUS121	X11-20
77B	ETPUB3	ETPUB3	77B	BUS122	X12-20
78B	TCRCLKA	TCRCLKA	78B	BUS123	X13-20
80B	ETPUB1	ETPUB1	80B	BUS128	X10-21
81B	ETPUA31	ETPUA31	81B	BUS129	X11-21
82B	ETPUA29	ETPUA29	82B	BUS130	X12-21
83B	ETPUA27	ETPUA27	83B	BUS131	X13-21
85B	ETPUA25	ETPUA25	85B	BUS136	X10-22
86B	ETPUA23	ETPUA23	86B	BUS137	X11-22
87B	ETPUA21	ETPUA21	87B	BUS138	X12-22
88B	ETPUA19	ETPUA19	88B	BUS139	X13-22
90B	ETPUA17	ETPUA17	90B	BUS144	X10-24
91B	ETPUA15	ETPUA15	91B	BUS145	X11-24
92B	ETPUA13	ETPUA13	92B	BUS146	X12-24
93B	ETPUA11	ETPUA11	93B	BUS147	X13-24
95B	ETPUA9	ETPUA9	95B	BUS152	X10-25
96B	ETPUA7	ETPUA7	96B	BUS153	X11-25
97B	ETPUA5	ETPUA5	97B	BUS154	X12-25
98B	ETPUA3	ETPUA3	98B	BUS155	X13-25
100B	ETPUA1	ETPUA1	100B	BUS159	X17-25
6C	VBAT	VBAT	6C	VBAT	X6-1
8C	PWRGOOD	PWRGOOD	8C	PFO	X8-1
9C	/RSTCFG	/RSTCFG	9C	BOOT	X8-2
10C	/RESET	/RESET	10C	RESET	X9-1
11C	/RSTOUT	/RSTOUT	11C	RESOUT	X9-2
13C	EMIOS1	EMIOS1	13C	GPIO2	X5-4
14C	EMIOS3	EMIOS3	14C	GPIO4	X7-4
15C	EMIOS5	EMIOS5	15C	GPIO5	X8-4
16C	EMIOS7	EMIOS7	16C	GPIO7	X2-5
18C	CANHB	CANHB	18C	GPIO10	X5-5
19C	RXDB	RXDB	19C	GPIO12	X7-5
20C	TXDB	TXDB	20C	GPIO13	X8-5
21C	RXDB_RS232	RXDB_RS232	21C	GPIO15	X2-6
23C	TXDB_RS232	TXDB_RS232	23C	GPIO18	X5-6
24C	CNRXC	CNRXC	24C	GPIO20	X7-6
25C	CNTXC	CNTXC	25C	GPIO21	X8-6
26C	EMIOS9	EMIOS9	26C	GPIO23	X2-7
28C	EMIOS11	EMIOS11	28C	GPIO26	X5-7
29C	EMIOS13	EMIOS13	29C	GPIO28	X7-7
30C	EMIOS15	EMIOS15	30C	GPIO29	X8-7
31C	SCL	SCL	31C	GPIO31	X2-9
33C	LAN_LEDA	LAN_LEDA	33C	GPIO34	X5-9
34C	LAN_LEDB	LAN_LEDB	34C	GPIO36	X7-9
35C	LAN_TPI-	LAN_TPI-	35C	GPIO37	X8-9
36C	LAN_TPO-	LAN_TPO-	36C	GPIO39	X2-10
38C	EMIOS17	EMIOS17	38C	GPIO42	X5-10

phyCORE-MPC5554		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
39C	EMIOS19	EMIOS19	39C	GPIO44	X7-10
40C	EMIOS21	EMIOS21	40C	GPIO45	X8-10
41C	EMIOS23	EMIOS23	41C	GPIO47	X2-11
43C	GPIO204	GPIO204	43C	GPIO50	X5-11
44C	GPIO206	GPIO206	44C	GPIO52	X7-11
45C	SINA	SINA	45C	GPIO53	X8-11
46C	SOUTA	SOUTA	46C	GPIO55	X2-12
48C	PSCA1	PSCA1	48C	GPIO58	X5-12
49C	PSCA3	PSCA3	49C	GPIO60	X7-12
50C	PSCA5	PSCA5	50C	GPIO61	X8-12
51C	SINB	SINB	51C	GPIO63	X2-14
53C	SOUTB	SOUTB	53C	GPIO66	X5-14
54C	PCSB1	PCSB1	54C	GPIO68	X7-14
55C	PCSB3	PCSB3	55C	GPIO69	X8-14
56C	PCSB5	PCSB5	56C	GPIO71	X2-15
58C	/TEST	/TEST	58C	GPIO74	X5-15
59C	JCOPM	JCOPM	59C	GPIO76	X7-15
60C	MPC_TDI	MPC_TDI	60C	GPIO77	X8-15
61C	MPC_TCK	MPC_TCK	61C	GPIO79	X2-16
63C	MPC_TMS	MPC_TMS	63C	GPIO82	X5-16
64C	/MSEO0	/MSEO0	64C	GPIO84	X7-16
65C	/MSEO1	/MSEO1	65C	GPIO85	X8-16
66C	MDO0	MDO0	66C	GPIO87	X2-17
68C	MDO2	MDO2	68C	GPIO90	X5-17
69C	MDO4	MDO4	69C	GPIO92	X7-17
70C	MDO6	MDO6	70C	GPIO93	X8-17
71C	MDO8	MDO8	71C	GPIO95	X2-19
73C	DAC0	DAC0	73C	GPIO98	X5-19
74C	ETRIG1	ETRIG1	74C	GPIO100	X7-19
75C	ETRIG0	ETRIG0	75C	GPIO101	X8-19
76C	AN38	AN38	76C	GPIO103	X2-20
78C	AN36	AN36	78C	GPIO106	X5-20
79C	AN34	AN34	79C	GPIO108	X7-20
80C	AN32	AN32	80C	GPIO109	X8-20
81C	AN30	AN30	81C	GPIO111	X2-21
83C	AN28	AN28	83C	GPIO114	X5-21
84C	AN26	AN26	84C	GPIO116	X7-21
85C	AN24	AN24	85C	GPIO117	X8-21
86C	AN22	AN22	86C	GPIO119	X2-22
88C	AN20	AN20	88C	GPIO122	X5-22
89C	AN18	AN18	89C	GPIO124	X7-22
90C	AN16	AN16	90C	GPIO125	X8-22
91C	AN14	AN14	91C	GPIO127	X2-24
93C	AN12	AN12	93C	GPIO130	X5-24
94C	AN10	AN10	94C	GPIO132	X7-24
95C	AN8	AN8	95C	GPIO133	X8-24
96C	AN6	AN6	96C	GPIO135	X2-25
98C	AN4	AN4	98C	GPIO138	X5-25
99C	AN2	AN2	99C	GPIO140	X7-25

phyCORE-MPC5554		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
100C	AN0	AN0	100C	GPIO141	X8-25
6D	VPD	VPD	6D	*VPD	X6-2
7D	/WDO	/WDO	7D	PFI	X7-1
8D	WDI	WDI	8D	WDI	X7-2
10D	X_10D	X_10D	10D	RESIN	X2-4
11D	EMIOS0	EMIOS0	11D	GPIO0	X3-4
12D	EMIOS2	EMIOS2	12D	GPIO1	X4-4
13D	EMIOS4	EMIOS4	13D	GPIO3	X6-4
15D	EMIOS6	EMIOS6	15D	GPIO6	X9-4
16D	RXDA	RXDA	16D	GPIO8	X3-5
17D	TXDA	TXDA	17D	GPIO9	X4-5
18D	CANLB	CANLB	18D	GPIO11	X6-5
20D	CANLA	CANLA	20D	GPIO14	X9-5
21D	CANHA	CANHA	21D	GPIO16	X3-6
22D	RXDA_RS232	RXDA_RS232	22D	GPIO17	X4-6
23D	TXDA_RS232	TXDA_RS232	23D	GPIO19	X6-6
25D	EMIOS8	EMIOS8	25D	GPIO22	X9-6
26D	EMIOS10	EMIOS10	26D	GPIO24	X3-7
27D	EMIOS12	EMIOS12	27D	GPIO25	X4-7
28D	EMIOS14	EMIOS14	28D	GPIO27	X6-7
30D	EMIOS16	EMIOS16	30D	GPIO30	X9-7
31D	EMIOS18	EMIOS18	31D	GPIO32	X3-9
32D	SDA	SDA	32D	GPIO33	X4-9
33D	/RTC_IRQ	/RTC_IRQ	33D	GPIO35	X6-9
35D	LAN_TPI+	LAN_TPI+	35D	GPIO38	X9-9
36D	LAN_TPO+	LAN_TPO+	36D	GPIO40	X3-10
37D	DQ1WIRE	DQ1WIRE	37D	GPIO41	X4-10
38D	EMIOS20	EMIOS20	38D	GPIO43	X6-10
40D	EMIOS22	EMIOS22	40D	GPIO46	X9-10
41D	GPIO203	GPIO203	41D	GPIO48	X3-11
42D	GPIO205	GPIO205	42D	GPIO49	X4-11
43D	GPIO207	GPIO207	43D	GPIO51	X6-11
45D	SCKA	SCKA	45D	GPIO54	X9-11
46D	PSCA0	PSCA0	46D	GPIO56	X3-12
47D	PSCA2	PSCA2	47D	GPIO57	X4-12
48D	PSCA4	PSCA4	48D	GPIO59	X6-12
50D	SCKB	SCKB	50D	GPIO62	X9-12
51D	PCSB0	PCSB0	51D	GPIO64	X3-14
52D	PCSB2	PCSB2	52D	GPIO65	X4-14
53D	PCSB4	PCSB4	53D	GPIO67	X6-14
55D	FPGA_TMS	FPGA_TMS	55D	GPIO70	X9-14
56D	FPGA_TDI	FPGA_TDI	56D	GPIO72	X3-15
57D	FPGA_TDO	FPGA_TDO	57D	GPIO73	X4-15
58D	FPGA_TCK	FPGA_TCK	58D	GPIO75	X6-15
60D	MPC_TDO	MPC_TDO	60D	GPIO78	X9-15
61D	/EVTO	/EVTO	61D	GPIO80	X3-16
62D	/EVTI	/EVTI	62D	GPIO81	X4-16
63D	/RDY	/RDY	63D	GPIO83	X6-16

phyCORE-MPC5554		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
65D	MCKO	MCKO	65D	GPIO86	X9-16
66D	MDO1	MDO1	66D	GPIO88	X3-17
67D	MDO3	MDO3	67D	GPIO89	X4-17
68D	MDO5	MDO5	68D	GPIO91	X6-17
70D	MDO7	MDO7	70D	GPIO94	X9-17
71D	MDO9	MDO9	71D	GPIO96	X3-19
72D	MDO10	MDO10	72D	GPIO97	X4-19
73D	MDO11	MDO11	73D	GPIO99	X6-19
75D	AN39	AN39	75D	GPIO102	X9-19
76D	AN37	AN37	76D	GPIO104	X3-20
77D	AN35	AN35	77D	GPIO105	X4-20
78D	AN33	AN33	78D	GPIO107	X6-20
80D	AN31	AN31	80D	GPIO110	X9-20
81D	AN29	AN29	81D	GPIO112	X3-21
82D	AN27	AN27	82D	GPIO113	X4-21
83D	AN25	AN25	83D	GPIO115	X6-21
85D	AN23	AN23	85D	GPIO118	X9-21
86D	AN21	AN21	86D	GPIO120	X3-22
87D	AN19	AN19	87D	GPIO121	X4-22
88D	AN17	AN17	88D	GPIO123	X6-22
90D	AN15	AN15	90D	GPIO126	X9-22
91D	AN13	AN13	91D	GPIO128	X3-24
92D	AN11	AN11	92D	GPIO129	X4-24
93D	AN9	AN9	93D	GPIO131	X6-24
95D	AN7	AN7	95D	GPIO134	X9-24
96D	AN5	AN5	96D	GPIO136	X3-25
97D	AN3	AN3	97D	GPIO137	X4-25
98D	AN1	AN1	98D	GPIO139	X6-25
100D	VRH	VRH	100D	GPIO142	X9-25

Table 17: Signal Pin Assignment for the phyCORE-MPC5554 / Development Board / Expansion Board

phyCORE MPC5554		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
VDD3V3	1C, 2C, 1D, 2D	VDD3V3	1C, 2C, 1D, 2D	VCC1	X2-1, X2-2 X3-1, X3-2
VDD5V	4C, 5C	5V	4C, 5C	VCC2	X4-1, X4-2
VDD3V3	4D, 5D	VDD3V3	4D, 5D	VCC3	X5-1, X5-2
DGND	2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A, 82A, 87A, 92A, 97A, 4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B, 84B, 89B, 94B, 99B, 3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D, 72C	DGND	2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A, 82A, 87A, 92A, 97A, 4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B, 84B, 89B, 94B, 99B, 3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D, 72C	GND	X2-3, X2-8, X2-13, X2-18, X2-23, X3-3, X3-8, X3-13, X3-18, X3-23, X4-3, X4-8, X4-13, X4-18, X4-23, X5-3, X5-8, X5-13, X5-18, X5-23, X6-3, X6-8, X6-13, X6-18, X6-23, X7-3, X7-8, X7-13, X7-18, X7-23, X8-3, X8-8, X8-13, X8-18, X8-23, X9-3, X9-8, X9-13, X9-18, X9-23, X10-3, X10-8, X10-13, X10-18, X10-23, X11-3, X11-8, X11-13, X11-18, X11-23, X12-3, X12-8, X12-13, X12-18, X12-23, X13-3, X13-8, X13-13, X13-18, X13-23, X14-3, X14-8, X14-13, X14-18, X14-23, X15-3, X15-8, X15-13, X15-18, X15-23, X16-3, X16-8, X16-13, X16-18, X16-23, X17-3, X17-8, X17-13, X17-18, X17-23
AGND	77C, 82C, 87C, 92C, 97C, 74D, 79D, 84D, 89D, 94D, 99D	AGND	77C, 82C, 87C, 92C, 97C, 74D, 79D, 84D, 89D, 94D, 99D		

Table 18: Pin Assignment Power Supply for the phyCORE-MPC5554 / Development Board / Expansion Board

11.3.7.2 Pin Assignment for phyCORE-MPC5567

phyCORE-MPC5567		Development Board Expansion Bus		Expansion Board Patch Field	
1A	EXTCLK	EXTCLK	1A	BUS0	X10-1
3A	IRQ4	IRQ4	3A	BUS4	X14-1
4A	IRQ5	IRQ5	4A	BUS5	X15-1
5A	FPGA_B1_IO0	FPGA_B1_IO0	5A	BUS6	X16-1
6A	FPGA_B1_IO1	FPGA_B1_IO1	6A	BUS7	X17-1
8A	FPGA_B1_IO6	FPGA_B1_IO6	8A	BUS12	X14-2
9A	FPGA_B1_IO7	FPGA_B1_IO7	9A	BUS13	X15-2
10A	FPGA_B1_IO8	FPGA_B1_IO8	10A	BUS14	X16-2
11A	FPGA_B1_IO9	FPGA_B1_IO9	11A	BUS15	X17-2
13A	FPGA_B1_IO14	FPGA_B1_IO14	13A	BUS20	X14-4
14A	FPGA_B1_IO15	FPGA_B1_IO15	14A	BUS21	X15-4
15A	FPGA_B1_IO16	FPGA_B1_IO16	15A	BUS22	X16-4
16A	FPGA_B1_IO17	FPGA_B1_IO17	16A	BUS23	X17-4
18A	FPGA_B1_IO22	FPGA_B1_IO22	18A	BUS28	X14-5
19A	FPGA_B1_IO23	FPGA_B1_IO23	19A	BUS29	X15-5
20A	FPGA_B1_IO24	FPGA_B1_IO24	20A	BUS30	X16-5
21A	FPGA_B1_IO25	FPGA_B1_IO25	21A	BUS31	X17-5
23A	FPGA_B4_IO4	FPGA_B4_IO4	23A	BUS36	X14-6
24A	FPGA_B4_IO5	FPGA_B4_IO5	24A	BUS37	X15-6
25A	FPGA_B4_IO6	FPGA_B4_IO6	25A	BUS38	X16-6
26A	FPGA_B4_IO7	FPGA_B4_IO7	26A	BUS39	X17-6
28A	FPGA_B4_IO12	FPGA_B4_IO12	28A	BUS44	X14-7
29A	FPGA_B4_IO13	FPGA_B4_IO13	29A	BUS45	X15-7
30A	FPGA_B4_IO14	FPGA_B4_IO14	30A	BUS46	X16-7
31A	FPGA_B4_IO15	FPGA_B4_IO15	31A	BUS47	X17-7
33A	FPGA_B4_IO20	FPGA_B4_IO20	33A	BUS52	X14-9
34A	FPGA_B4_IO21	FPGA_B4_IO21	34A	BUS53	X15-9
35A	FPGA_B4_IO22	FPGA_B4_IO22	35A	BUS54	X16-9
36A	FPGA_B4_IO23	FPGA_B4_IO23	36A	BUS55	X17-9
38A	FPGA_B2_IO0	FPGA_B2_IO0	38A	BUS60	X14-10
39A	FPGA_B2_IO1	FPGA_B2_IO1	39A	BUS61	X15-10
40A	FPGA_B2_IO2	FPGA_B2_IO2	40A	BUS62	X16-10
41A	FPGA_B2_IO3	FPGA_B2_IO3	41A	BUS63	X17-10
43A	FPGA_B2_IO8	FPGA_B2_IO8	43A	BUS68	X14-11
44A	FPGA_B2_IO9	FPGA_B2_IO9	44A	BUS69	X15-11
45A	FPGA_B2_IO10	FPGA_B2_IO10	45A	BUS70	X16-11
46A	FPGA_B2_IO11	FPGA_B2_IO11	46A	BUS71	X17-11
48A	FPGA_B2_IO16	FPGA_B2_IO16	48A	BUS76	X14-12
49A	FPGA_B2_IO17	FPGA_B2_IO17	49A	BUS77	X15-12
50A	FPGA_B2_IO18	FPGA_B2_IO18	50A	BUS78	X16-12
51A	FPGA_B2_IO19	FPGA_B2_IO19	51A	BUS79	X17-12
53A	FPGA_B3_IO4	FPGA_B3_IO4	53A	BUS84	X14-14
54A	FPGA_B3_IO5	FPGA_B3_IO5	54A	BUS85	X15-14
55A	FPGA_B3_IO6	FPGA_B3_IO6	55A	BUS86	X16-14
56A	FPGA_B3_IO7	FPGA_B3_IO7	56A	BUS87	X17-14

phyCORE-MPC5567		Development Board Expansion Bus		Expansion Board Patch Field	
58A	FPGA_VDDIO_B2	FPGA_VDDIO_B2	58A	BUS92	X14-15
59A	FPGA_VDDIO_B3	FPGA_VDDIO_B3	59A	BUS93	X15-15
60A	FEC_TXD3	ETPUB30	60A	BUS94	X16-15
61A	NC	TCRCLKB	61A	BUS95	X17-15
63A	FEC_TXD1	ETPUB28	63A	BUS100	X14-16
64A	FEC_TX_EN	ETPUB26	64A	BUS101	X15-16
65A	FEC_TXCLK	ETPUB24	65A	BUS102	X16-16
66A	NC	ETPUB22	66A	BUS103	X17-16
68A	VDD3V3	ETPUB20	68A	BUS108	X14-17
69A	NC	ETPUB18	69A	BUS109	X15-17
70A	NC	ETPUB16	70A	BUS110	X16-17
71A	FEC_RX_DV	ETPUB14	71A	BUS111	X17-17
73A	FEC_MCD	ETPUB12	73A	BUS116	X14-19
74A	VDD3V3	ETPUB10	74A	BUS117	X15-19
75A	FEC_RXD2	ETPUB8	75A	BUS118	X16-19
76A	FEC_MDIO	ETPUB6	76A	BUS119	X17-19
78A	NC	ETPUB4	78A	BUS124	X14-20
79A	NC	ETPUB2	79A	BUS125	X15-20
80A	NC	ETPUB0	80A	BUS126	X16-20
81A	ETPUA30	ETPUA30	81A	BUS127	X17-20
83A	ETPUA28	ETPUA28	83A	BUS132	X14-21
84A	ETPUA26	ETPUA26	84A	BUS133	X15-21
85A	ETPUA24	ETPUA24	85A	BUS134	X16-21
86A	ETPUA22	ETPUA22	86A	BUS135	X17-21
88A	ETPUA20	ETPUA20	88A	BUS140	X14-22
89A	ETPUA18	ETPUA18	89A	BUS141	X15-22
90A	ETPUA16	ETPUA16	90A	BUS142	X16-22
91A	ETPUA14	ETPUA14	91A	BUS143	X17-22
93A	ETPUA12	ETPUA12	93A	BUS148	X14-24
94A	ETPUA10	ETPUA10	94A	BUS149	X15-24
95A	ETPUA8	ETPUA8	95A	BUS150	X16-24
96A	FRB_RX	ETPUA6	96A	BUS151	X17-24
98A	FRB_TX	ETPUA4	98A	BUS156	X14-25
99A	ETPUA2	ETPUA2	99A	BUS157	X15-25
100A	ETPUA0	ETPUA0	100A	BUS158	X16-25
1B	CLKOUT	CLKOUT	1B	BUS1	X11-1
2B	IRQ2	IRQ2	2B	BUS2	X12-1
3B	IRQ3	IRQ3	3B	BUS3	X13-1
5B	FPGA_B1_IO2	FPGA_B1_IO2	5B	BUS8	X10-2
6B	FPGA_B1_IO3	FPGA_B1_IO3	6B	BUS9	X11-2
7B	FPGA_B1_IO4	FPGA_B1_IO4	7B	BUS10	X12-2
8B	FPGA_B1_IO5	FPGA_B1_IO5	8B	BUS11	X13-2
10B	FPGA_B1_IO10	FPGA_B1_IO10	10B	BUS16	X10-4
11B	FPGA_B1_IO11	FPGA_B1_IO11	11B	BUS17	X11-4
12B	FPGA_B1_IO12	FPGA_B1_IO12	12B	BUS18	X12-4
13B	FPGA_B1_IO13	FPGA_B1_IO13	13B	BUS19	X13-4
15B	FPGA_B1_IO18	FPGA_B1_IO18	15B	BUS24	X10-5
16B	FPGA_B1_IO19	FPGA_B1_IO19	16B	BUS25	X11-5

phyCORE-MPC5567		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
17B	FPGA_B1_IO20	FPGA_B1_IO20	17B	BUS26	X12-5
18B	FPGA_B1_IO21	FPGA_B1_IO21	18B	BUS27	X13-5
20B	FPGA_B4_IO0	FPGA_B4_IO0	20B	BUS32	X10-6
21B	FPGA_B4_IO1	FPGA_B4_IO1	21B	BUS33	X11-6
22B	FPGA_B4_IO2	FPGA_B4_IO2	22B	BUS34	X12-6
23B	FPGA_B4_IO3	FPGA_B4_IO3	23B	BUS35	X13-6
25B	FPGA_B4_IO8	FPGA_B4_IO8	25B	BUS40	X10-7
26B	FPGA_B4_IO9	FPGA_B4_IO9	26B	BUS41	X11-7
27B	FPGA_B4_IO10	FPGA_B4_IO10	27B	BUS42	X12-7
28B	FPGA_B4_IO11	FPGA_B4_IO11	28B	BUS43	X13-7
30B	FPGA_B4_IO16	FPGA_B4_IO16	30B	BUS48	X10-9
31B	FPGA_B4_IO17	FPGA_B4_IO17	31B	BUS49	X11-9
32B	FPGA_B4_IO18	FPGA_B4_IO18	32B	BUS50	X12-9
33B	FPGA_B4_IO19	FPGA_B4_IO19	33B	BUS51	X13-9
35B	FPGA_B4_IO24	FPGA_B4_IO24	35B	BUS56	X10-10
36B	FPGA_B4_IO25	FPGA_B4_IO25	36B	BUS57	X11-10
37B	FPGA_VDDIO_B1	FPGA_VDDIO_B1	37B	BUS58	X12-10
38B	FPGA_VDDIO_B4	FPGA_VDDIO_B4	38B	BUS59	X13-10
40B	FPGA_B2_IO4	FPGA_B2_IO4	40B	BUS64	X10-11
41B	FPGA_B2_IO5	FPGA_B2_IO5	41B	BUS65	X11-11
42B	FPGA_B2_IO6	FPGA_B2_IO6	42B	BUS66	X12-11
43B	FPGA_B2_IO7	FPGA_B2_IO7	43B	BUS67	X13-11
45B	FPGA_B2_IO12	FPGA_B2_IO12	45B	BUS72	X10-12
46B	FPGA_B2_IO13	FPGA_B2_IO13	46B	BUS73	X11-12
47B	FPGA_B2_IO14	FPGA_B2_IO14	47B	BUS74	X12-12
48B	FPGA_B2_IO15	FPGA_B2_IO15	48B	BUS75	X13-12
50B	FPGA_B3_IO0	FPGA_B3_IO0	50B	BUS80	X10-14
51B	FPGA_B3_IO1	FPGA_B3_IO1	51B	BUS81	X11-14
52B	FPGA_B3_IO2	FPGA_B3_IO2	52B	BUS82	X12-14
53B	FPGA_B3_IO3	FPGA_B3_IO3	53B	BUS83	X13-14
55B	FPGA_B3_IO8	FPGA_B3_IO8	55B	BUS88	X10-15
56B	FPGA_B3_IO9	FPGA_B3_IO9	56B	BUS89	X11-15
57B	FPGA_B3_IO10	FPGA_B3_IO10	57B	BUS90	X12-15
58B	FPGA_B3_IO11	FPGA_B3_IO11	58B	BUS91	X13-15
60B	FEC_TXD0	ETPUB31	60B	BUS96	X10-16
61B	VDD3V3	ETPUB29	61B	BUS97	X11-16
62B	FEC_TX_ER	ETPUB27	62B	BUS98	X12-16
63B	FEC_TXD2	ETPUB25	63B	BUS99	X13-16
65B	FEC_CRS	ETPUB23	65B	BUS104	X10-17
66B	NC	ETPUB21	66B	BUS105	X11-17
67B	NC	ETPUB19	67B	BUS106	X12-17
68B	FEC_COL	ETPUB17	68B	BUS107	X13-17
70B	FEC_RX_ER	ETPUB15	70B	BUS112	X10-19
71B	VDD3V3	ETPUB13	71B	BUS113	X11-19
72B	FEC_RXD3	ETPUB11	72B	BUS114	X12-19
73B	FEC_RX_CLK	ETPUB9	73B	BUS115	X13-19
75B	FEC_RXD1	ETPUB7	75B	BUS120	X10-20
76B	FEC_RXD0	ETPUB5	76B	BUS121	X11-20
77B	NC	ETPUB3	77B	BUS122	X12-20

phyCORE-MPC5567		Development Board Expansion Bus		Expansion Board Patch Field	
78B	TCRCLKA	TCRCLKA	78B	BUS123	X13-20
80B	NC	ETPUB1	80B	BUS128	X10-21
81B	ETPUA31	ETPUA31	81B	BUS129	X11-21
82B	ETPUA29	ETPUA29	82B	BUS130	X12-21
83B	ETPUA27	ETPUA27	83B	BUS131	X13-21
85B	ETPUA25	ETPUA25	85B	BUS136	X10-22
86B	ETPUA23	ETPUA23	86B	BUS137	X11-22
87B	ETPUA21	ETPUA21	87B	BUS138	X12-22
88B	ETPUA19	ETPUA19	88B	BUS139	X13-22
90B	ETPUA17	ETPUA17	90B	BUS144	X10-24
91B	ETPUA15	ETPUA15	91B	BUS145	X11-24
92B	ETPUA13	ETPUA13	92B	BUS146	X12-24
93B	ETPUA11	ETPUA11	93B	BUS147	X13-24
95B	ETPUA9	ETPUA9	95B	BUS152	X10-25
96B	ETPUA7	ETPUA7	96B	BUS153	X11-25
97B	FRB_TX_EN	ETPUA5	97B	BUS154	X12-25
98B	ETPUA3	ETPUA3	98B	BUS155	X13-25
100B	ETPUA1	ETPUA1	100B	BUS159	X17-25
6C	VBAT	VBAT	6C	VBAT	X6-1
8C	PWRGOOD	PWRGOOD	8C	PFO	X8-1
9C	/RSTCFG	/RSTCFG	9C	BOOT	X8-2
10C	/RESET	/RESET	10C	RESET	X9-1
11C	/RSTOUT	/RSTOUT	11C	RESOUT	X9-2
13C	EMIOS1	EMIOS1	13C	GPIO2	X5-4
14C	EMIOS3	EMIOS3	14C	GPIO4	X7-4
15C	EMIOS5	EMIOS5	15C	GPIO5	X8-4
16C	EMIOS7	EMIOS7	16C	GPIO7	X2-5
18C	FRA_TX	CANHB	18C	GPIO10	X5-5
19C	RXDB	RXDB	19C	GPIO12	X7-5
20C	TXDB	TXDB	20C	GPIO13	X8-5
21C	RXDB_RS232	RXDB_RS232	21C	GPIO15	X2-6
23C	TXDB_RS232	TXDB_RS232	23C	GPIO18	X5-6
24C	CNRXC	CNRXC	24C	GPIO20	X7-6
25C	CNTXC	CNTXC	25C	GPIO21	X8-6
26C	EMIOS9	EMIOS9	26C	GPIO23	X2-7
28C	EMIOS11	EMIOS11	28C	GPIO26	X5-7
29C	EMIOS13	EMIOS13	29C	GPIO28	X7-7
30C	EMIOS15	EMIOS15	30C	GPIO29	X8-7
31C	SCL	SCL	31C	GPIO31	X2-9
33C	LAN_LEDA	LAN_LEDA	33C	GPIO34	X5-9
34C	LAN_LEDB	LAN_LEDB	34C	GPIO36	X7-9
35C	LAN_TPI-	LAN_TPI-	35C	GPIO37	X8-9
36C	LAN_TPO-	LAN_TPO-	36C	GPIO39	X2-10
38C	EMIOS17	EMIOS17	38C	GPIO42	X5-10
39C	EMIOS19	EMIOS19	39C	GPIO44	X7-10
40C	EMIOS21	EMIOS21	40C	GPIO45	X8-10
41C	EMIOS23	EMIOS23	41C	GPIO47	X2-11
43C	GPIO204	GPIO204	43C	GPIO50	X5-11

phyCORE-MPC5567		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
44C	GPIO206	GPIO206	44C	GPIO52	X7-11
45C	SINA	SINA	45C	GPIO53	X8-11
46C	SOUTA	SOUTA	46C	GPIO55	X2-12
48C	PSCA1	PSCA1	48C	GPIO58	X5-12
49C	PSCA3	PSCA3	49C	GPIO60	X7-12
50C	PSCA5	PSCA5	50C	GPIO61	X8-12
51C	SINB	SINB	51C	GPIO63	X2-14
53C	SOUTB	SOUTB	53C	GPIO66	X5-14
54C	PCSB1	PCSB1	54C	GPIO68	X7-14
55C	PCSB3	PCSB3	55C	GPIO69	X8-14
56C	PCSB5	PCSB5	56C	GPIO71	X2-15
58C	/TEST	/TEST	58C	GPIO74	X5-15
59C	JCOPM	JCOPM	59C	GPIO76	X7-15
60C	MPC_TDI	MPC_TDI	60C	GPIO77	X8-15
61C	MPC_TCK	MPC_TCK	61C	GPIO79	X2-16
63C	MPC_TMS	MPC_TMS	63C	GPIO82	X5-16
64C	/MSEO0	/MSEO0	64C	GPIO84	X7-16
65C	/MSEO1	/MSEO1	65C	GPIO85	X8-16
66C	MDO0	MDO0	66C	GPIO87	X2-17
68C	MDO2	MDO2	68C	GPIO90	X5-17
69C	MDO4	MDO4	69C	GPIO92	X7-17
70C	MDO6	MDO6	70C	GPIO93	X8-17
71C	MDO8	MDO8	71C	GPIO95	X2-19
73C	DAC0	DAC0	73C	GPIO98	X5-19
74C	ETRIG1	ETRIG1	74C	GPIO100	X7-19
75C	ETRIG0	ETRIG0	75C	GPIO101	X8-19
76C	AN38	AN38	76C	GPIO103	X2-20
78C	AN36	AN36	78C	GPIO106	X5-20
79C	AN34	AN34	79C	GPIO108	X7-20
80C	AN32	AN32	80C	GPIO109	X8-20
81C	AN30	AN30	81C	GPIO111	X2-21
83C	AN28	AN28	83C	GPIO114	X5-21
84C	AN26	AN26	84C	GPIO116	X7-21
85C	AN24	AN24	85C	GPIO117	X8-21
86C	AN22	AN22	86C	GPIO119	X2-22
88C	AN20	AN20	88C	GPIO122	X5-22
89C	AN18	AN18	89C	GPIO124	X7-22
90C	AN16	AN16	90C	GPIO125	X8-22
91C	AN14	AN14	91C	GPIO127	X2-24
93C	AN12	AN12	93C	GPIO130	X5-24
94C	AN10	AN10	94C	GPIO132	X7-24
95C	AN8	AN8	95C	GPIO133	X8-24
96C	AN6	AN6	96C	GPIO135	X2-25
98C	AN4	AN4	98C	GPIO138	X5-25
99C	AN2	AN2	99C	GPIO140	X7-25
100C	AN0	AN0	100C	GPIO141	X8-25
6D	VPD	VPD	6D	*VPD	X6-2
7D	/WDO	/WDO	7D	PFI	X7-1

phyCORE-MPC5567		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
8D	WDI	WDI	8D	WDI	X7-2
10D	X_10D	X_10D	10D	RESIN	X2-4
11D	EMIOS0	EMIOS0	11D	GPIO0	X3-4
12D	EMIOS2	EMIOS2	12D	GPIO1	X4-4
13D	EMIOS4	EMIOS4	13D	GPIO3	X6-4
15D	EMIOS6	EMIOS6	15D	GPIO6	X9-4
16D	RXDA	RXDA	16D	GPIO8	X3-5
17D	TXDA	TXDA	17D	GPIO9	X4-5
18D	FRA_RX	CANLB	18D	GPIO11	X6-5
20D	CANLA	CANLA	20D	GPIO14	X9-5
21D	CANHA	CANHA	21D	GPIO16	X3-6
22D	RXDA_RS232	RXDA_RS232	22D	GPIO17	X4-6
23D	TXDA_RS232	TXDA_RS232	23D	GPIO19	X6-6
25D	EMIOS8	EMIOS8	25D	GPIO22	X9-6
26D	EMIOS10	EMIOS10	26D	GPIO24	X3-7
27D	EMIOS12	EMIOS12	27D	GPIO25	X4-7
28D	EMIOS14	EMIOS14	28D	GPIO27	X6-7
30D	EMIOS16	EMIOS16	30D	GPIO30	X9-7
31D	EMIOS18	EMIOS18	31D	GPIO32	X3-9
32D	SDA	SDA	32D	GPIO33	X4-9
33D	/RTC_IRQ	/RTC_IRQ	33D	GPIO35	X6-9
35D	LAN_TPI+	LAN_TPI+	35D	GPIO38	X9-9
36D	LAN_TPO+	LAN_TPO+	36D	GPIO40	X3-10
37D	DQ1WIRE	DQ1WIRE	37D	GPIO41	X4-10
38D	EMIOS20	EMIOS20	38D	GPIO43	X6-10
40D	EMIOS22	EMIOS22	40D	GPIO46	X9-10
41D	GPIO203	GPIO203	41D	GPIO48	X3-11
42D	GPIO205	GPIO205	42D	GPIO49	X4-11
43D	GPIO207	GPIO207	43D	GPIO51	X6-11
45D	SCKA	SCKA	45D	GPIO54	X9-11
46D	PSCA0	PSCA0	46D	GPIO56	X3-12
47D	PSCA2	PSCA2	47D	GPIO57	X4-12
48D	PSCA4	PSCA4	48D	GPIO59	X6-12
50D	SCKB	SCKB	50D	GPIO62	X9-12
51D	PCSB0	PCSB0	51D	GPIO64	X3-14
52D	FRA_TX_EN	PCSB2	52D	GPIO65	X4-14
53D	PCSB4	PCSB4	53D	GPIO67	X6-14
55D	FPGA_TMS	FPGA_TMS	55D	GPIO70	X9-14
56D	FPGA_TDI	FPGA_TDI	56D	GPIO72	X3-15
57D	FPGA_TDO	FPGA_TDO	57D	GPIO73	X4-15
58D	FPGA_TCK	FPGA_TCK	58D	GPIO75	X6-15
60D	MPC_TDO	MPC_TDO	60D	GPIO78	X9-15
61D	/EVTO	/EVTO	61D	GPIO80	X3-16
62D	/EVTI	/EVTI	62D	GPIO81	X4-16
63D	/RDY	/RDY	63D	GPIO83	X6-16
65D	MCKO	MCKO	65D	GPIO86	X9-16
66D	MDO1	MDO1	66D	GPIO88	X3-17
67D	MDO3	MDO3	67D	GPIO89	X4-17
68D	MDO5	MDO5	68D	GPIO91	X6-17

phyCORE-MPC5567		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
70D	MDO7	MDO7	70D	GPIO94	X9-17
71D	MDO9	MDO9	71D	GPIO96	X3-19
72D	MDO10	MDO10	72D	GPIO97	X4-19
73D	MDO11	MDO11	73D	GPIO99	X6-19
75D	AN39	AN39	75D	GPIO102	X9-19
76D	AN37	AN37	76D	GPIO104	X3-20
77D	AN35	AN35	77D	GPIO105	X4-20
78D	AN33	AN33	78D	GPIO107	X6-20
80D	AN31	AN31	80D	GPIO110	X9-20
81D	AN29	AN29	81D	GPIO112	X3-21
82D	AN27	AN27	82D	GPIO113	X4-21
83D	AN25	AN25	83D	GPIO115	X6-21
85D	AN23	AN23	85D	GPIO118	X9-21
86D	AN21	AN21	86D	GPIO120	X3-22
87D	AN19	AN19	87D	GPIO121	X4-22
88D	AN17	AN17	88D	GPIO123	X6-22
90D	AN15	AN15	90D	GPIO126	X9-22
91D	AN13	AN13	91D	GPIO128	X3-24
92D	AN11	AN11	92D	GPIO129	X4-24
93D	AN9	AN9	93D	GPIO131	X6-24
95D	AN7	AN7	95D	GPIO134	X9-24
96D	AN5	AN5	96D	GPIO136	X3-25
97D	AN3	AN3	97D	GPIO137	X4-25
98D	AN1	AN1	98D	GPIO139	X6-25
100D	VRH	VRH	100D	GPIO142	X9-25

Table 19: Signal Pin Assignment for the phyCORE-MPC5567 / Development Board / Expansion Board

phyCORE MPC5554		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
VDD3V3	1C, 2C, 1D, 2D	VDD3V3	1C, 2C, 1D, 2D	VCC1	X2-1, X2-2 X3-1, X3-2
VDD5V	4C, 5C	5V	4C, 5C	VCC2	X4-1, X4-2
VDD3V3	4D, 5D	VDD3V3	4D, 5D	VCC3	X5-1, X5-2
DGND	2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A, 82A, 87A, 92A, 97A, 4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B, 84B, 89B, 94B, 99B, 3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D, 72C	DGND	2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A, 82A, 87A, 92A, 97A, 4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B, 84B, 89B, 94B, 99B, 3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D, 72C	GND	X2-3, X2-8, X2-13, X2-18, X2-23, X3-3, X3-8, X3-13, X3-18, X3-23, X4-3, X4-8, X4-13, X4-18, X4-23, X5-3, X5-8, X5-13, X5-18, X5-23, X6-3, X6-8, X6-13, X6-18, X6-23, X7-3, X7-8, X7-13, X7-18, X7-23, X8-3, X8-8, X8-13, X8-18, X8-23, X9-3, X9-8, X9-13, X9-18, X9-23, X10-3, X10-8, X10-13, X10-18, X10-23, X11-3, X11-8, X11-13, X11-18, X11-23, X12-3, X12-8, X12-13, X12-18, X12-23, X13-3, X13-8, X13-13, X13-18, X13-23, X14-3, X14-8, X14-13, X14-18, X14-23, X15-3, X15-8, X15-13, X15-18, X15-23, X16-3, X16-8, X16-13, X16-18, X16-23, X17-3, X17-8, X17-13, X17-18, X17-23
AGND	77C, 82C, 87C, 92C, 97C, 74D, 79D, 84D, 89D, 94D, 99D	AGND	77C, 82C, 87C, 92C, 97C, 74D, 79D, 84D, 89D, 94D, 99D		

Table 20: Pin Assignment Power Supply for the phyCORE-MPC5567 / Development Board / Expansion Board

11.3.8 JTAG/Once/Nexus Debug Interface

The development board PCM-979 provides two debug connectors.

X2 reduced JTAG/OnCE/Nexus port to a 14-pin header connector (2.54 mm pin spacing)

X3 full JTAG/OnCE/Nexus port to a 38-pol Mictor AMP 767054-1

11.3.9 Reduced JTAG/OnCE/NEXUS Pin Header Connector X2

The 14-pin header connector at X2 on the Development Board enables connection of a simple external debug interface device (e.g. P&E Wiggler).

Signal	Pin Number	Pin Number	Signal
MPC_TDI	1	2	DGND
MPC_TDO	3	4	DGND
MPC_TCK	5	6	DGND
Nc	7	8	Nc
/RESET	9	10	MPC_TMS
VDD3V3	11	12	DGND
/RDY	13	14	JCOMP

Table 21: Pin Assignment of the Reduced JTAG/OnCE/Nexus Pin Header X2

11.3.10 Full JTAG/OnCE/NEXUS Pin Header Connector X3

The pin header connector at X3 supports a standard 38-pin NEXUS debug connection (connector type AMP 767054-1) to various emulator probes (e.g. iSystem IC3000)

Signal	Pin Number	Pin Number	Signal
NC	1	2	NC
NC	3	4	NC
MDO9	5	6	CLKOUT
Vendor	7	8	MDO8
/RESET	9	10	/EVTI
MPC_TDO	11	12	VDD3V3
MDO10	13	14	/RDY
MPC_TCK	15	16	MDO7
MPC_TMS	17	18	MDO6
MPC_TDI	19	20	MDO5
JCOMP	21	22	MDO4
MDO11	23	24	MDO3
vendor	25	26	MDO2
NC	27	28	MDO1
NC	29	30	MDO0
NC	31	32	/EVTO
NC	33	34	MCKO
NC	35	36	/MSEO1
NC	37	38	/MSEO0

Table 22: Pin Assignment of the Full JTAG/OnCE/Nexus Pin Header X3

11.4 Technical Specification of the Development Board

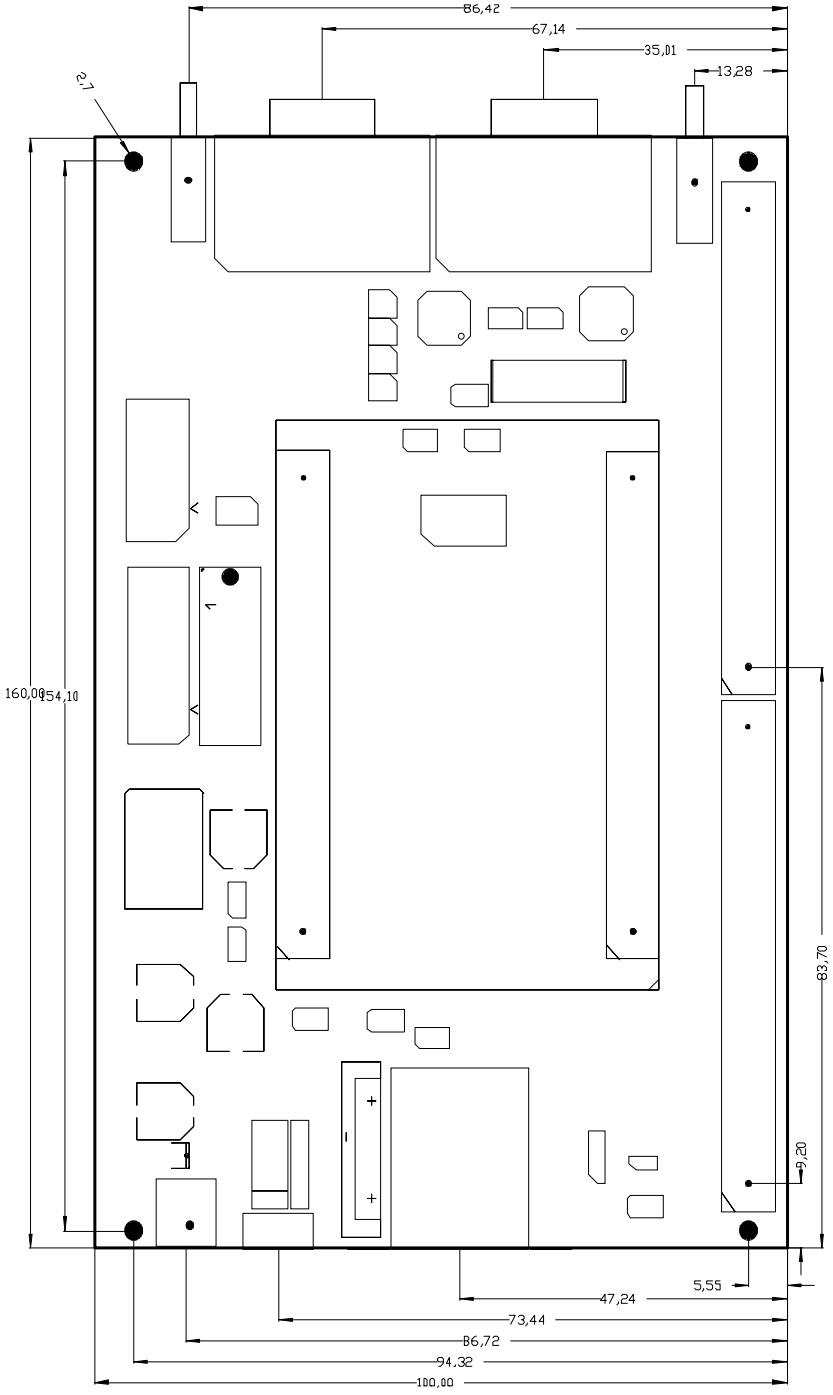

Figure 23 Physical Dimensions of the Development Board PCM-979

Technical Data:

Parameter	Requirements	Characteristics
Dimensions		160 mm x 100 mm
Humidity		Max. 95 % r.F., not condensed
Storage Temp. Range		-40° to +90°C
Operating Temp. Range:		0 °C to +70 °C
Operating voltages:		5 V ±10 %
Operating Power Consumption: Voltage +5 V	phyCORE-MPC5554 128 MHz core clock 8 MByte BurstRAM 8 MByte Flash LAN91C111 FPGA XP6 without any installed I/O line or expansion board	 Typ. 1000 mA

Table 23: Technical Data of the Development Board PCM-979

11.5 Release Notes

The following section contains information about deviations to the description in this manual. Revisions to previous manuals are also listed.

Caution:
This manual exclusively describes the board revisions 1241.0 and 1241.1

Revision: PCB# 1241.0

- PCB footprint of the Expansion Bus has wrong grid. X7 is unpopulated.

- L6 RJ45 connector has wrong PCB footprint. Some mechanical changes were done prior population of the LAN connector.

Revision: PCB# 1241.1

- Ethernet LAN is not working properly while the Expansion Board PCM977 is connected to the Expansion Bus.

12 Technical Specifications

The physical dimensions of the phyCORE-MPC5554 are represented in *Figure 24.*

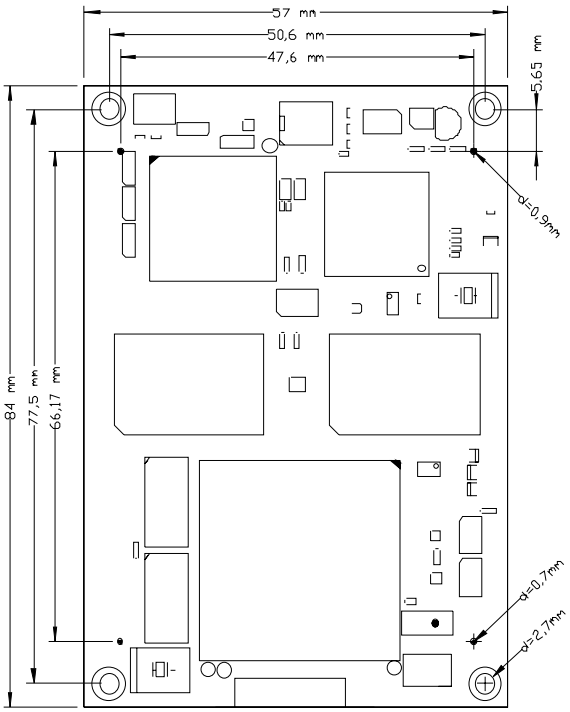

Figure 24: Physical Dimensions (Top View)

The holes with diameter 0.7 m and 0.9 mm are the positioning holes for the Molex connectors.

The module edge mounting holes are plated and connected to DGND.

The height of all components on the top side of the PCB is ca. 3 mm. The PCB itself is approximately 1.3 mm thick. The Molex connector pins are located on the underside of the PCB, oriented parallel to its two long sides. The maximum height of components on the underside of the PCB is 3 mm.

Additional Technical Data:

Parameter	Requirements	Characteristics
Dimensions		84 mm x 57 mm
Weight	With maximum circuitry installed	Approx. 40 grams
Humidity		Max. 95 % r.F. not condensed
Storage Temp. Range		-40° to +90°C
Operating Temp. Range		-40 °C to +85 °C
Operating voltages: Voltage 3.3 V Voltage 5 V		 3.3 V ±5 % 5 V ±5 %
Operating Power Consumption: Voltage 3.3 V Voltage 5 V	MPC5554/5567 128 MHz frequency 8 MByte SRAM 8 MByte stand. Flash Ethernet FPGA XP6	 Typ. 900 mA Typ. 60 mA

Table 24: Technical Data

These specifications describe the standard configuration of the phyCORE-MPC5554 as of the printing of this manual.

Connectors on the phyCORE-MPC5554:

Manufacturer	Molex
Number of pins per contact rows	200 (2 rows of 100 pins each)
Molex part number	52760-2009 (receptacle)

Two different heights are offered for the receptacle sockets that correspond to the connectors populating the underside of the phyCORE-MPC5554. The given connector height indicates the distance between the two connected PCBs when the module is mounted on the corresponding carrier board. In order to get the exact spacing, the maximum component height (3 mm) on the underside of the phyCORE must be subtracted.

Component height 6 mm

Manufacturer	Molex
Number of pins per contact row	200 (2 rows of 100 pins each)
Molex type number	53467-2009 (header)

Component height 10 mm

Manufacturer	Molex
Number of pins per contact row	200 (2 rows of 100 pins each)
Molex type number	53553-2009 (header)

Please refer to the corresponding data sheets and mechanical specifications provided by Molex (www.molex.com).

13 Hints for Handling the Module

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Integrating the phyCORE-MPC5554 in Application Circuitry

Successful integration in user target circuitry depends on whether the layout for the GND connections matches those of the phyCORE module. It is recommended that the target application circuitry is equipped with one layer dedicated to carry the GND potential. In any case, be sure to connect all GND pins neighboring signals which are used in the application circuitry. For the supply voltage, there must be contact with at least six of the GND pins neighboring the supply voltage pins.

14 Design Considerations - Check List

Please note the following points when implementing the phyCORE-MPC5554 into target applications:

> Data line D31 represents the LSB and D0 the MSB.
> Address line A31 represents the LSB and A8 the MSB.
> Byte ordering is big Endian.

Due to the conversion of little to big Endian byte ordering, the byte portions of LAN91C111 data bus are swapped to the MPC5554 data bus. Respectively the processor recognizes the LAN91C111 register contents byte-swapped. The network data stream, read from the frame buffer, is supplied in correct Big Endian byte order.

MPC5554 I/O signals (not bus signals) need an input high level of 0.65*VDDEH. Each VDDEHx is connected on-board to VDD3V3 or VDD5V via jumpers J14-J18. Default for all is VDD3V3. Respectively the I/O's need a input high voltage level of 0.65*(3.3 V+5 %) = 2.25 V. The 5 % are the margin of the acceptable input voltage tolerance.
The internal ADC of the MPC5554 works with VDD5V. Respectively the nominal input operating range is up to 5 V.
Never connect signals to the MPC5554 output drivers carrying a higher potentials (e.g. pull-ups) than the internal supply voltage.

For more information on the controller's I/O voltage range as well as other controller-related features please refer to the detailed MPC5554 or MPC5567 User's Manual provided by Freescale.

15 Revision History

Date	Version numbers	Changes in this manual
31-January-2006	Manual L-484e_0 PCM-028 PCB# 1239.1 PCM-979 PCB# 1241.1	First preliminary edition.
26-January 2007	Manual L-484e_1	Table 1: Pin assignment 22B and 23B corrected. 2B and 3B description corrected. AGND pins inserted for D. Module block diagram Figure 1: 12MHz changed to 8MHz Figure 10, Figure 12 and Figure 13: Description of Dual RS232 and Dual FlexCAN corrected. P2 is Dual RS232 and P1 is Dual FlexCAN.
1-December 2008	Manual L-484e_2	Hardware revision 1239.3 Deviated Pin description for MPC5567 added. Description for J39 to J44 added. FPGA basic firmware description added

A Appendices

A.1 Release Notes

The following section contains information about deviations to the description in this manual. Revisions to previous manuals are also listed.

Caution:
This manual exclusively describes the board revision 1239.3

Revision: PCB# 1239.0

No known issues.

Revision: PCB# 1239.1

Comparison to 1239.0:

Data lines to the LAN91C1111 are now swapped due to little to big Endian conversion. Network payload data are transferred in the right order and can be copied direct to the memory. Configuration and status registers must be handled by swapping the data bytes.

Revision: PCB# 1239.2
Not existing

Revision: PCB# 1239.3

No known issues.

Comparison to 1239.1:

The 1239.3 now has only two Sync. Burst memory banks to reduce the bus load of the system. With using higher device capacities, the same system memory amount is supported. To support the MPC5567's 40MHz input clock mode, R122 was added. J41 to J44 conncects the MPC5567 FEC power inputs to the power supply net. The CAN Transceivers can now fed with different power supply via J40 depending on the use alternative Transceiver type.

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Document: **phyCORE-MPC5554**
Document number: **L-484e_2, December 2008**

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Did you find any mistakes in this manual? page

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Published by

PHYTEC

Ordering No. L-484e_2
Printed in Germany