Development Board for phyCORE-MPC555 PCM-995

Hardware Manual

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Preface

This manual describes only the functions of the PHYTEC Development Board. The controllers and relevant Single Board Computers for use with the Development Board are not described herein. Additional controller- and board-level information and technical descriptions can be found in appropriate Hardware Manual or User's Manual support documentation. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration regarding Electro Magnetic Conformity of the PHYTEC Development Board PCM-995

PHYTEC Development Boards (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Note:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header rows or connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The Development Board phyCORE-MPC555 is one of a series of PHYTEC Development Boards supporting the phyCORE-MPC555 Single Board Computer module. PHYTEC supports common 8-, 16- and selected 32-bit controllers on two types of Single Boards Computers:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform
(2) as insert-ready, fully functional micro-, mini- and phyCORE OEM modules, which can be embedded directly into the user's peripheral hardware, design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market.

1 Introduction

The Development Board phyCORE-MPC555, in EURO-card dimensions (160 x 100 mm.), is a universal carrier board for start-up and programming of the PHYTEC phyCORE-MPC555 Single Board Computer module with two high density SMT (160 pins each, 0.63 mm pitch) pin header connectors. The Development Board is fully equipped with all mechanical and electrical components necessary for the speedy and secure insertion and subsequent programming of the high-density PHYTEC phyCORE module. These components include DB-9, DB-25, VG-96 and power socket connectors. The phyCORE module can be plugged like a "big chip" onto the Development Board's Molex connector receptacles. Once programmed, the phyCORE module can be removed from the Development Board and inserted like a "big chip" in a target hardware application.

The Development Board was designed to support software development, debugging and programming of the phyCORE-MPC555 Single Board Computer module.

The hardware manual for this Development Board does not describe the features and functions of the phyCORE-MPC55 SBC module, as this is not relevant for the basic functioning of the Development Board. For module and controller-specific features *please refer to the corresponding Hardware Manuals/User's Manuals*.

The Development Board offers the following features:

- Reset push button, configurable via jumper for different reset signals
- IRQ push button, configurable via jumper for different interrupt signals
- Wake-up push button
- Boot jumper to select internal or external Flash memory
- Jumper to enable the programming voltage for internal Flash memory
- Reset jumper to choose between internal and external reset configuration
- Two software programmable LED's (red/green)
- LED's for power monitoring
- LED to monitor debug or run mode
- Power supply for unregulated input voltage from 7 V to 12 V. It supplies regulated +5 V, +3.3 V for the phyCORE-MPC555. Additional +5 V is created for the VG96 connector.
- VG-96 connector with all I/O signals of the MPC555
- Two standard width pin header rows (3x54) which provide all phyCORE-MPC555 signals
- Two DB-9 sockets for RS-232 interface
- Two DB-9 plugs for two separate CAN interfaces with configurable terminating resistors
- DB-25 plug for BDM interface to support direct connection to a host-PC's printer port
- 2* 5-pin standard width header rows to support 3rd party BDM interfaces

1.1 Block Diagram

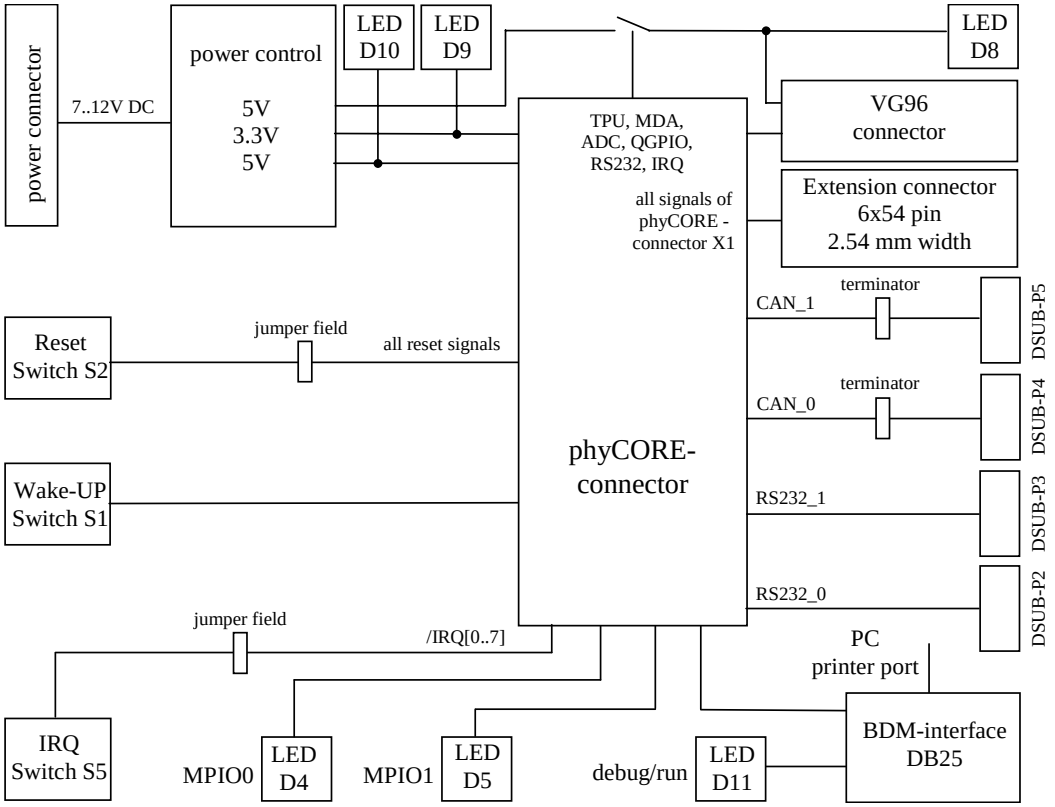


Figure 1: Block Diagram of the Development Board

1.2 Overview

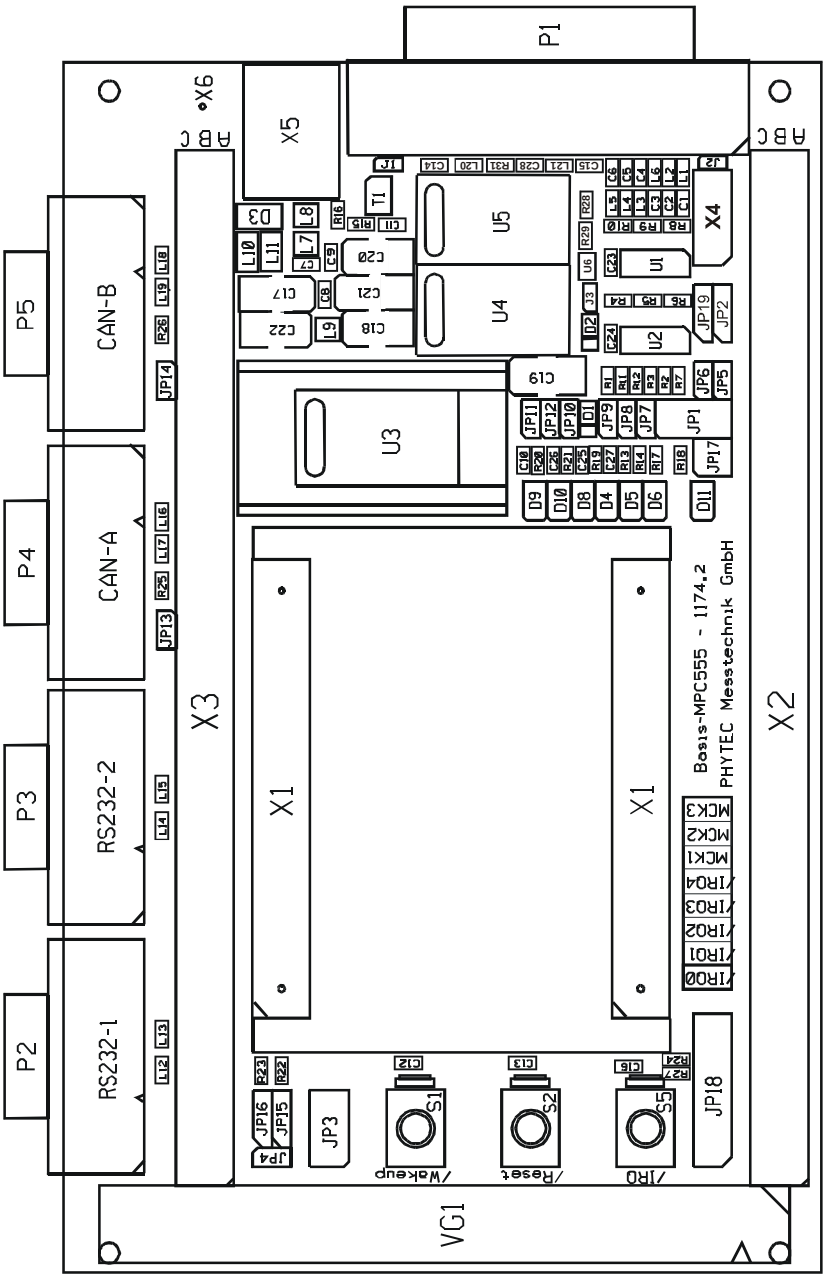


Figure 2: Development Board Overview (Component Side)

2 Connectors

Please note that all connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As depicted below, the following connectors are available on the Development Board:

- X1: receptacle to install the phyCORE-MPC555 SBC module
- X2, X3: 2.54 mm standard width pin header rows for extension boards, providing all signals of the phyCORE-connector X1
- X4: 2* 5-pin 2.54 mm standard width header row to connect to external BDM interfaces
- X5: low voltage power source connector
- VG1: VG-96 I/O peripheral connector
- P1: DB-25 plug of the on-board BDM interface
- P2, P3: DB-9 sockets for both RS-232 interfaces
- P4, P5: DB-9 plugs for both CAN interfaces

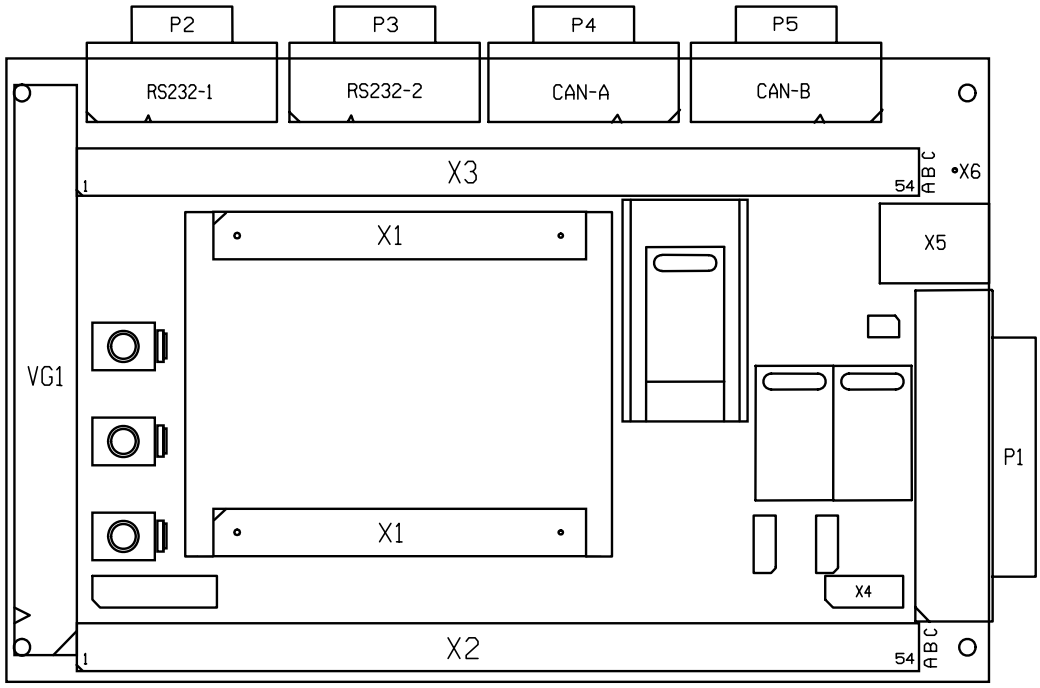


Figure 3: Connector Location

2.1 Power Connector X5

The low voltage socket at X5 can be used to supply power to the Development Board.

Caution:
Please avoid changing jumpers or modules while the Development Board is powered up.

2.1.1 Connection via the Low Voltage Socket X5

An unregulated power supply with the following characteristics can be connected to the Development Board at low voltage socket X5.

DC input voltage range: 7 V to 12 V

Recommended power supply:

9V@500mA for phyCORE-MPC555 equipped up to 1 MByte synchronous burst SRAM

9V@1000mA for phyCORE-MPC555 equipped more than 1 MByte synchronous burst SRAM

The on-board supply voltage conversion consists of two paths. One path will generate +5 VDC and +3.3 VDC for supplying the phyCORE-MPC555 module using DC/DC converters at U3 and U4. The second path is generating +5 VDC using a third DC/DC converter at U5 to supply the VG-96 I/O connector. Jumpers JP11 and JP12 connect the +5 VDC and +3.3 VDC voltage to the phyCORE module while JP10 connects the +5 VDC_{EXT} to the VG-96 connector.

The +5 VDC_{EXT} can be switched with FET T1 which is controlled by the /PWRON signal of the phyCORE-MPC555. This enables software controlled switching of any peripheral circuitry attached to the I/O connector VG1 if the SBC module goes into power down mode. If +5 VDC_{EXT} is required constantly J1 must be closed. This will bypass the FET switch T1.

The status of each output voltage is monitored by a LED.

- LED D9: +5 VDC for phyCORE-MPC555
- LED D10: +3.3 VDC for phyCORE-MPC555
- LED D8: +5 VDC_{EXT} for the VG-96 connector

- The maximum total power dissipation of the +5 V/+3V3 path must not exceed 5 watts. The current draw is limited to 750 mA by the input EMI filter.

5 watts > (input voltage – 5 V) x total current and max total current < 750 mA

The nominal current consumption of phyCORE-MPC555 is about 300….520 mA@3V3 and 40 mA@5 V. It is not recommended to supply additional loads with these voltages.

For the maximum current of 750 mA the input voltage is limited to 12 VDC.

- The maximum power dissipation of the +5 V_{EXT} path must not exceed 2 watts.

2 watts > (input voltage – 5 V) x current

For 12 VDC input voltage, the maximum current allowed for +5 V_{EXT} path adds up to 280 mA.

If the power supply adapter that is included with the Development Board is not used, make sure that the correct polarity is used on any other implemented power supply as depicted in the figure below.

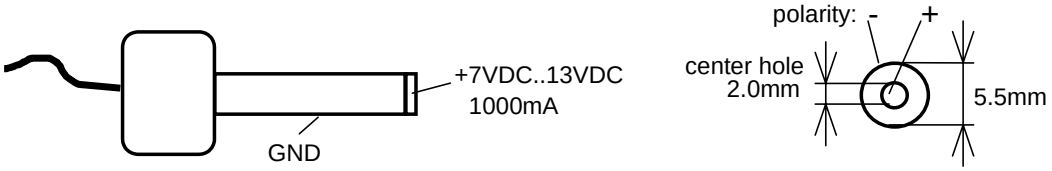


Figure 4: Polarity of the Power Connector at X5

2.2 DB-25 Socket P1 – BDM Interface

The DB-25 socket (male) P1 connects the on-board BDM interface logic to a PC's printer port. A standard DB-25 male-female cable must be used to establish the connection. The length of the DB-25 cable must not exceed 2 meters.

A set of jumpers associated with the on-board BDM interface logic is available to configure the signal connection *(refer to section 3.1)*.

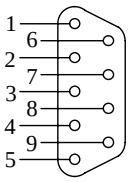
Two LED's display the status of the target. LED D11 (red) will illuminate if the phyCORE is held in debug mode. LEDD6 (red) will light if the target is in reset state (reset active).

2.3 DB-9 Sockets P2 and P3 – RS-232 Interfaces

The DB-9 sockets at P2 and P3 can be used as RS-232 interfaces. P2 corresponds to MPC555 UART 1 and P3 to MPC555 UART 2.

The pinout is shown in the figure below:

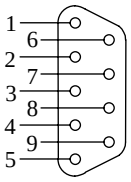
DB-9 socket P2



Pin 2: TXD1 (RS-232)
Pin 3: RXD1 (RS-232)
Pin 5: GND

Figure 5: *Pinout of DB-9 Socket P2 (Front View)*

DB-9 socket P3



Pin 2: TXD2 (RS-232)
Pin 3: RXD2 (RS-232)
Pin 5: GND

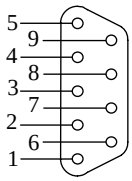
Figure 6: Pinout of DB-9 socket P3 (Front View)

2.4 DB-9 Plugs P4 and P5 – CAN Interfaces

The DB-9 plugs at P4 and P5 can be used as CAN interfaces. P4 corespondents to MPC555 CAN channel A and P5 to MPC555 CAN channel B.

The pinout is shown in the figure below:

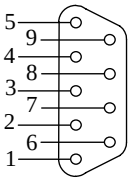
DB-9 plug P4



Pin 2:	A_CANL
Pin 7:	A_CANH
Pin 3,6:	GND

Figure 7: *Pinout of the DB-9 Plug at P4 (Front View)*

DB-9 plug P5



Pin 2:	B_CANL
Pin 7:	B_CANH
Pin 3,6:	GND

Figure 8: *Pinout of the DB-9 Plug at P5 (Front View)*

For each CAN channel a terminating resistor of 120 Ohm is configurable via removable jumpers. Closing Jumper JP13 terminates CAN channel A (P4), while closing Jumper JP14 terminates CAN channel B (P5).

2.5 10-pin Header X4 – External BDM Interface

This section contains important information regarding the use of external BDM interfaces on the phyCORE-MPC555 Development Board PCM-995 in conjunction with the phyCORE-MCP555 Single Board Computer module.

The factory default jumper settings of the phyCORE-MPC555 Development Board (PCM-995) connect the BDM signals from the MPC555 controller through the phyCORE-MPC555 Molex connector to the on-board BDM interface logic. This allows for immediate operation of the Rapid Development Kit and the Metrowerks CodeWarrior tool chain without requiring an external BDM device simply by connecting the DB-25 connector with the LPT port on your computer or laptop.

As an alternative, an external BDM interface can be used at pin header connector X4. In this case Jumpers JP1 as well as JP5 through JP9 on the Development Board must be removed. This disconnects the controller's BDM signals from the on-board interface logic.

Jumper JP2 must be configured according to the BDM interface supply voltage requirements. Jumper JP2 connects the VBDM signal (pin 9 on X4) with either the +3V3 or the +5 V supply voltage of the phyCORE-MPC555 Development Board. No supply voltage is available at pin 9, if Jumper JP2 remains open. *Refer to your BDM interface data sheet for more information on the VBDM supply voltage level.*

The pin assignment of the 10-pin header connector X4 on the PHYTEC phyCORE-MPC555 Development Board is shown in the following table.

BDM Signal	Pin	Pin	BDM Signal
VFLS0	1	2	/SRESET
GND	3	4	DSCK
GND	5	6	VFLS1
/HRESET	7	8	DSDI
VBDM	9	10	DSDO

Table 1: BDM Connector X4 Pin Assignment

A 10 kOhm pull-down resistor for the DSCK signal is located on the phyCORE-MPC555 SBC module.

Note:
Using an external BDM interface at X4 on the phyCORE-MPC555 Development Board without opening Jumpers JP1 and JP5 through JP9 may result in damage to the on-board circuitry or to the BDM interface. Make sure JP2 is set to the correct position in order to supply the required VBDM voltage. Never operate the hardware with an external BDM interface and the Jumpers mentioned above closed!

2.6 VG-96 I/O Connector VG1

The I/O connector VG1 is a standard 96 pin (3* 32 A-B-C, male) DIN41612 connector.

	A		**B**		**C**
1	GND	33	GND	65	GND
2	nc	34	/IRQ2	66	/IRQ3
3	/IRQ4	35	B_CNRX0	67	B_CNTX0
4	RXD2_TTL	36	TXD2_TTL	68	B_TPU0
5	B_TPU1	37	B_TPU2	69	B_TPU3
6	B_TPU4	38	B_TPU5	70	B_TPU6
7	B_TPU7	39	B_TPU8	71	B_TPU9
8	B_TPU10	40	B_TPU11	72	B_TPU12
9	B_TPU13	41	B_TPU14	73	B_TPU15
10	B_T2CLK	42	A_T2CLK	74	A_TPU0
11	A_TPU1	43	A_TPU2	75	A_TPU3
12	A_TPU4	44	A_TPU5	76	A_TPU6
13	A_TPU7	45	A_TPU8	77	A_TPU9
14	A_TPU10	46	A_TPU11	78	A_TPU12
15	A_TPU13	47	A_TPU14	79	A_TPU15
16	VRH	48	GNDA	80	A_AD0
17	A_AD1	49	A_AD2	81	A_AD3
18	A_AD4	50	A_AD5	82	A_AD6
19	A_AD7	51	A_AD8	83	A_AD9
20	A_AD10	52	A_AD11	84	A_AD12
21	A_AD13	53	A_AD14	85	A_AD15
22	ETRIG1	54	MDA0	86	MDA1
23	MDA2	55	MDA3	87	MDA4
24	MDA5	56	MDA6	88	MDA7
25	MDA8	57	MDA9	89	MPWM0
26	MPWM1	58	MPWM2	90	MPWM3
27	MPIO8	59	MPIO9	91	MPIO10
28	MPIO11	60	MPIO12	92	MPIO13
29	MPIO14	61	MPIO15	93	QGPIO0
30	QGPIO1	62	QGPIO2	94	QGPIO3
31	QGPIO4	63	QGPIO5	95	QGPIO6
32	+5VEXT	64	+5VEXT	96	+5VEXT

Table 2: Pinout of the I/O Connector VG1

The $+5V_{EXT}$ supply voltage is generated by the DC/DC converter populating U5. The $+5\ VDC_{EXT}$ can be switched with FET T1 which is controlled by the /PWRON signal of the phyCORE-MPC555. This enables software controlled switching of any peripheral circuitry attached to the I/O connector VG1 if the SBC module goes into power down mode. If $+5\ VDC_{EXT}$ is required constantly J1 must be closed. This will bypass the FET switch T1.

- The maximum power dissipation of the $+5V_{EXT}$ path must not exceed 2 watts.

2 watt > (input voltage – 5 V) x current

For 12 VDC input voltage, the maximum current allowed for the $+5V_{EXT}$ path amounts to 280 mA.

Additional information of the signals can be found in the phyCORE-MPC555 Hardware Manual and in the Motorola User's Manual MPC555.

2.7 Pinout of Connectors X2 and X3

Table 3 provides a pinout overview of the X2 connector located on the phyCORE-MPC555 Development Board. *Please refer to the phyCORE-MPC555 Hardware Manual (section 2, pin description) and the Motorola MPC555 User Manual/Data Sheet for details on the functions and features of controller signals and port pins.*

X2	Signal	X2	Signal	X2	Signal
1A	EXTCLK	1B	CLKOUT	1C	GND
2A	/IRQ1	2B	/IRQ3	2C	/IRQ2
3A	/IRQ0	3B	GND	3C	/CS2
4A	/CS3	4B	/CS1	4C	/CS0
5A	GND	5B	/OE	5C	/WE3
6A	A31	6B	A30	6C	GND
7A	A29	7B	A28	7C	A27
8A	A26	8B	GND	8C	A25
9A	A24	9B	A23	9C	A22
10A	GND	10B	A21	10C	A20
11A	A19	11B	A18	11C	GND
12A	A17	12B	A16	12C	D31
13A	D30	13B	GND	13C	D29
14A	D28	14B	D27	14C	D26
15A	GND	15B	D25	15C	D24
16A	A15	16B	A14	16C	GND
17A	A13	17B	A12	17C	A11
18A	A10	18B	GND	18C	A9
19A	A8	19B	D23	19C	D22
20A	GND	20B	D21	20C	D20
21A	D19	21B	D18	21C	GND
22A	D17	22B	D16	22C	/WE2
23A	/TA	23B	GND	23C	/TEA
24A	/BG	24B	/BB	24C	/BR
25A	GND	25B	D15	25C	D14
26A	D13	26B	D12	26C	GND
27A	D11	27B	D10	27C	D9
28A	D8	28B	GND	28C	D7
29A	D6	29B	D5	29C	D4
30A	GND	30B	D3	30C	D2
31A	D1	31B	D0	31C	GND
32A	47B	32B	48A	32C	48B

33A	49A	33B	GND	33C	50A
34A	50B	34B	TSIZ0	34C	TSIZ1
35A	GND	35B	/WE1	35C	/TS
36A	/WE0	36B	RDNWR	36C	GND
37A	/BDIP	37B	/IRQ4	37C	/BURST
38A	MODCK1	38B	GND	38C	MODCK2
39A	/BI / /STS	39B	MODCK3	39C	59A
40A	GND	40B	B_TPU15	40C	B_TPU14
41A	B_TPU13	41B	B_TPU12	41C	GND
42A	B_TPU10	42B	B_TPU11	42C	B_TPU8
43A	B_TPU9	43B	GND	43C	B_TPU7
44A	B_TPU6	44B	B_TPU5	44C	B_TPU4
45A	GND	45B	B_TPU2	45C	B_TPU3
46A	B_TPU0	46B	B_TPU1	46C	GND
47A	B_T2CLK	47B	A_T2CLK	47C	A_TPU15
48A	A_TPU14	48B	GND	48C	A_TPU12
49A	A_TPU13	49B	A_TPU10	49C	A_TPU11
50A	GND	50B	A_TPU9	50C	A_TPU8
51A	A_TPU7	51B	A_TPU6	51C	GND
52A	A_TPU4	52B	A_TPU5	52C	A_TPU2
53A	A_TPU3	53B	GND	53C	A_TPU1
54A	A_TPU0	54B	NC	54C	NC

Table 3: Pinout of the Development Board Connector X2

Table 4 provides a pinout overview of the X3 connector located on the phyCORE-MPC555 Development Board. *Please refer to the phyCORE-MPC555 Hardware Manual (section 2, pin description) and the Motorola MPC555 User Manual/Data Sheet for details on the functions and features of controller signals and port pins.*

X3	**Signal**	**X3**	**Signal**	**X3**	**Signal**
1A	+3V3	1B	+3V3	1C	+3V3
2A	GND	2B	GND	2C	+3V3
3A	+5V	3B	4D	3C	+5V
4A	VPD	4B	VBAT	4C	5D
5A	+3V3GOOD	5B	/PFI	5C	GND
6A	GND	6B	TEXP/ /RSTCNF	6C	/SRESET
7A	/PORESET	7B	/HRESIN	7C	/HRESET
8A	MPIO2	8B	GND	8C	MPIO14
9A	MPIO13	9B	MPIO10	9C	MPIO15
10A	MPIO8	10B	MPIO11	10C	GND

11A	GND	11B	RXD1_TTL	11C	MPIO9
12A	B_CANL	12B	B_CANH	12C	TXD1_TTL
13A	ECK	13B	GND	13C	MPIO7
14A	A_CANH	14B	RXD2	14C	A_CANL
15A	TXD2	15B	RXD1	15C	GND
16A	GND	16B	MPIO6	16C	TXD1
17A	QGPIO3	17B	QGPIO6	17C	QGPIO5
18A	QGPIO2	18B	GND	18C	QGPIO4
19A	MPIO5	19B	QGPIO0	19C	QGPIO1
20A	SGPIOC7	20B	MPIO4	20C	GND
21A	GND	21B	SGPIOc6	21C	SCL
22A	/IRTC	22B	DSDI	22C	SDA
23A	DSCK	23B	GND	23C	/TRST
24A	VFLS0	24B	TMS	24C	DSDO
25A	MPIO3	25B	VFLS1	25C	GND
26A	GND	26B	MPIO1	26C	MPIO12
27A	MDA7	27B	MPIO0	27C	MDA9
28A	MDA6	28B	GND	28C	MDA8
29A	MDA3	29B	MDA4	29C	MDA5
30A	MDA2	30B	MDA1	30C	GND
31A	GND	31B	MDA0	31C	MPWM7
32A	MPWM4	32B	MPWM5	32C	MPWM6
33A	MPWM1	33B	GND	33C	MPWM3
34A	VDDGOOD	34B	MPWM0	34C	MPWM2
35A	RXD2_TTL	35B	/VDDGOOD	35C	GND
36A	GND	36B	TXD2_TTL	36C	EPEE
37A	/WAKEUP	37B	B_CNTX0	37C	/PWRON
38A	A_CNTX0	38B	GND	38C	B_CNRX0
39A	ETRIG1	39B	A_CNRX0	39C	ETRIG2
40A	B_AD15	40B	B_AD14	40C	GNDA
41A	GNDA	41B	B_AD13	41C	B_AD12
42A	B_AD9	42B	B_AD10	42C	B_AD11
43A	B_AD6	43B	GNDA	43C	B_AD8
44A	B_AD5	44B	B_AD4	44C	B_AD7
45A	B_AD2	45B	B_AD3	45C	GNDA
46A	GNDA	46B	B_AD0	46C	B_AD1
47A	A_AD12	47B	A_AD15	47C	A_AD14
48A	A_AD11	48B	GNDA	48C	A_AD13
49A	A_AD8	49B	A_AD9	49C	A_AD10
50A	A_AD7	50B	A_AD6	50C	GNDA
51A	GNDA	51B	A_AD5	51C	A_AD4
52A	A_AD1	52B	A_AD2	52C	A_AD3

53A	VDDA	53B	GNDA	53C	A_AD0
54A	NC	54B	NC	54C	VRH

Table 4: Pinout of the Development Board Connector X3

3 Jumpers

To provide different signal configurations and operation modes, the phyCORE-MPC555 has 18 removable jumpers and 1 solder jumper. *Figure 9* illustrates the numbering of the jumper pads, while *Figure 10* shows the location of the jumpers on the board.

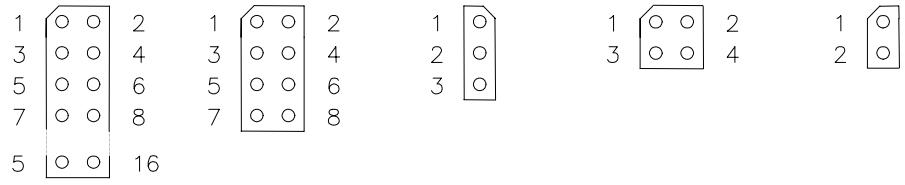


Figure 9: Numbering of the Jumper Pads

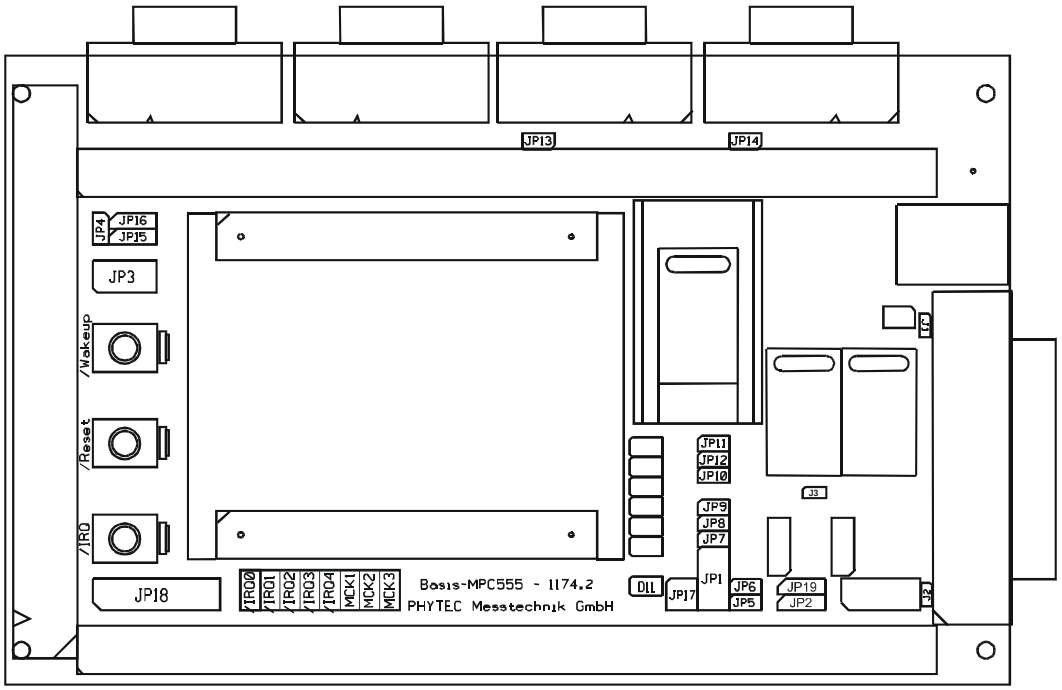


Figure 10: Location of the Jumpers (Top Side)

The jumpers are grouped by function as follows:

- BDM interface related jumpers:
  JP1, JP2, JP5 to JP9, JP17, JP19

- supply voltage related jumpers:
  JP10 to JP12, J1

- interrupt push button related jumper:
  JP18

- reset push button related jumper:
  JP3

- target configuration jumpers:
  JP4, JP13, JP16

- CAN bus termination jumper:
  JP13 and JP14

3.1 JP1, JP2, JP5 to JP9, JP17, JP19 BDM Interface

Jumper	Default	Description
JP1		JP1 connects the BDM reset signal to one of the reset signals on the target module.
1 + 2		BDM reset signal to /PORESET
3 + 4	X	BDM reset signal to /HRESIN
5 + 6		BDM reset signal to /HRESET
7 + 8		BDM reset signal to /SRESET
JP2		Selection of the signal interface voltage to the target processor BDM interface.
1 + 2	X	Select 3.3 V BDM voltage
2 + 3		Select 5 V BDM voltage
JP5		JP5 connects the DSDI output signal of BDM logic to the target DSDI signal.
closed	X	
JP6		JP6 connects the DSCK output signal of BDM logic to the target DSCK signal.
closed	X	The target stops always in debug mode after RESET.
open		The target runs in normal mode after RESET.
JP7		JP7 connects the VFLS0 output signal of the target to the BDM logic.
closed	X	
JP8		JP8 connects the VFLS1 output signal of the target to the BDM logic.
closed	X	
JP9		JP9 connects the DSD0 output signal of the target to the BDM logic.
closed	X	
JP17		JP17 connects /HRESET or /SRESET to the BDM interface logic. This is used to read the reset status from the debugger.
1 + 2	X	/HRESET is attached to the BDM interface logic.
3 + 4		/SRESET is attached to the BDM interface logic.

Jumper	Default	Description
JP19		JP19 has been added because some PC printer ports leave their signal lines at an undefined state after releasing the debugger. This feature may be used to hold the target running while terminating the debugger.
1 + 2		Disconnects the reset line of the target from the BDM interface if the debugger on the host-PC is terminated.
2 + 3	X	Static connection of the target's reset line to the BDM interface and to the host-PC's printer port.

Table 5: BDM Interface Jumpers

Attaching an external BDM interface via header X4

To connect an external BDM interface via pin header X4, jumpers JP1, as well as JP5 to JP9 must be removed. Select the appropriated BDM supply voltage with JP2 or remove it. Some BDM interfaces provide their own power supply and do not need the supply voltage from the Development Board. *Refer to section 2.5 for detailed information.*

3.2 JP3 Reset Push Button S2

Jumper	Default	Description
JP3		JP3 connects push button S2 to different reset signals.
1 + 2	X	Connects /HRESIN to push button S2.
3 + 4		Connects /HRESET to push button S2.
5 + 6		Connects /SRESET to push button S2.
7 + 8		Connects /PORESET to push button S2.

Table 6: JP3 Reset Push Button Configuration

It is not allowed to close more than one jumper at the same time.

3.3 JP4, JP15, JP16 Target Configuration

Jumper	Default	Description
JP4		JP4 enables programming of the internal Flash memory of the MPC555. JP4 controls the phyCORE signal EPEE at X1D53.
open		Programming of the internal MPC555 Flash memory is disabled (EPEE=low) and the supply voltage of the Flash module is reduced to 3.3 V.
closed	X	Programming of the internal MPC555 Flash memory is enabled (EPEE=high) and the supply voltage of the Flash module is increased to 5 V.
JP15		JP15 selects the memory that is used to boot the phyCORE-MPC555. JP15 is connected to data line D20. During hard-reset D20 controls the FLEN bit in the Hard Reset Configuration Word. For proper operation, Jumper J1 on phyCORE-MPC555 must be removed.
open		Boot memory selected with Jumper J1 on the phyCORE-MPC555
1 + 2	X	Boot from internal Flash memory.
2 + 3		Boot from external Flash memory.
JP16[1]		JP16 controls the capability to select the source of Hard Reset Configuration Word for the phyCORE-MPC555.
open	X	Source of the Hard Reset Configuration Word selected with Jumper J5 on the phyCORE-MPC555
1 + 2		Enables Hard Reset Configuration from internal source.
2 + 3		Enables Hard Reset Configuration from external source.

Table 7: JP4, JP15, JP16 Target Configuration Jumpers

1: **Caution:** JP16 does not work with the current phyCORE-MPC555 PCB revision and should be removed. External or internal Reset Configuration Word must be configured on the phyCORE-MPC555.

3.4 JP10 to JP12, J1 Supply Voltages

These jumpers can be used to open the power paths in order to connect a current meter into the corresponding supply path.

Caution:
Do not supply the system if any of these jumpers are open.

Jumper	Default	Description
JP10 closed	X	JP10 connects the +5 V_{EXT} supply voltage to the I/O-Connector VG1. LED D8 is connected to this voltage.
J1 closed open	 X	This is a solder jumper! +5 V_{EXT} is controlled by the target signal /PWRON. /PWRON is always active if the target is not in power-down mode. If the target is in power-down mode, /PWRON goes inactive and switches off the +5 V_{EXT} voltage. LED D8 is then turned off. +5 V_{EXT} is constantly attached to the I/O connector VG1 (i.e. FET T1 is bypassed)
JP11 closed	X	JP11 connects the +5 V supply voltage to the target module. LED D9 is connected to this voltage and illuminates regardless of the target power-down mode.
JP12 closed	X	JP12 connects the +3V3 supply voltage to the target module. LED D10 is connected to this voltage and illuminates regardless of the target power-down mode.

Table 8: J1, JP10, JP11, JP12 Supply Voltage Configuration

3.5 JP18 Interrupt Push Button S5

Each of the interrupt inputs of the target can be connected to push-button S5. This allows to generate an external interrupt in order to test interrupt service routines. It is possible to close more than one jumper at the same time, i.e. to connect push-button S5 to multiple interrupts.

Jumper	Default	Description
JP18		JP18 connects push button S5 to an interrupt input of the target.
1 + 2	X	Connects /IRQ0 to push button S5.
3 + 4		Connects /IRQ1 to push button S5.
5 + 6		Connects /IRQ2 to push button S5.
7 + 8		Connects /IRQ3 to push button S5.
9 + 10		Connects /IRQ4 to push button S5.
11 + 12		Connects /IRQ5 (MODCK1) to push button S5.
13 + 14		Connects /IRQ6 (MODCK2) to push button S5.
15 + 16		Connects /IRQ7 (MODCK3) to push button S5.

Table 9: JP18 Interrupt Push Button Configuration

/IRQ5 to /IRQ7 are double action inputs. While /PORESET is active, the target processor reads the status of these signals to determine the default clock operating mode. Ensure that push button S5 is not pressed while /PORESET is active if Jumper JP18 is closed at 11+12, 13+14 or 15+16, i.e. ensure that signals connected to /IRQ5 to /IRQ7 remain in tri-state while /PORESET is active.

3.6 JP13, JP14 CAN Bus Termination

Jumper	default	Description
JP13/JP14		JP13 and JP14 are used to terminate the CAN busses with terminating resistor of 120 Ohm. Terminating both ends of a CAN bus system is essential for proper CAN signal transmission. The termination jumper should only be closed, if the CAN node is at the end of the CAN bus.
JP13 closed	X	JP13 connects a terminating resistor to the CAN bus A signals CANH and CANL at DB-9 connector P4.
JP14 closed	X	JP14 connects a termination resistor to the CAN bus B signals CANH and CANL at DB-9 connector P5.

Table 10: JP13, JP14 CAN Bus Termination Configuration

3.7 Default Jumper Configuration Overview

Figure 11 depicts the default jumper configuration. The on-board BDM interface logic is active and holds the phyCORE-MPC555 in debug mode after any reset. In debug mode the CPU is stopped and the red LED D11 illuminates. To start the phyCORE after any reset in normal mode, remove JP6.

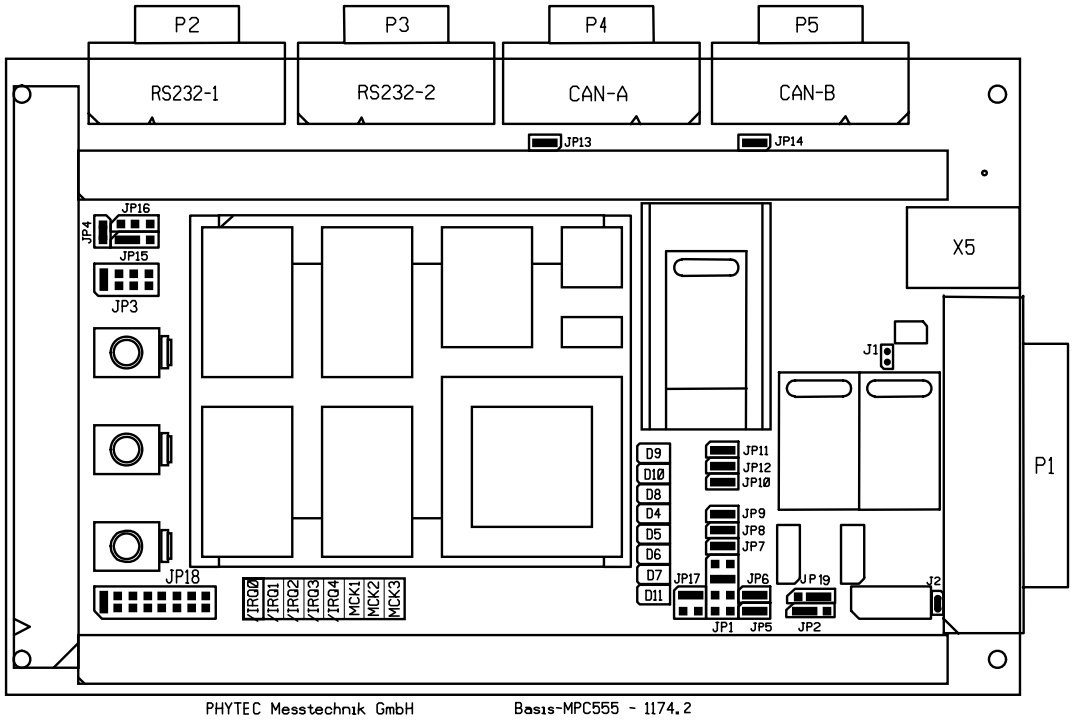


Figure 11: Default Jumper Configuration

4 Technical Specifications

The physical dimensions of the Development Board are represented in *Figure 12*.

The maximum height of all components and the inserted phyCORE module above the top side of the PCB is ca. 16 mm. The profile of the underside of the Development Board is ca. 3 mm. The PCB itself is approximately 1.6 mm thick.

It is not possible to insert the device in a 19" chassis because of the DB-9 connectors populating the upper long side of the Development Board.

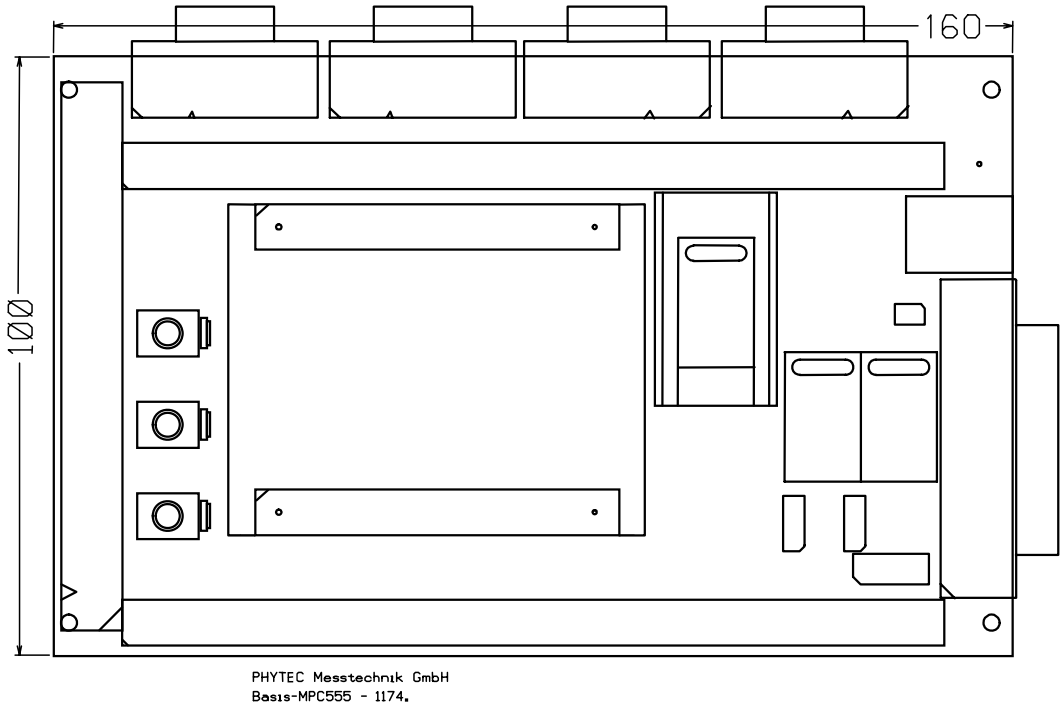


Figure 12: Physical Dimensions

Additional specifications:

- Dimensions: 160 mm x 100 mm
- Weight: approximately 170 g
- Storage temperature: -40°C to +90°C
- Operating temperature: 0°C to +70°C
- Humidity: 95 % r.F. not condensed
- Operating voltage: 7 VDC – 12 VDC supplied via power jack or terminal block,
- Power consumption: for all peripheral components without an implemented phyCORE module ca. 50 mA, 350mA to 650mA with phyCORE module installed

These specifications describe the standard configuration of the Development Board as of printing of this manual.

Please note that the storage temperature is only 0°C to +70°C, if a phyCORE module with a battery buffer for the RAM device and the Real-Time Clock populates the Development Board.

5 Revision History

Date	Version numbers	Changes in this manual
11-Apr-2000	Manual L-525e_1 PCM-995 PCB# 1174.0	First edition.
13-Nov-2000	Manual L-525e_2 PCM-995 PCB# 1174.0	Minor revisions regarding spelling errors and conventions.
2-Aug-2001	Manual L-525e_3 PCM-995 PCB# 1174.0	Section *Release Notes* added.
28-Oct-2003	Manual L-525e_4 PCM-995 PCB# 1174.0	Pin assignment in section *2.5* corrected. New paragraph added in section *Release Notes*.
27-Feb-2004	Manual L-525e_5 PCM-995 PCB# 1174.2	Description modified to match new PCB revision 1174.2. Section *2.1.1*, power supply properties added. Sections *2.5* (*10-pin Header X4 – External BDM Interface*) and *2.7* (*Pinout of Connectors X2 and X3*) added. In section *3.1*, JP19 added. Applicable new paragraphs added in section *Release Notes*.
3-Aug-2006	Manual L-525e_5 PCM-995 PCB# 1174.2	Error in *Table 4*, Pin 8 signal corrected. Error in *Figure 11*, Jumper settings corrected.

Appendices A

A.1 Release Notes

The following section contains information about deviations to the description in this manual.

General

- Push button S5 - /IRQ5 (MODCK1)
  /IRQ5 (MODCK1) is only accessible if R37 located at the phyCORE-MPC555 is removed.

PCB 1174.0

- VG1B Pin 35 (B_CNRX0) is not connected. In the next revision the B_CNRX0 signal will be connected to this pin.

PCB 1174.1

- Short circuit between connector P1 pin 7 and X2 pin 29B resp. X1 pin 43B found in schematics. All delivered units have been manually reworked to correct that problem.

PCB 1174.2

- Signal B_CNRX0 is connected to VG1 at pin 35 (3B)
- Some BDM related circuitry has been added: pull-up resistor at connector P1 pin 13; advanced reset handling (JP19, U6 etc.)
- Pin assignment of X4 is changed at pin 2 (/SRESET) and pin 7 (/HRESET)

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Document: Development Board for phyCORE-MPC555
Document number: L-525e_6, August 2006

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