PHYTEC

phyCORE-PXA255

Hardware Manual

Edition June 2005

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Preface

This phyCORE-PXA255 Hardware Manual describes the board's design and functions. Precise specifications for the Intel PXA255 microcontroller series can be found in the enclosed PXA255 microcontroller Data-Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /OE). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration regarding Electro Magnetic Conformity of the PHYTEC phyCORE-PXA255

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Note:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

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Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-PXA255 is one of a series of PHYTEC Single Board Computers that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports common 8-, 16- and selected 32-bit controllers on two types of Single Boards Computers:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform
(2) as insert-ready, fully functional micro-, mini- and phyCORE OEM modules, which can be embedded directly into the user's peripheral hardware, design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market.

1 Introduction

The phyCORE-PXA255 belongs to PHYTEC's phyCORE Single Board Computer module family. The phyCORE SBCs represent the continuous development of PHYTEC Single Board Computer technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a sub-miniature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments the phyCORE board design features an increased pin package. The increased pin package allows dedication of approximately 20 % of all pin header connectors on the phyCORE boards to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD and laser-drilled Microvias components are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCORE-PXA255 is a subminiature (70 x 57 mm) insert-ready Single Board Computer populated with Intel's Xscale PXA255 microcontroller. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to high-density (0.635 mm) Molex pin header connectors aligning two sides of the board, allowing it to be plugged like a "big chip" into a target application.

Precise specifications for the controller populating the module can be found in the applicable controller User's Manual or Data Sheet. The descriptions in this manual are based on the PXA255 controller. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCORE-PXA255.

The phyCORE-PXA255 offers the following features:

- Single Board Computer in subminiature form factor (70 x 57 mm) according to phyCORE specifications
- all applicable controller and other logic signals extend to two high-density 160-pin Molex connectors
- processor: Intel XScale PXA255, max. 400 MHz clock

- **PXA255 Core Features:**

  - 32-bit ARM™ Core Version 5TE ISA compilant
    - ARM thumb instruction support
    - ARM DSP enhanced instructions

  - Intel Media Processing Technology
    - Enhanced 16-bit multiply
    - 40-bit accumulator

  - 32 kB data und 32 kB instructions cache
  - 2 kB mini data und 2 kB mini instructions cache
  - Instructions and Data Memory Management Unit
  - Branch target buffer
  - Debug Capability via JTAG Port
  - 0-400 MHz CPU speed
  - Low-power consumption and high performance

- **PXA255 System Features:**

  - Memory controller with DMA
    - 4 * SDRAM 64 MB each
    - 6 * SRAM, FLASH ROM (4 of which sync.)

  - Clock and Power Controllers
  - USB Client Interface
  - 2 * PCMCIA / Compact Flash
  - 2 * MMC card resp. SD card
  - LCD controller
  - AC97 / I²C controller
  - 4 UARTs
  - Synchronous Serial Protocol ports (SSP and NSSP)
  - I²C interface
  - 2 * PWM
  - RTC
  - OS timer
  - General purpose I/O pins (GPIO)
  - Interrupt control

- **phyCORE-PXA255 Memory Configuration[1]:**

  - SDRAM: 64 MByte (128 MByte) 32-bit 100 MHz
  - Flash-ROM: 32 MByte (8 MByte, 16 MByte, 64 MByte) synchronous/ asynchronous 32-bit (16-bit)
  - I²C EEPROM 4 kByte

1 Please contact PHYTEC for more information about additional module configuration options.

- **phyCORE-PXA255 Features:**

  - Power supply for PLL and core voltage
  - Core power control via 10-bit DAC
  - Reset control for module and periphery ICs
  - MCP2515 CAN controller
  - 10/100Mbps LAN91C111 Ethernet controller, 32-bit
  - Configuration storage EEPROM for Ethernet controller
  - Full-speed USB-OTG controller ISP1361
  - MAX7301 GPIO expander
  - Full RS-232 transceiver for FF-UART
  - Real-Time Clock RTC8564 with wakeup function
  - external battery backup for RTC
  - 2.0 mm JTAG port on module edge
  - Multi-Media card connector
  - Two indicator LEDs for system information
  - All required Chip Select signals and interrupts can be configured via jumpers on the module

- **phyCORE-PXA255 Operating Systems (examples):**

  - Linux
  - Win CE
  - QNX
  - PXROS (HighTec)

- **phyCORE-PXA255 Debugging Systems (examples):**

  - iSYSTEM: iC3000 Active Emulator™
  - HITEX: Tantino Xscale

1.1 Block Diagram

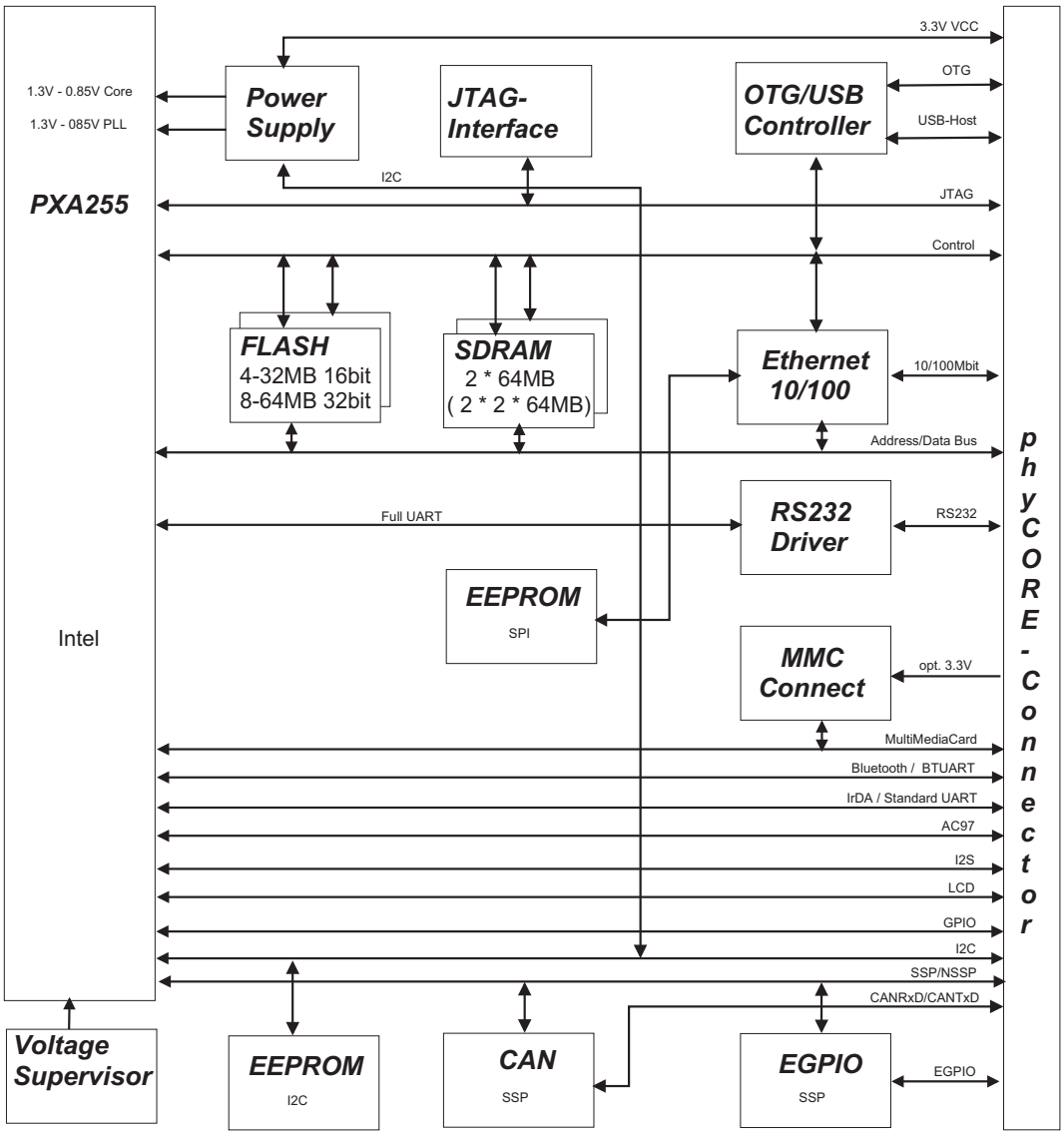

Figure 1: Block Diagram phyCORE-PXA255

1.2 View of the phyCORE-PXA255

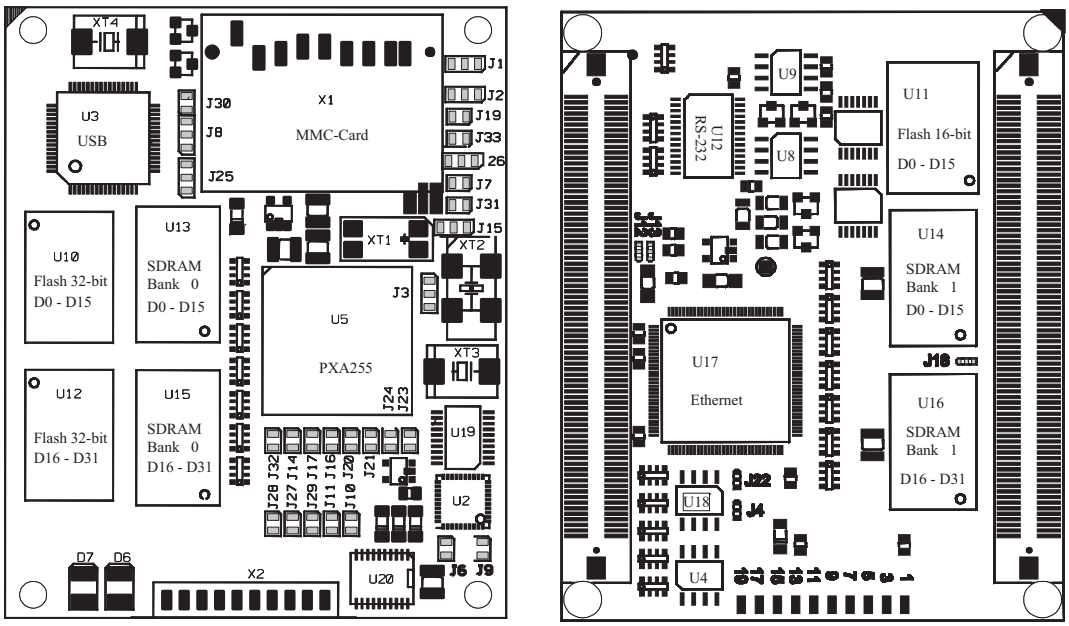

Figure 2: View of the phyCORE-PXA255, PCB Revision 1219.3

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 3* indicates, all controller signals extend to surface mount technology (SMT) connectors (0.635 mm) lining two sides of the module (referred to as phyCORE-connector). This allows the phyCORE-PXA255 to be plugged into any target application like a "big chip".

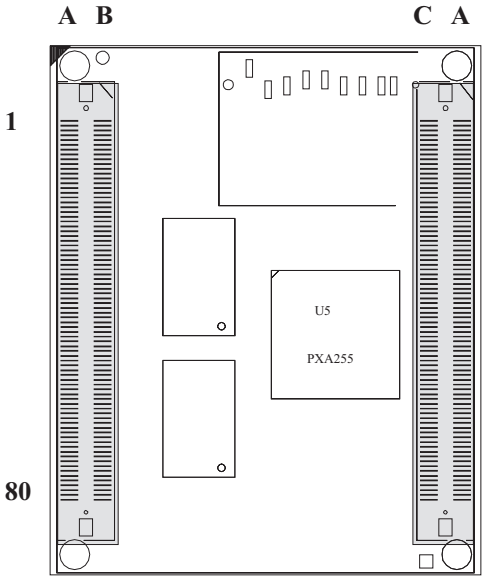

Figure 3: Pinout of the phyCORE-PXA255 (TOP View)

Many of the controller port pins accessible at the edges of the board have been assigned alternate functions that can be activated via software.

Table 1 provides an overview of the pinout of the phyCORE-connector , as well as descriptions of possible alternative functions. *Please refer to the Intel PXA255 Elctrical, Mechanical and Thermal Specification for details on the functions and features of controller signals and port pins.*

Pin Number	Signal	I/O	Comments
Pin Row X1A			
1A	CLKIN	I	Optional external clock input of the processor
2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A	GND	-	Ground 0 V
3A	GPIO2	I/O	Processor I/O port, *alternative: interrupt*
4A	GPIO0	I/O	Processor I/O port, *alternative: interrupt*
5A	/CS_2	I/O	Freely available /CS signal of the processor, *alternative: GPIO78*
6A	/CS_4	I/O	Chip Select signal of the processor, can be used to access the USB controller, *alternative: GPIO80*
8A	/WE	O	Write-enable signal for SDRAM, SRAM and Flash devices. Please note that the /PWE signal must be used for I/O components.
9A, 10A, 11A, 13A, 14A, 15A, 16A, 18A, 24A, 25A, 26A, 28A, 36A	A1, A2, A4, A7, A9, A10, A12, A15, A17, A18, A20, A23, A24	I/O	Address lines
19A, 20A, 21A, 23A, 29A, 30A, 31A, 33A, 38A, 39A, 40A, 41A, 43A, 44A, 45A, 46A	D1, D2, D4, D7, D9, D10, D12, D15, D18, D19, D20, D22, D25, D27, D28, D30	I/O	Data lines
34A, 35A	DQM_1, DQM_2	O	Byte enable signals
48A	RDY	I/O	Ready signal of the processor, *alternative: GPIO 18*
49A	RDnWR	O	Bus control singal of the processor

Pin Number	Signal	I/O	Comments
Pin Row X1A			
50A, 51A	DREQ_0 DREQ_1	O	DMA request singal DREQ0 *alternative: GPIO 20* DREQ1 *alternative: GPIO 19*
53A, 54A	/SDCKE_0 /SDCKE_1	O	Clock enable for synchronous memory
55A, 56A	/SDCLK_0 /SDCLK_1	O	Clock signal for synchronous memory
58A, 59A	/PCE_1 /PCE_2	I/O	PCMCIA Chip Select resp. byte control signal, *alternative: GPIO52/53*
60A	/PWAIT	I/O	PCMCIA wait signal, *alternative: GPIO56*
61A	/IOIS16	I/O	PCMCIA 16-bit access *alternative: GPIO57*
63A	/PREG	I/O	PCMCIA register control signal *alternative: GPIO55*
64A	/LAN_CS	I	I/O Chip Select for LAN controller
65A	/LAN_DATA	I	DATA Chip Select for LAN controller
66A	LAN_RDY	O	Ready output of LAN controller
68A	L_PCLK	I/O	LCD pixel clock *alternative: GPIO76*
69A	L_LCLK	I/O	LCD line clock *alternative: GPIO75*
70A	L_FCLK	I/O	LCD frame clock *alternative: GPIO74*
71A	L_BIAS	I/O	LCD enable *alternative: GPIO77*
73A, 74A, 75A, 76A, 78A, 79A, 80A	L_DD3, L_DD5 L_DD6, L_DD8, L_DD11, L_DD13 L_DD14	I/O	LCD data *alternative: GPIO61, GPIO63, GPIO64, GPIO66, GPIO69, GPIO71, GPIO72*
Pin Row X1B			
1B	DEV_RES	I	Reset for USB, CAN and Ethernet Device only
2B	GPIO_3	I/O	Processor I/O port, *alternative: interrupt*
3B	GPIO_1	I/O	Processor I/O port, *alternative: interrupt*
4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B	GND	-	Ground 0 V
5B	/CS_3	I/O	Freely available /CS signal of the processor, *alternative: GPIO79*

Pin Number	Signal	I/O	Comments
Pin Row X1B			
6B	/CS_5	I/O	Chip Select signal of the processor, can be used to access the LAN controller, *alternative: GPIO33*
7B	/OE	O	Output-enable signal of the processor
8B, 10B, 11B, 12B, 13B, 15B, 16B, 17B, 23B, 25B, 26B, 27B 36B	A0, A3, A5, A6, A8, A11, A13, A14, A16, A19, A21, A22, A25	I/O	Address lines
18B, 20B, 21B, 22B, 28B, 30B, 31B, 32B, 37B, 38B, 40B, 41B, 42B, 43B, 45B, 46B	D0, D3, D5, D6, D8, D11, D13, D14, D16, D17, D21, D23, D24, D26, D29, D31	I/O	Data lines
33B, 35B	DQM_0, DQM_3	O	Byte enable signals
47B	/CS_0	O	Chip Select for on-board Flash
48B	/CS_1	I/O	/CS-Signal for second on-board 16-bit Flash, *alternative: GPIO15*
50B 51B 52B 53B	/SDCS_0 /SDCS_1 /SDCS_2, /SDCS_3	O	/CS SDRAM bank #0 /CS SDRAM bank #1 /CS SDRAM bank #2 /CS SDRAM bank #3
55B	/SDCLK_2	O	Clock signal for synchronous memory
56B	/SDRAS	O	/SDRAS control signal for SDRAM
57B	/SDCAS	O	/SDCAS control signal for SDRAM
58B	/PKSEL	I/O	Card0/1 select *alternative: GPIO 54*
60B	/PWE	I/O	PCMCIA memory write signal and I/O write signal *alternative: GPIO 49*
61B	/POE	I/O	PCMCIA memory read signal *alternative: GPIO 48*
62B	/PIOR	I/O	PCMCIA I/O write signal *alternative: GPIO 50*
63B	/PIOW	I/O	PCMCIA I/O read signal *alternative: GPIO 51*
65B	/LAN_IRQ	I/O	Interrupt LAN controller
66B	/OTG_CS	I	/CS signal for USB controller (PXA /CS_2 or /CS_4)
67B	/OTG_INT1	I	Interrupt /INT1 signal USB controller
68B	/OTG_INT2	I	Interrupt /INT2 signal USB controller

Pin Number	Signal	I/O	Comments
Pin Row X1B			
70B, 71B, 72B, 73B, 75B, 76B 77B, 78B 80B	L_DD0, L_DD1, L_DD2, L_DD4, L_DD7, L_DD9, L_DD10, L_DD12, L_DD15	I/O	LCD data bus *alternative: GPIO 58, GPIO 59, GPIO 62, GPIO 65, GPIO 67, GPIO 68, GPIO 70, GPIO 73*
Pin Row X1C			
1C, 2C	+3V3	P	Supply voltage +3.3 VDC
3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C 72C, 77C	GND	P	Ground 0 V
4C	VMMC	P	Optional supply voltage for internal MMC card
5C	VBAT	P	Input for external battery
6C	OTG_5V	I	USB Controller VDD_5V Pin
8C, 9C	/H_OC1, /H_OC2	I	USB Controller Over Current Inputs Cannel 1 /2
10C	/RESIN	I/O	/Reset input for reset controller at U9
11C	/RESET_OUT	I/O	/Reset output of the PXA255 processor
13C	NSSP_TxD	I/O	Network SPI TxD signal, used for CAN Controller *Alternative: GPIO 83*
14C	NSSP_CLK	I/O	Network SPI Clock signal *Alternative: GPIO 81*
15C	NSSP_RxD	I/O	Network SPI RxD signal *Alternative: GPIO 84*
16C	NSSP_FRM	I/O	Network SPI Frame signal, used for CAN Controller *alternative: GPIO 82*
18C	IR_TXD	O	IrDA TxD *Alternative: GPIO 47*
19C	IR_RXD	I	IrDA RxD *Alternative: GPIO 46*
20C	FF_RI_DETECT	O	RI-Detect FF-UART (for interrupt)
21C	FF_/INVALID	O	Invalid level FF_UART
23C	/ACRESET	O	/RESET AC97
24C	SYNC	I/O	SYNC AC97 *Alternative: GPIO 31*

Pin Number	Signal	I/O	Comments
Pin Row X1C			
25C	BITCLK	I/O	BITCLK *Alternative: GPIO 28*
26C	SDATA_IN_1	I/O	SDATA_IN1 (AC97 interface) *Alternative: GPIO 32*
28C	SDATA_IN_0	I/O	SDATA_IN0 (AC97 interface) *Alternative: GPIO 29*
29C	SDATA_OUT	I/O	SDATAOUT *Alternative: GPIO 30*
30C	SDA	I/O	I^2C data from processor
31C	SCL	I	I^2C clock from processor
33C	/LAN_LED_A-	O	LED A LAN controller, freely configurable
34C	/LAN_LED_B	O	LED B LAN-Controller, freely configurable
35C	LAN_TPI-	O	LAN negativer input
36C	LAN_TPO-	O	LAN negativer output
38C	OTG_ID	I	OTD ID Input USB Controller
39C	PWM0	O	PWM output #0 *Alternative: GPIO 16*
40C	PWM1	O	PWM output #1 *Alternative: GPIO 17*
41C	/TRST	O	JTAG reset
43C	H_DP2	IO	USB H_DP2
44C	H_DM2	IO	USB H_DM2
45C	MMC_CS_1	O	MMC_C1 for external MMC card *Alternative: GPIO 8*
46C	MMC_CS_0	O	MMC_C0 for internal MMC card *Alternative: GPIO 9*
48C, 49C, 50C, 51C, 53C	GPIO4, GPIO7 GPIO10, GPIO12, GPIO21	I/O	GPIOs *Alternative: interrupt signals*

Pin Number	Signal	I/O	Comments
Pin Row X1C			
54C, 55C, 56C, 58C, 59C, 60C, 61C, 63C, 64C, 65C, 66C, 68C, 69C, 70C, 71C	EGPIO0, EGPIO1, EGPIO3, EGPIO6, EGPIO8, EGPIO9, EGPIO11, EGPIO14, EGPIO16, EGPIO17 EGPIO18, EGPIO22, EGPIO24, EGPIO25, EGPIO27	I/O	Additional GPIOs generated by the MAX7301 IC
73C	SSP_RXD	I	SPI RxD signal
74C	SSP_TXD	O	SPI TxD signal
75C	/CS_EGPIO	I	SSP /CS1 signal for MAX7301 (EGPIO)
76C	/CAN_CS	I	NSSP /CS2 signal for MCP2515 (CAN)
78C	/CAN_INT	O	CAN Interrupt
79C	CANRXD	I/O	CAN RxD signal
80C	CANTXD	I/O	CAN TxD signal
Pin Row X1D			
1D, 2D	VCC	I	Supply voltage +3.3 VDC
3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D, 74D, 79D	GND	-	Ground 0 V
4D, 5D	VCC1	I	Optional external supply voltage VCORE for processor, 3-5.0V
6D	OTG_VBUS	IO	USB Controller VBUS signal
7D	/H_PSW1	O	USB Controller Power Switch 1 signal
8D	/H_PSW2	O	USB Controller Power Switch 1 signal
10D	/RESET	O	Reset output from reset controller
11D	/BATT_FAULT	I	Low battery voltage indication
12D	/VCC_FAULT	I	Low supply voltage indication
13D	PWR_ENAB	O	Power Enable PXA255
15D	BT_CTS	I	CTS Bluetooth UART *Alternative: GPIO 44*
16D	BT_RXD	I	RXD Bluetooth UART *Alternative: GPIO 42*

Pin Number	Signal	I/O	Comments
Pin Row X1D			
17D	BT_TXD	O	TXD Bluetooth UART *Alternative: GPIO 43*
18D	BT_RTS	O	RTS Bluetooth UART *Alternative: GPIO 45*
20D	FF_/SHDN	I	FF-UART power on
21D	FL_WP_PEN	I	Flash Write Protect
22D	RS_RXD	I	FF-UART RxD signal (RS-232)
23D	RS_TXD	O	FF-UART TxD signal (RS-232)
25D	RS_RTS	I	FF-UART RTS signal (RS-232)
26D	RS_CTS	I	FF-UART CTS signal (RS-232)
27D	RS_DSR	I	FF-UART DSR signal (RS-232)
28D	RS_DTR	O	FF-UART DTR signal (RS-232)
30D	RS_RI	I	FF-UART RI signal (RS-232)
31D	RS_DCD	I	FF-UART DCD signal (RS-232)
32D	USB_P	I/O	USB Client positive, from processor
33D	USB_N	I/O	USB Client negative, from processor
35D	LAN_TPI+	O	LAN input positive
36D	LAN_TPO+	O	LAN output positive
37D	OTG_DP1	I/O	USB Controller OTG_DP1
38D	OTG_DM1	I/O	USB Controller OTG_DM1
40D	TDI	I	JTAG TDI signal
41D	TDO	O	JTAG TDO signal
42D	TMS	I	JTAG TMS signal
43D	TCK	I	JTAG TCK signal
45D	MMC_CLK	I/O	MMC_CLK signal
46D	MMC_DAT	I/O	MMC_DAT signal
47D	MMC_CMD	I/O	MMC_CMD signal
48D, 50D, 51D, 52D, 53D	GPIO5, GPIO11, GPIO13, GPIO14, GPIO22,	I/O	GPIOs, *alternative: interrupt signals*
55D, 56D, 57D, 58D, 60D, 61D, 62D, 63D, 65D, 66D, 67D, 68D, 70D	EGPIO2, EGPIO4, EGPIO5, EGPIO7 EGPIO10, EGPIO12, EGPIO13, EGPIO15, EGPIO19, EGPIO20, EGPIO21, EGPIO23, EGPIO26	I/O	Additional GPIOs generated by the MAX7301 IC with 7 interrupt-capable inputs for connection to a matrix keyboard

Pin Number	Signal	I/O	Comments
Pin Row X1D			
71D	SSP_EXTCLK	I	SPI external clock *alternative: GPIO 27*
72D	SSP_CLK	O	SPI clock signal *alternative: GPIO 23*
73D	SSP_SFRM	I/O	SPI frame signal *alternative: GPIO 24*
75D	FL_DIS	I	Signal to disable internal Flash
76D	H_SUSWKUP	I/O	USB controller /H_SUSWKUP
77D	D_SUSWKUP	I/O	USB controller /D_SUSWKUP
78D	OTG_LED	I/O	USB controller LED signal
80D	/INT_RTC	O	Interrupt output RTC

Table 1: Pinout of the phyCORE-Connector X1

The section *"Initialization of the phyCORE-PXA255"* shows all GPIO signals and their default settings.

3 Jumper

For configuration purposes, the phyCORE-PXA255 has 32 solder jumpers, some of which have been installed prior to delivery. *Figure 4* illustrates the numbering of the jumper-pads, while *Figure 5* and *Figure 6* indicate the location of the jumpers on the board.

Figure 4: Numbering of the Jumper Pads

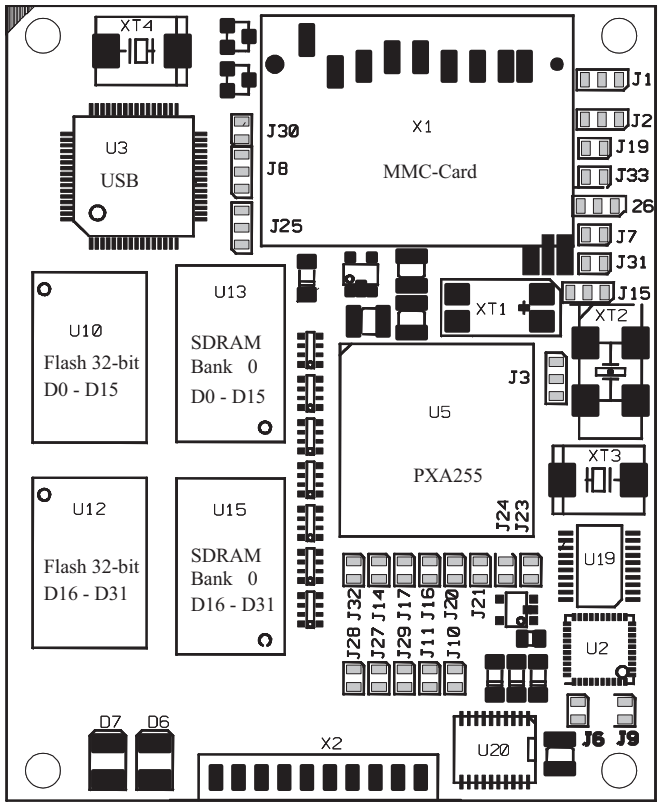

Figure 5: Location of the Jumpers (Controller Side)

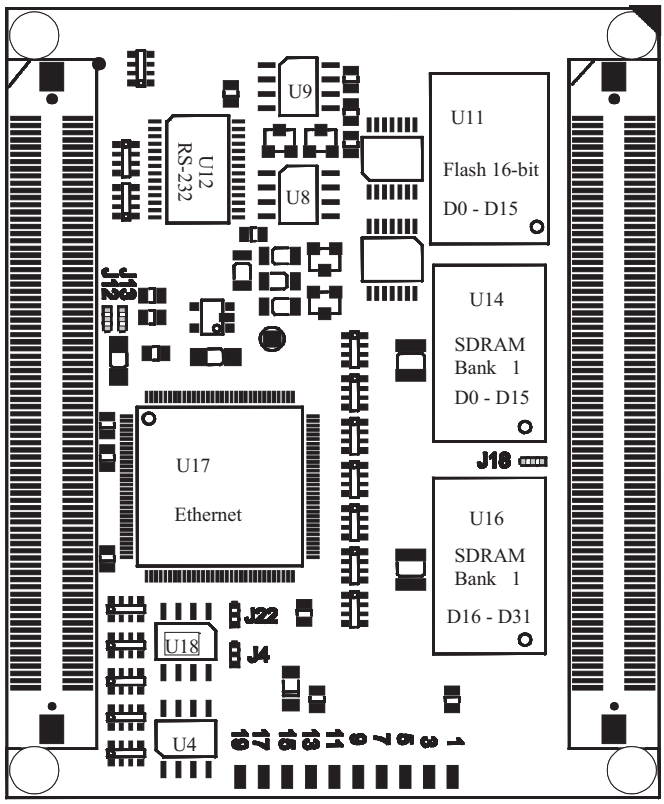

Figure 6: Location of the Jumpers (Connector Side)

The jumpers (J = solder jumper) have the following functions:

Jumper	Default	Comment
J1		This jumper configures the supply voltage for the on-board MM card.
1 + 2	X	MM card supplied via VCC.
2 + 3		MM card supplied externally via VMMC.
Package Type		0R in SMD 0805
J2		This jumper configures the supply input voltage for the voltage regulator generating the VCORE voltage.
1 + 2	X	Voltage regulator supplied by VCC.
2 + 3		Voltage regulator supplied by external VCC1.
Package Type		0R in SMD 0805
J3		This jumper configures the controller's clock source (3.686 MHz).
1 + 2		External clock connected to PXTAL.
2 + 3		External clock connected to PEXTAL.
open	X	Clock via on-board quartz at XT2.
Package Type		0R in SMD 0805
J4		This jumper configures the organization for the SPI EEPROM connected to the Ethernet controller.
1 + 2		Using an SPI EEPROM from another manufacturer.
2 + 3	X	Using an Atmel AT93C46 SPI EEPROM.
Package Type		0R in SMD 0805
J5		Vcore test jumper J1X1
Package Type		Pin only
J6		This jumper configures the SPI /CS signal for the MAX7301 GPIO expander controller.
closed		/CS signal for MAX7301 connected to GPIO22.
open	X	External /CS signal used for MAX7301, connected via phyCORE-Connector.
Package Type		0R in SMD 0805
J7		This jumper configures the MCC_WP signal
closed		MCC_WP signal for MM card connected to GPIO10.
open	X	MCC_WP signal for MM card is open
Package Type		0R in SMD 0805

Jumper	Default	Comment
J8		USB Controller OTG Mode
1 + 2	X	USB Controller Host Mode
2 + 3		USB Controller OTG Mode
open		External interrupt signal used for ADS7846, connected via phyCORE-Connector.
Package Type		0R in SMD 0402
J9		This jumper configures the interrupt signal for the MAX7301 GPIO expander controller.
1 + 2	X	Interrupt signal for MAX7301 connected to GPIO27.
open		External interrupt signal used for MAX7301, connected via phyCORE-Connector.
Package Type		0R in SMD 0805
J10/J11		These jumpers connect the I²C bus with the 24C08 I²C EEPROM at U4.
closed		On-board SDA and SCL signals connected to I²C EEPROM.
open	X	External SDA and SCL signals used for I²C EEPROM, connected via phyCORE-Connector.
Package Type		0R in SMD 0805
J12, J13, J15		These jumpers select the bus configuration of the PXA255 processor ('x' stands for closed, '0' for open).
		J12 J13 J15 bus interface
1+2|1+2|1+2	X	X X X 32-bit asynchronous Boot ROM
1+2|1+2| 0		X X 0 16-bit asynchronous Boot ROM
0 |1+2|1+2		0 X X 32-bit 2 * 16-bit sync. Boot ROM (32 MB)
0 |1+2| 0		0 X 0 16-bit synchronous Boot ROM (64 MB)
0 | 0|1+2		0 0 X 2* 16-bit synchronous Boot ROM (64 MB)
0 | 0| 0		0 0 0 32-bit asynchronous Boot ROM (64 MB)
Package Type		0R in SMD 0805 / 0402
J14		This jumper configures the interrupt 1 signal for the USB controller at U3.
closed	X	Interrupt signal for ISP1362 connected to GPIO3.
open		External interrupt signal used for ISP1362, connected via phyCORE-Connector.
Package Type		0R in SMD 0805

Jumper	Default	Comment
J16		This jumper configures the /CS signal for the LAN91C111 Ethernet controller at U17.
closed		/CS signal for LAN91C111 connected to /CS5 of the PXA255 processor.
open	X	External /CS signal used for LAN91C111, connected via phyCORE-Connector.
Package Type		0R in SMD 0805
J17		This jumper configures the Ready signal for the LAN91C111 Ethernet controller at U17.
closed		LAN_RDY signal from LAN91C111 connected to RDY input of the PXA255 processor.
open	X	LAN_RDY signal from LAN91C111 can be connected externally, available on phyCORE-Connector (X3A66).
Package Type		0R in SMD 0805
J18		Flash WP or PEN on FL_WP_PEN
1 + 2		FL_WP_PEN is /PEN
2 + 3	X	FL_WP_PEN is /WP
open		
Package Type		0R in SMD 0805
J19		USB Controller VDD_5V Input
closed		USB VDD_5V is VCC 3.3V
open	X	USB VDD_5V is connected externally
Package Type		0R in SMD 0805
J20		This jumper configures the Ethernet interrupt.
1 + 2	X	Ethernet interrupt is connectet to GPIO_2
open		Ethernet interrupt is connectet to external signal.
Package Type		0R in SMD 0805
J21		This jumper enables the Ethernet EEPROM.
closed	X	Ethernet EEPROM is enabled.
open		Ethernet EEPROM is disabled.
Package Type		0R in SMD 0805

Jumper	Default	Comment
J22		Ethernet /WE signal configuration
1 + 2	X	Ethernet /WE is connected to /PWE (VLIO interface) on the PXA255.
2 + 3		Ethernet /WE is connected to /WE (SRAM/ROM interface) on the PXA255.
Package Type		0R in SMD 0402
J23		Currently not used! This jumper connects the /CAN_CS signal to GPIO_84.
closed		/CAN_CS is connected with GPIO_84 (NSSP_TXD).
open	X	/CAN_CS needs to be connected externally.
Package Type		0R in SMD 0805
J24		This jumper connects the /CAN_INT signal to GPIO5.
closed	X	/CAN_INT is connected to GPIO5.
open		/CAN_INT needs to be connected externally.
Package Type		0R in SMD 0805
J25		USB controller /CS configuration
1 + 2		/OTG_CS is connected to /CS_2.
2 + 3	X	/OTG_CS is connected to /CS_4.
open		/OTG_CS is connected externally.
Package Type		0R in SMD 0805
J26		RS-232 transceiver FORCEON input configuration
1 + 2	X	RS-232 FORCEON is connected to GND (*see MAX3245EAI RS-232 transceiver data sheet for details*).
2 + 3		RS-232 FORCEON is connected to the FF_/INVALID signal.
Package Type		0R in SMD 0805

Jumper	Default	Comment
J27 / J28		LED configuration, red LED D6 connected to GPIO22, green LED D7 to GPIO21.
closed	X	LED D6 (red) is connected to GPIO22, D7 (green) to GPIO21.
open		LEDs not used.
Package Type		1kOhm in SMD 0805
J29		RTC interrupt configuration
closed	X	RTC interrupt is connected to GPIO_0.
open		RTC interrupt needs to be connected externally.
Package Type		0R in SMD 0805
J30		This jumper configures the Flash Reset.
closed	X	Flash Reset connected with DEV_RESET and /RESET
open		No Flash Reset
Package Type		0R in SMD 0805
J31		This jumper configures the MCC_DETECT signal
closed		MCC_DETECT signal for MMC-Card connected to GPIO_7.
open	X	MCC_DETECT signal for MMC-Card not connected.
Package Type		0R in SMD 0805
J32		This jumper configures the interrupt 2 signal for the USB controller at U3.
closed	X	Interrupt 2 signal for ISP1362 connected to GPIO_4.
open		External interrupt 2 signal used for ISP1362, connected via phyCORE-Connector.
Package Type		0R in SMD 0805
J33		This jumper configures the RS-232 transceiver's /FORCEOFF signal.
closed	X	
open		RS-232 transceiver /FORCEOFF signal is connect with FORCEON RS-232 transceiver /FORCEOFF signal is connected to external FF_/SHDN (phyCORE-Commector pin X3D20)
Package Type		0R in SMD 0805

Table 2: Jumper Settings

4 Power System and Reset Behavior

The phyCORE-PXA255 is only supplied with a single supply voltage. However it is possible to power the MMC card and the internal voltage regulator of the Vcore voltage externally.

Supply voltage 1: +3.3 V (VCC)
Supply voltage 2: +3.3 V (VCC1) optional
Supply voltage 3: +3.3 V (VMMC) optional

Caution!
The VMMC voltage cannot be connected without VCC being supplied at the same time.

Power-On Behavior

In the standard operating mode all of the module's components are supplied by a common 3.3 V (VCC) supply voltage. The chronological order for turning the individual voltages as well as the reset signal on is defined on the module. The data in SDRAM is not defined in the case of a power-on, which is why the system will always reboot and initialize the memory.

The voltage VMMC (if configured as an option) can be switched on or off while VCC is connected.

Power-Off Behavior

In the standard operating mode all components including the SDRAM are supplied by a common 3.3 V (VCC) supply voltage. If the VCC is switched off, the SDRAM will lose its data and the system will reboot with the next power-on. It is therefore recommended that the system is always supplied with the VCC voltage and that the power management features of the controller are used to conserve power.

Power Management

The power management is carried out on the module. The controller can switch the Vcore voltage regulator on or off indepently. Furthermore the controller offers a number of power saving possibilities. *For more on the power saving features refer to the PXA255 data sheets*.

Device Reset

A special DEV_RES input is provided on the phyCORE-PXA255 for resetting the Ethernet, CAN, USB and Flash devices without resetting the PXA255 controller. In the event of a /RESET the internal DEV_RES will also be released allowing all these components to get reset along with the PXA255 controller. RES_DEV can be used for power managment or in watchdog applications.

5 VCore Supply Voltage

The PXA255 processor requires a core voltage of 1.3 V which can be reduced to 1.1 V, 1 V or 0.85 V depending on the power management mode. The voltage regulator for the Vcore is located on the phyCORE-PXA255 at U6 and has over 90 % efficiency. The controller can turn the switching regulator on or off using the PWR_EN output. The input voltage of the regulator can be supplied with the VCC from the module or an external voltage via solder jumper J2. The external voltage regulator supply option should only be used during battery operation. The Vcore input voltage can then be generated directly from the battery voltage.

J2	Description
1 + 2	Input voltage for Vcore voltage regulator supplied by the on-board +3.3 V (VCC) operating voltage.
2 + 3	Input voltage for Vcore voltage regulator supplied by an external source ranging from +3.3 V to +5 V.

Table 3: Jumper J2 for Vcore Supply Voltage

The default value of the Vcore voltage following a hardware reset is 1.3 V. The voltage can be reduced to 0.845 V by using a 10-bit DAC, type LTC1663CS5. The Vcore voltage is reduced inversely proportional to the DAC voltage *(refer to Table 4)*. The voltage range of the DAC is 0 - 2.5 V.

DAC Voltage	Vcore Voltage
0 V	1.3 V
1,15 V	1.1 V
1,65 V	1.0 V
2.5 V	0.85 V (not used with PXA255)

Table 4: Vcore Voltage Range

6 System Memory

The controller PXA255 provides a configurable memory interface for:

- 4 * SDRAM with max. 64 MByte each
- 4 * asynchronous or synchronous ROM/Flash/RAM/IO with max. 64 MByte each
- 2 * asynchronous ROM/Flash/RAM/IO with max. 64 MByte each

The internal MMU and the configurable memory interface of the PXA255 processor enable it to adapt the memory model during runtime with the help of software. The configuration of the Boot-ROM can be set on the phyCORE module using solder jumpers (J12, J13, J14, *refer to section 3*).

6.1 Memory Model Following Reset

The memory model following a hardware reset only activates the controller's /CS0 signal. Access using this /CS signal is configured with the BOOT_SELx connection. Closing Jumpers J12, J13 or J14 connects the corresponding boot select signal BOOT_SEL0-2 to GND potential resulting in a low level being read by the PXA255 processor.

BOOT_SEL0 BOOT_SEL1 BOOT_SEL2	**J12**	**J13**	**J15**	**Default**	**Bus Interface Configuration for /CS0**
000	closed	closed	closed	**X**	32-bit asynchronous Boot ROM
001	closed	closed	open		16-bit asynchronous Boot ROM
100	open	closed	closed		32-bit 2+ 16-bit synchronous Boot ROM (32 MB)
101	open	closed	open		16-bit synchronous Boot ROM (64 MB)
110	open	open	closed		2*16-bit synchronous Boot ROM (64 MB)
111	open	open	open		32-bit synchronous Boot ROM (64 MB)

Table 5: Boot Configuration via BOOT_SELx Pins

After reset the memory range of /CS0 is pre-initialized to 64 MByte. Therefore all configuration options from 16 MByte to 64 MByte can be addressed with 2*16-bit Flash devices connected to /CS0. By default the access occurs with 32-bit data bus width in asynchronous mode. The Flash contains a boot loader starting at address 0x00000000 which performs all necessary initialization stepos for the PXA255 processor.

6.2 Runtime Memory Model with the U-Boot Loader

The runtime memory model is selected via software by configuring the internal registers of the PXA255 processor. The U-Boot loader, which belongs to the standard delivery package, configures the following memory model:

/CS0	2 * 16-bit Flash memory 16 to 64 MByte asynchronous or synchronous (optional 16-bit Flash memory 8 MByte async.)
/CS1	free (pre-configured for 16-bit asynchonous ROM/RAM)
/CS2	free (pre-configured for 16-bit VLIO interface)
/CS3	free (pre-configured for 32-bit VLIO interface)
/CS4	free or USB chip with 16-bit VLIO interface
/CS5	free or Ethernet chip with 32-bit VLIO interface
/SDCS0	64 MByte 2*16-bit SDRAM
/SDCS1	optional 64 MByte 2*16-bit SDRAM
/SDCS2	free (optional 256-MB Configuration)
/SDCS3	free (optional 256-MB Configuration)

The configuration can be adapted to user requirements during runtime with the exception of the SDRAM registers. The following table *Table 6* shows the default values for the /CS0... /CS5 signals of the PXA255 controller.

PXA255 Register	**Default Value**
MSC0	0x12CB 12C3
MSC1	0x128C 128C
MSC2	0x1234 12BC

Table 6: /CS0..5 Init Values

6.3 SDRAM Memory (U13/U15)

The phyCORE-PXA255 is equipped with a 64 MByte, 32-bit data width SDRAM memory. This memory is created by using two SDRAM devices with 32 MByte each and 16-bit data bus at U13 and U15. This also refered to as SDRAM bank 0. The total SDRAM memory can be expanded to 128 MByte by populating the second banks (bank 1) at U14 and U16 with additional memory devices. The configuration of bank 1 corresponds to the configuration of bank 0.

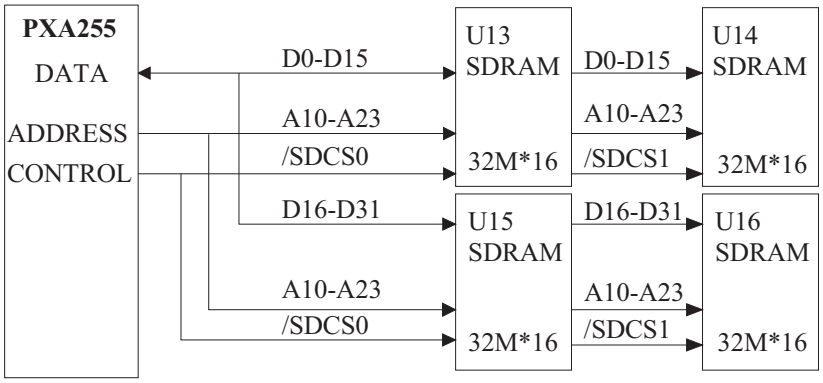

Figure 7: SDRAM 32-128 MB Connection to PXA255

Upon special request the phyCORE-PXA255 can also be populated with 256 MByte SDRAM. In this configuration 64M*16 SDRAM memory chips populate U13-U16, with 2 Chip Selects controlling each SDRAM device.

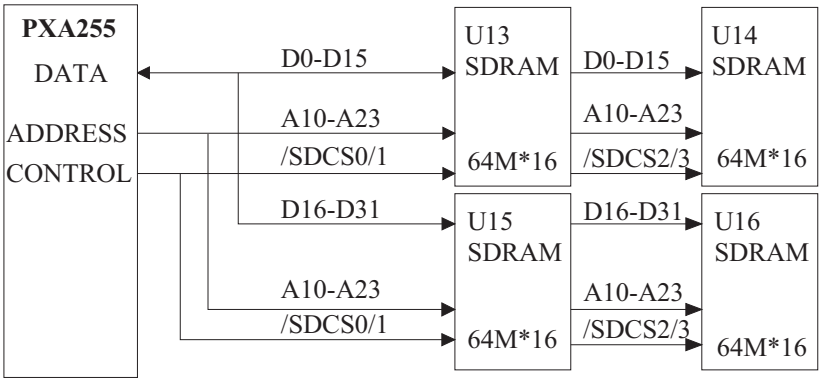

Figure 8: SDRAM 128-256 MB Connection to PXA255

SDRAM	**Configuration (also refer to the PXA255 controller documentation)**														
Range	16 M*32-bit (2 * 16-bit SDRAM each)														
Bus Width	32-bit														
Address Mode	SA1111 Address Mode														
Address Scheme	2*13*10*16														
Assignment	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10
	A12	B1	B0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Clock Rate	100 MHz														

Table 7: SDRAM Configuration

SDRAM initialization is performed by a boot loader or the operating system following a power-on reset and must not be changed at a later point by any application code. The following table *Table 8* shows the initialization values for bank0/1 as an example.

PXA255 Regitser	**Initialization Values**
MDCNFG	0x1ED8 1EDB
MDREFR	0x0085 C018
MDMRSLP	0x0000 0000
MDMRS	0x0000 0000

Table 8: SDRAM Init values

The physical memory areas of SDRAM bank 0 to bank 3 are shown in the following table. Using the PXA255's internal MMU it is possible to assign different virtual addresses to these banks at any time.

SDRAM Bank	**Start Address**
Bank 0	0xA000 0000
Bank 1	0xA400 0000
Bank 2	0xA800 0000
Bank 3	0xAA00 0000

Table 9: SDRAM Address Ranges

6.4 Flash Memory (U10/U11)

Use of Flash as non-volatile memory on the phyCORE-PXA255 provides an easily reprogrammable means of code storage. Intel Strata Flash is used as the Flash device for the phyCORE-PXA255. The Flash devices operate in 16-bit mode. Two individual Flash chips are connected to the 32-bit data bus on the module. The device at U13 is connected to the low data bus (D0-D15) and the device at U15 is connected to the high data bus (U16-U31).

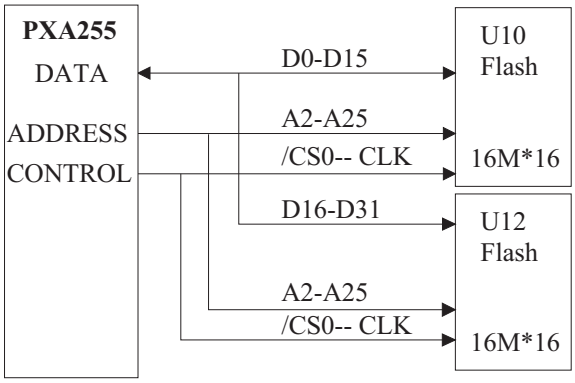

Figure 9: Flash Connection to PXA255

The Flash devices can operate in asynchronous as well as synchronous mode. Currently the asynchronous mode is used on the phyCORE-PXA255. Upon special request it is possible to deliver the module with a 4M*16-bit asynchronous Flash (U11). This is intended for use in applications with minimal memory requirements.

Flash	**Configuration**
Range	8M* 32-bit (2* 16-bit 28F128K3 Intel Strata Flash each)
Access	32-bit
Clock Rate	Asynchronous (optional synchronous up to 66 MHz)

Table 10: Flash Configuration

The physical memory area of the Flash bank is shown in the following table. Using the internal MMU of the PXA255 it is possible to assign different virtual addresses to this Flash bank at any time.

Flash	**Start Address**
Bank 0	0x0000 0000

Table 11: Flash Address Ranges

Use of Flash memory enables in-circuit programming of the module. The Flash devices on the phyCORE-PXA255 are programmable at 3.3 VDC. Consequently, no dedicated programming voltage is required. As of the printing of this manual, Flash devices generally have a life expectancy of at least 100,000 erase/program cycles.

6.5 External Address and Data Bus

The address and data bus of the PXA255 is accessible on the Molex connector at X3. The address/data bus operates on the module with a clock speed of 100 MHz. It is therefore absolutely necessary to decouple the address/data bus when using it for external circuitry. The decoupling circuits should be located as close to phyCORE-Connector at X3A/B as possible. The optimal signal trace length is less than 40 mm!

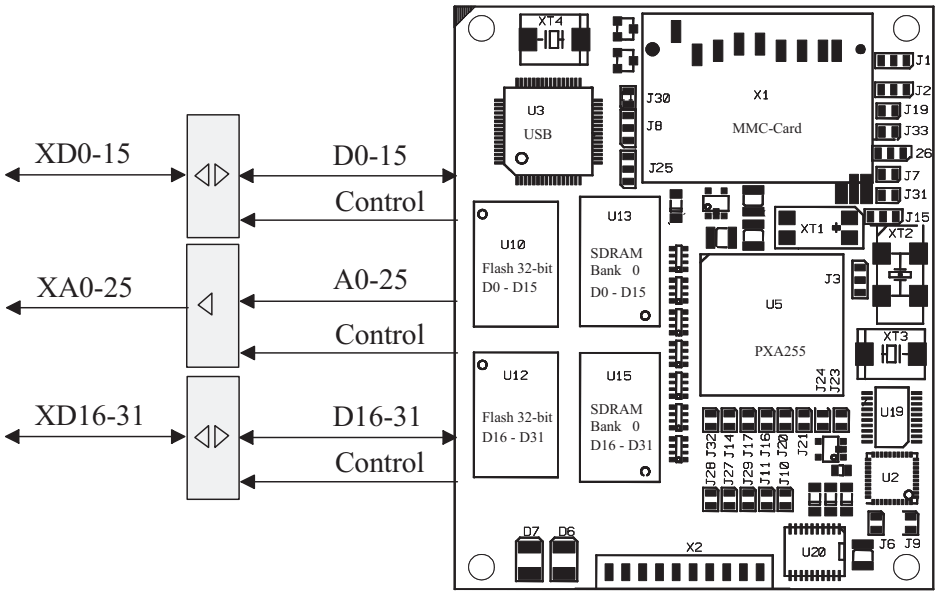

Figure 10: Decoupling the Address/Data Bus for External Connections

7 Ethernet Controller (U7)

Connection of the phyCORE-PXA255 to the world wide web or a local network is possible with the on-board SMSC LAN91C111 10/100 Mbps Ethernet controller populating the module at U17. This Ethernet controller features an integrated PHY layer. Thus the external components required to connect the phyCORE-PXA255 to a LAN are limited to the transformer, the RJ45 socket and a few discrete components. The Ethernet chip is supported by a wide range of operating systems, such as Linux, WIN CE and QNX.

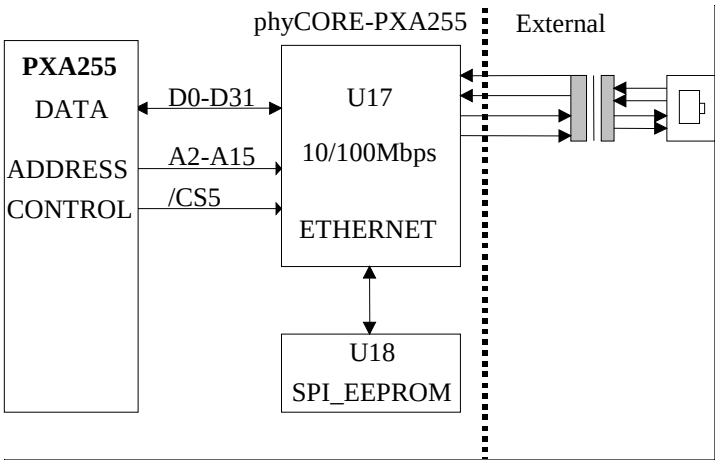

Figure 11: Ethernet Connection to PXA255

The Ethernet controller is connected to the data bus with a 32-bit width and can be configured via Jumpers J16, J17, J20 and J22. Jumper J15 is used to connect the interrupt signal of the LAN91C111 with a corresponding input on the PXA255 processor or to external logic. The interrupt is being used as active high edge triggered.

J20	**Description**
closed	LAN91C111 interrupt signal connected to GPIO2 on the PXA255 processor.
open	External interrupt signal used for LAN91C111, connected via phyCORE-Connector.

Table 12: Ethernet Controller Interrupt Signal Connection

The /CS signal for the LAN91C111 Ethernet controller at U17 can be connected to the PXA255 processor's /CS5 signal using Jumper J16. The Ethernet controller's offset of 0x300 has to be noted when accessing the chip.

J16	**Description**
closed	/CS signal for LAN91C111 connected to /CS5 of the PXA255 processor.
open	External /CS signal used for LAN91C111, connected via phyCORE-Connector.

Table 13: Ethernet Controller /CS Signal Connection

The Ethernet controller provides a READY output that can be connected to the /RDY input of the controller using Jumper J17. It is also possible to combine various signal sources externally if multiple components need to use the processor's RDY input.

J17	**Description**
closed	LAN_RDY (ARDY) signal from LAN91C111 connected to RDY input of the PXA255 processor.
open	LAN_RDY (ARDY) signal from LAN91C111 not used or connected externally, available on phyCORE-Connector (X3A66).

Table 14: Ethernet Controller READY Output Connection

The VLIO interface on the PXA255 is used as the memory interface for the Ethernet controller. For this reason the /WE signal from the Ethernet controller is connected to the /PWE signal on the PXA255.

J22	**Description**
1 + 2	PXA255 VLIO memory interface with /PWE
2 + 3	PXA255 SRAM/ROM memory interface with /WE

Table 15: Ethernet Controller Memory Interface Connection

The physical memory area for the Ethernet chip is defined in the following table (*see Table 16*). An offset of 0x300 has to be added to the address of /CS5 if Jumper J16 is closed. When using an external /CS signal the same procedure applies, add an offset of 0x300 to the address of the external /CS signal.

Ethernet	Start Address
/CS5 + OFFSET	0x1400 0000 + 0x0000 0300 = 0x1400 0300

Table 16: Memory Area Ethernet Controller

Connection to an external Ethernet transformer should be done using very short signal lines. The lines TPI+/TPI- and TPO+/TPO- should be routed in pairs. The same applies for the signal lines after the transformer circuit. The carrier board layout should avoid any other signal lines crossing the Ethernet signals. Furthermore, the impedance of the signal lines should be take into considertaion during the design and layout process.

Caution!
Please note the design specifications provided by SMSC when creating the Ethernet transformer circuitry.

8 USB OTG Controller (U3)

The Philips ISP1362 USB controller populates the phyCORE-PXA255 at U3. This USB controller features two integrated USB host interfaces. The first USB interface can be operated in OTG (On-The-Go) mode. When connecting the USB interfaces to external devices only minimal circuitry for connection of the USB signal lines and the USB power supply is required. All necessary USB controller signals are directly accessible on the phyCORE-Connector without furrther configuration. This ISP1362 USB controller is supported by a wide range of operating systems such as Linux and Windows CE.

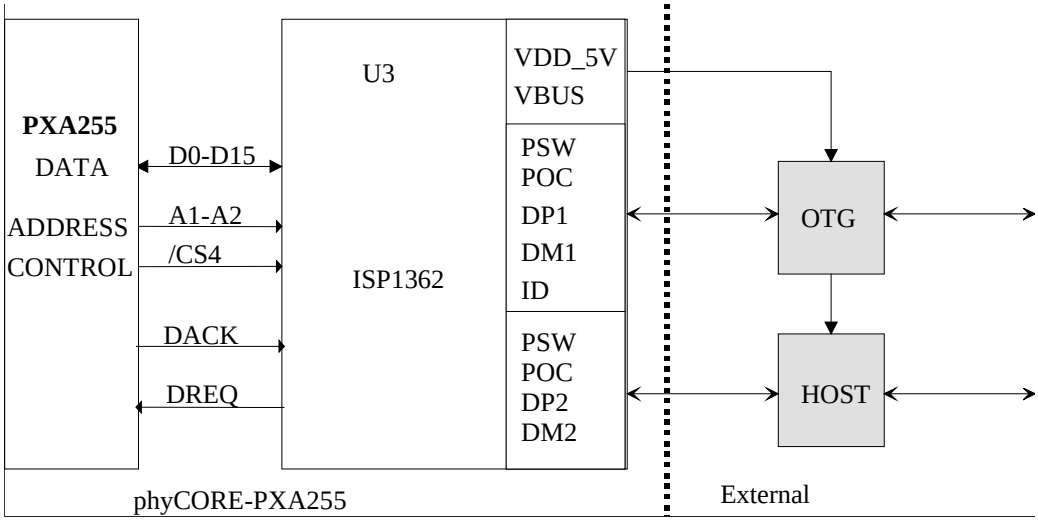

Figure 12: USB Circuitry

The USB controller is connected to the PXA255 with a 16-bit data bus. Jumpers J14 and J25 configure the USB controller interrupt outputs

J14	**Description**
closed	USB interrupt 1 signal connected with GPIO_3 on the controller
open	USB interrupt 1 signal connected to external interrupt input

Table 17: USB Controller Interrupt 1 Signal

J32	Description
closed	USB interrupt 2 signal connected with GPIO_4 on the controller
open	USB interrupt 2 signal connected to external interrupt input

Table 18: USB Controller Interrupt 2 Signal

Jumper JP25 connects the USB controller /CS signal with /CS2 or /CS4 on the PXA255 controller. The default configuration connects /CS4 on the PXA255 to the /OTG_CS signal on the USB controller.

J25	Description
1 + 2	USB /CS signal connected to /CS2 on the PXA255 controller
2 + 3	Default; USB /CS signal connected to /CS4 on PXA255
open	External /CS signal required to select the USB controller

Table 19: USB Controller /CS Signal

The USB controller provides a DMA circuitry with DACK1 connected to the active address A24 and DACK0 with address A25 within the USB controller memory space. This allows the PXA255 controller to access both DMA channels on the USB controller. The DMA request from the USB controller goes to the DREQ0 and DREQ1 lines with each of these lines having an open-emitter circuitry. This enables other circuits to use the DMA request signals as well.

Jumper J8 is provided to configure the mode of USB interface 1 to either USB host or USB OTG (On-The-Go). The default setting selects host mode.

J8	Description
1 + 2	USB Interface 1 operates in host mode.
2 + 3	USB Interface 1 operates in OTG mode.

Table 20: USB Interface 1 Mode

Jumper J9 can be closed in order to connect the VDD_5V voltage input permanently to VCC (3.3 V). This is only recommended if no over current protection is desired.

J9	Description
closed	VDD_5V connected to VCC (3.3 V)
open	External connection required via phyCORE-Connector pin X3C6.

Table 21: USB VDD_5V

9 PCMCIA Connection

The Intel PXA255 processor supports two PCMCIA sockets. These cannot be connected directly to the address and data bus of the processor. Proper operation requires external decoupling between the address/data bus and the PCMCIA sockets. The circuitry required for implementing one or two external PCMCIA sockets is described in the corresponding Intel application notes.

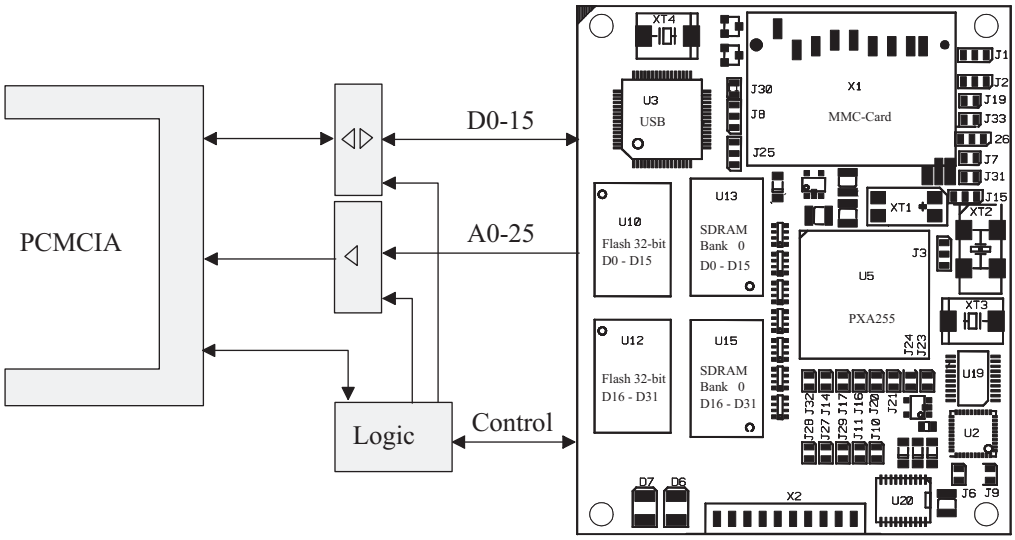

Figure 13: PCMCIA Connection to phyCORE-PXA255

10 phyCORE LEDs

A yellow RUN and a red BUSY LED are provided on the phyCORE-PXA255 indicating the state of the module. These LEDs can be controlled via operating system functions using pins GPIO21 (RUN) and GPIO22 (BUSY).

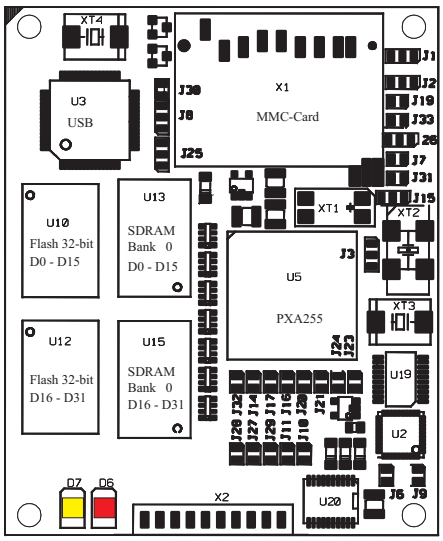

Figure 14: phyCORE-PXA255 LEDs

Jumper J27 configures the RUN LED. Closing this jumper with a 1 kOhm resistor (0805 footprint) will connect the LED to GPIO21.

J27	**Description**
closed with 1 kOhm	RUN LED connected to GPIO21 on PXA255
open	RUN LED not used

Table 22: RUN LED

Jumper J28 configures the BUSY LED. Closing this jumper with a 1 kOhm resistor (0805 footprint) will connect the LED to GPIO22.

J28	**Description**
closed with 1 kOhm	BUSY LED connected to GPIO22 on PXA255
open	BUSY LED not used

Table 23: BUSY LED

11 LCD Connection

The Intel PXA255 processor supports a wide variety of passive and active LCDs. *Additional information about the LCD support feature is available in the Intel data sheets*. We recommend to decouple the LCD data and control lines from the PCA255 pins using applicable line driver circuits. The brightness of the LCD's background light can be adjusted using one of the controller's PWM signals.

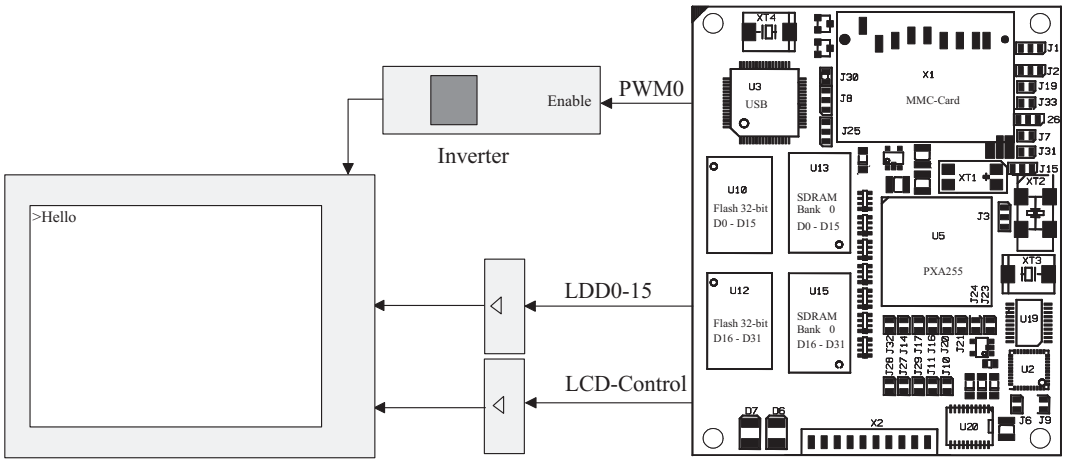

Figure 15: LCD Connection to phyCORE-PXA255

The example circuitry connection shown in the figure above refers to the control of the LCD with a fixed color depth setting. Multiplexers are required if the color depth needs to be able to vary between 16-bit and 8-bit because the RGB color information is distributed over LDD0-7 for 8-bit and LDD0-15 for 16-bit.

12 Serial Memory

12.1 I²C EEPROM (U4)

The phyCORE-PXA255 is populated with a non-volatile memory with a serial interface (I^2C interface) to store configuration data and operational parameters that need to be saved in the event of a power loss. According to the memory configuration of the module, an E²PROM (4 to 32 kByte) or FRAM can be mounted at U8. The I^2C bus signals from the PXA255 processor as well as the SDA/SCL signals from the EEROM are routed to the phyCORE-Connector at X3. This allows for an external connection of these signals. It is also possible to establish this signal connection on the phyCORE module using Jumpers J10 and J11.

A description of the I^2C memory protocol of the specific memory component at U4 can be found in the respective Data Sheet.

J10, J11	Description
closed	SDA and SCL from PXA255 connected to EEPROM at U4.
open	External SDA and SCL signal used for accessing the EEPROM.

Table 24: Jumper Configuration J10/J11 for Serial Memory at U4

The bootloader on the module uses this memory to store its configuration data. The EEPROM memory size is 1 kByte. Additional technical data is given in the following table.

Capacity	I^2C Clock	Address Pins	Write cycles	Data retention	Device	Manufacturer
1/ 2 KByte	400 kHz	A2, A1, A0	1,000,000	100 years	24WC08	Any

Table 25: Technical Data for Serial Memory at U4

12.2 MultiMedia Card (MMC)

The phyCORE module provides a receptacle socket for a MultiMedia card. The MM cards are available in capacities of 8 MByte to 512 MByte. Using such memory cards allows for easy expansion of the on-board memory configuration of the phyCORE-PXA255 to new application requirements retroactively.

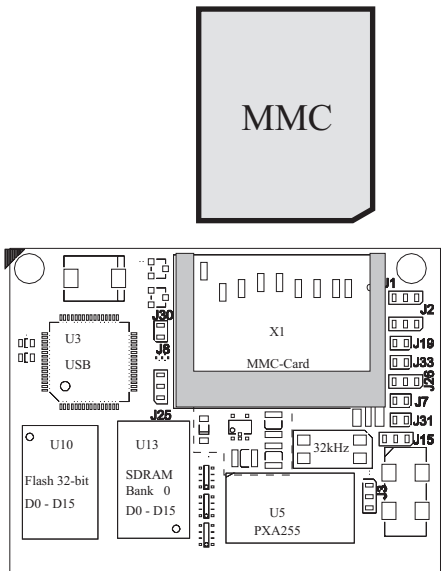

Figure 16: MMC Connector on the phyCORE-PXA255

The on-board MMC connector at X1 is controlled using the PXA255 processor's MMCS0 signal. The second interface (MMCS1 signal) is available for external use. The MMC socket signals Detect and WriteProtect are externally available and can be used as needed. Jumper J1 determines the source of the supply voltage for the MM card. The on-board 3.3 V VCC voltage are used by default. Setting Jumper J1 to position 2+3 can be useful for implementing special power saving modes, during which the external VMMC is only switched on in the event of an access to the card.

Caution!
The VMMC voltage cannot be connected without VCC being supplied at the same time.

J1	Description
1 + 2	MM card supplied via VCC.
2 + 3	MM card supplied externally via VMMC.

Table 26: MultiMedia Card VMMC Configuration

Detection of an inserted MM card at X1 is possible via the MMC_DET signal. A low level indicates a card is in the socket. This signal is connected to GPIO_7 on the PXA255 controller when Jumper J31 is closed with a 0 Ohm resistor.

J31	Description
closed	MM card detect connected to GPIO7
open	MM card detect not used

Table 27: MultiMedia Card Detect Configuration

The MMC_WP signal indicates with a low signal level that an insreted MM card is write protected. Jumper J7 connects this signal to GPIO_10 on the PXA255 controller.

J7	Description
closed	MM card write protect connected to GPIO10
open	MM card write protect not used

Table 28: MultiMedia Card WriteProtect Configuration

13 Serial Interfaces

13.1 RS-232 Interface

The Intel PXA255 processor provides four internal UARTS. Three of them are supported in the current version of the phyCORE-PXA255. The on-chip FF-UART (Full Function) is a UART that supports all modem signals and a maximum transfer rate of 230.4 kBaud. This interface is used on the phyCORE-PXA255 for communication with the host-PC. The RS-232 transceiver for is interface is located on the module at U1. The minimal wiring for establishing a connection between the PC and the phyCORE-PXA255 is shown in the figure below. Additional modem signals are available on the phyCORE-Connector at X3.

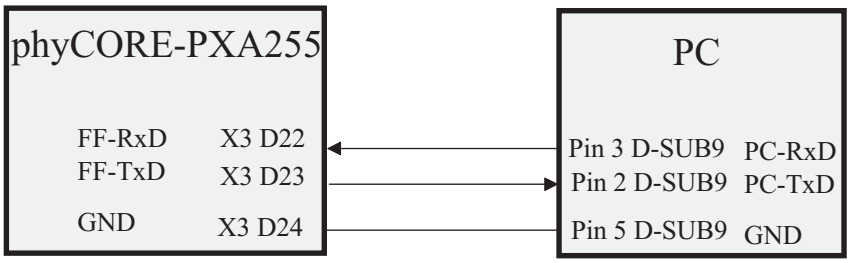

Figure 17: FF-UART Connection

The on-chip BT-UART (Bluetooth) is a high speed UART that supports baud rates up to 921.6 kBaud and can be connected to a Bluetooth module. This BT-UART only support the signals BT_RxD, BT_TxD, BT_CTC and BT_RTS. These signals extend to the phyCORE-Connector of the phyCORE-PXA255. The serial interface is intended for controlling Bluetooth send/receive modules, but it can also be used as a normal UART.

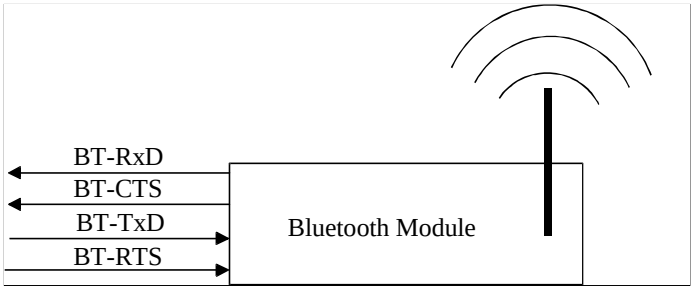

Figure 18: BT-UART Connection

The STD-UART (Standard) only provides the signals STD_RxD and STD_TxD. No modem signals are supported. The maximum transfer rate is 230.4 kBaud. The STD-UART has a special mode for controlling IrDA transmitters.

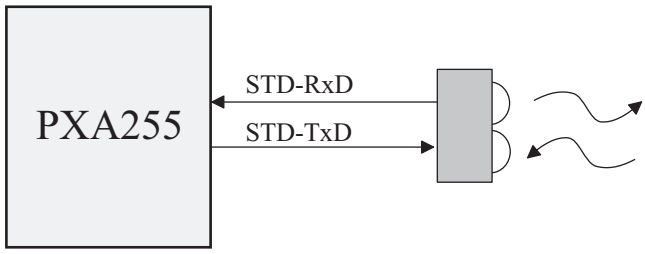

Figure 19: STD_UART Connection

The on-chip HW-UART is a high speed UART that supports baud rates up to 921.6 kBaud. This HW-UART only support the signals HW_RxD, HW_TxD, HW_CTC and HW_RTS.

The HW-UART interface pins are available either via the BT-UART pins or the PCMCIA general purpose I/O pins. The routing is selcted by PXA255 register configuration. When using the HW-UART through the PCMCIA pins, the signal /PWE can not be defined as HW-UART pin (HW_RxD) because it is required for the VLIO memory interface.

13.2 SSP and NSSP Interface

The phyCORE-PXA255 module is populated with a CAN controller and a GPIO expander which are connected to the processor's SSP or NSSP interface.

13.2.1 CAN Controller (U19)

The Microchip MPC2515 FullCAN controller is implemented on the phyCORE-PXA255. The CAN controller is connected with the PXA255 via the SSP (synchronous serial protocol) interface. The /CS signal for the CAN controller must be supplied externally via pin 76C on Molex connector X3.

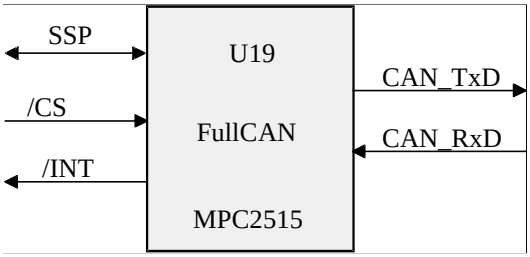

Figure 20: CAN Controller Connection

The control signals of the SPI access can be connected externally as well as internally using Jumper J24.

The CAN controller's interrupt output can be connected to various signals via Jumper J24.

J24	**Description**
closed	Interrupt signal from MPC2515 connected to GPIO_5 on PXA255.
open	Interrupt signal can be connected to external device.

Table 29: CAN Controller Interrupt Signal

There is no on-board CAN transceiver implemented on the phyCORE-PXA255. Thus connection to an external transceiver in the application circuitry is required when using this module oin a CAN system.

13.2.2 GPIO Expander (U2)

The Intel PXA255 processor features 80 GPIO ports. However, most of them are used on-board with useful alternative functions such as MMC, LCD, UARTs among others. In order to provide the user with a reasonable number of general purpose I/O (GPIO) lines, the phyCORE-PXA255 is populated with a MAX7301 GPIO expander IC. The MAX7301 has the following features:

- SPI interface
- 28 GPIO ports
- 7 interrupt-capable inputs
- One interrupt output

All GPIO signals are routed to the module's phyCORE-Connector. One of the special features of the MAX7301 controller is its capability to control matrix keyboards. *Refer to the MAX7301 datasheet for more details on this function.*

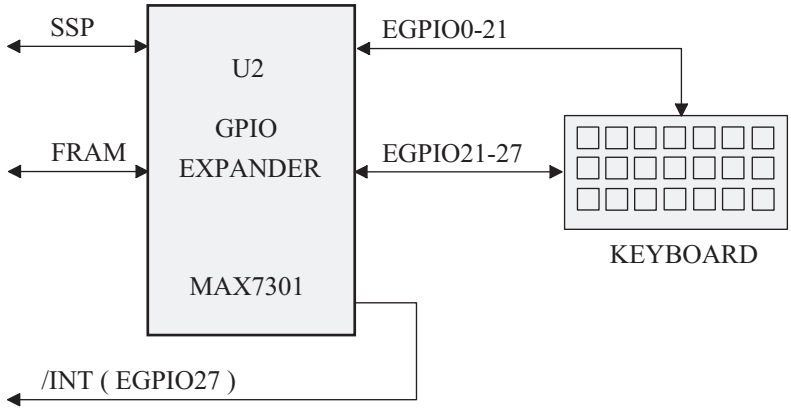

Figure 21: MAX7301 Connection

The MAX7301 can be connected externally as well as on-board using Jumpers J6 and J9. Jumper J6 configures the SPI /CS signal while J9 is used to connect the interrupt signal.

J6	**Description**
closed	/CS signal for MAX7301 connected to SSP_SFRM on PXA255.
open	External SPI /CS signal used for GPIO expander

Table 30: SPI /CS Signal for MAX7301

J9	**Description**
closed	Interrupt signal from MAX7301 connected to SSP_EXTCLK on PXA255.
open	Interrupt signal can be connected to external device.

Table 31: Interrupt Signal MAX7301

13.3 AC97 Interface

The Intel PXA255 processor integrates an AC97 interface for controlling sound decoder chips such as the Wolfson AC97 sound controller. One of the special features of the Wolfson device is an integrated touch controller.

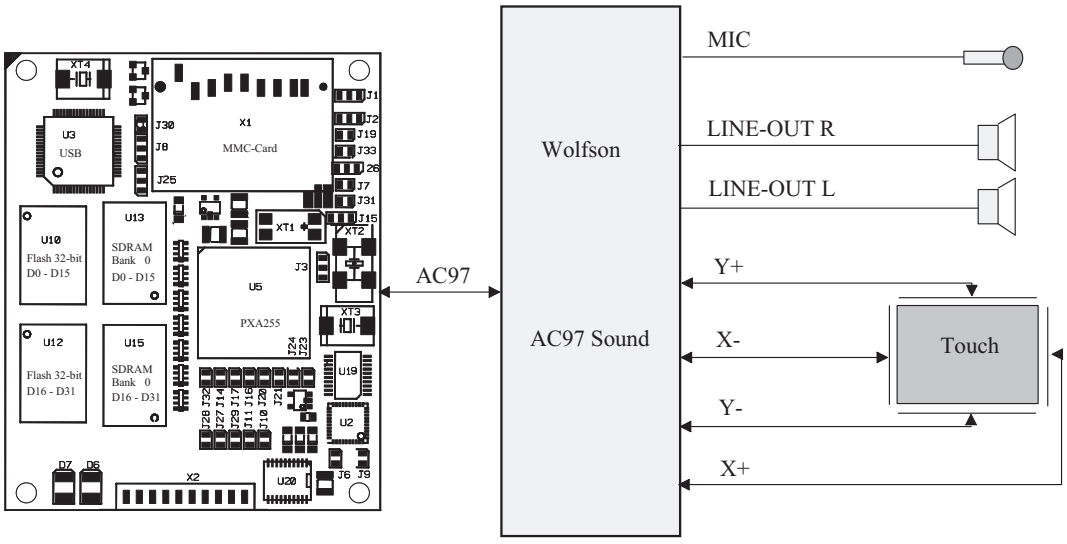

Figure 22: AC97 Interface with Wolfson

All signals of the AC97 interface are routed to the phyCORE-PXA255 Molex connector.

13.4 Real-Time Clock RTC-8564 (U20)

For real-time or time-driven applications, the phyCORE-PXA255 is equipped with an RTC-8564 Real-Time Clock at U20. This RTC device provides the following features:

- Serial input/output bus (I^2C), address 0xA2, up to 400 kHz bus frequency
- Power consumption
  I^2C bus active (400 kHz): < 1 mA
  I^2C bus inactive, CLKOUT inactive: < 1 µA
- Clock function with four year calendar
- Century bit for year 2000-compliance
- Universal timer with alarm and overflow indication
- 24-hour format
- Automatic word address incrementing
- Programmable alarm, timer and interrupt functions

If the phyCORE-PXA255 is equipped with a battery (VBAT), the Real-Time Clock runs independently of the board's power supply.

Programming the Real-Time Clock is done via the I^2C bus. The Real-Time Clock also provides an interrupt output that extends to GPIO0 on the PXA255 via Jumper J29. An interrupt occurs in case of a clock alarm, timer alarm, timer overflow and event counter alarm. An interrupt must be cleared by software. With the interrupt function, the Real-Time Clock can be utilized in various applications. *For more information on the features of the RTC-8564, refer to the corresponding Data Sheet.*

Note:
After connection of the supply voltage, or after a reset, the Real-Time Clock generates **no** interrupt. The RTC must first be initialized (*see RTC Data Sheet for more information*).

13.5 JTAG Interface

The PXA255 provides a JTAG interface for connecting to debuggers, emulators and boundary scan. The interface has its own reset controller (U8). The JTAG interface signals extend to the module's phyCORE-Connector. Furthermore, there is an on-board JTAG connector (X2) located at the edge of the module, which has the standard ARM pinout but uses a 2.0 mm pin pitch instead of 2.54 mm. The connector is not populated on the standard version of the phyCORE-PXA255. You can order a specific debug version of the module (denoted by the –D part number extension) or populate a 2* 10-pin header connector at space X2. The numbering scheme is depicted on the phyCORE-PXA255. The pinout of the JTAG interface at X2 is described in the following table.

Signal		Pin Row			Signal
		A	**B**		
VREF		1	2		VCC
/JTAG-RESET		3	4		GND
JTAG-TDI		5	6		GND
JTAG-TMS		7	8		GND
JTAG-TCK		9	10		GND
JTAG-RTCK		11	12		GND
JTAG-TDO		13	14		GND
RESET (System)		15	16		GND
N.C.		17	18		GND
N.C.		19	20		GND

Table 32: JTAG Interface

14 Technical Specifications

The physical dimensions of the phyCORE-PXA255 are represented in *Figure 23.*

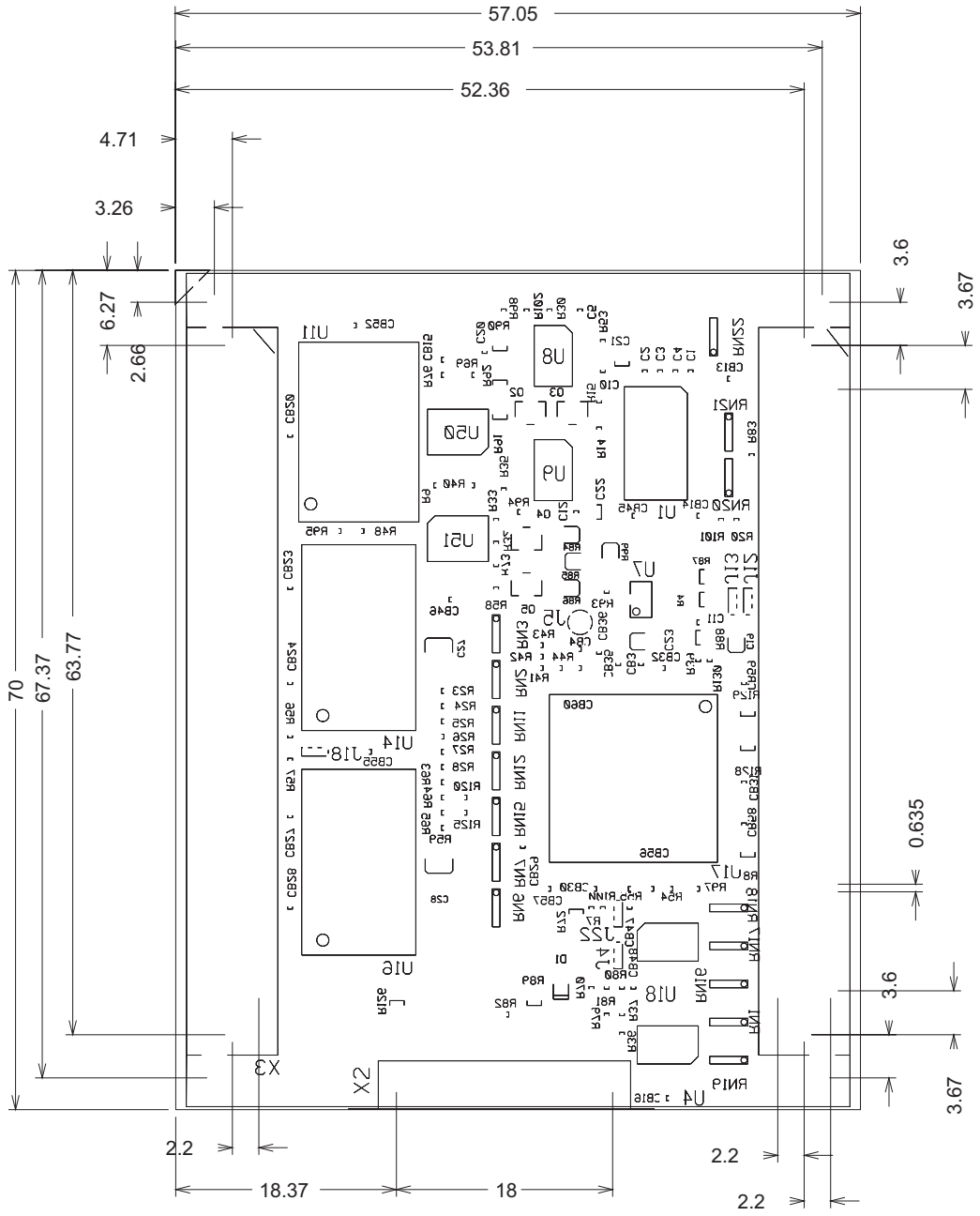

Figure 23: Physical Dimensions

The height of all components on the top side of the PCB is ca. 4.5 mm. The PCB itself is approximately 1.1 mm thick. The Molex connector pins are located on the underside of the PCB, oriented parallel to its two long sides. The maximum height of components on the underside of the PCB is 2 mm.

Additional Technical Data:

Parameter	**Condition**	**Characteristics**
Dimensions		72 mm x 57 mm
Weight		approximately 25 g with all optional components mounted on the circuit board
Storage Temp. Range		-40°C to +90°C
Operating Temp. Range: Extended		 -25°C to +85°C
Humidity		max. 95 % r.F. not condensed
Operating voltages: Spannung 3.3V		 3.3 V ±5 %
Operating Power Consumption: Voltage 3.3 V	(depending on load)	 Max. 1.5 Watt

Table 33: Technical Data

These specifications describe the standard configuration of the phyCORE-PXA255 as of the printing of this manual.

Connectors on the phyCORE-PXA255:

Manufacturer	Molex
Number of pins per contact rows	160 (2 rows of 80 pins each)
Molex part number	52760-1609 (receptacle)
Molex part number (lead free)	52760-1679 (receptacle)

Two different heights are offered for the receptacle sockets that correspond to the connectors populating the underside of the phyCORE-PXA255. The given connector height indicates the distance between the two connected PCBs when the module is mounted on the corresponding carrier board. In order to get the exact spacing, the maximum component height (2 mm) on the underside of the phyCORE must be subtracted.

Component height 6 mm

Manufacturer	Molex
Number of pins per contact row	160 (2 rows of 80 pins each)
Molex part number	55091-1609 (header)
Molex part number (lead free)	55091-1679 (header)

Component height 10 mm

Manufacturer	Molex
Number of pins per contact row	160 (2 rows of 80 pins each)
Molex part number	53553-1609 (header)
Molex part number (lead free)	53553-1679 (header)

Please refer to the coresponding data sheets and mechanical specifications provided by Molex (www.molex.com).

15 Hints for Handling the Module

- **Modifications on the phyCORE Module**

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while desoldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Caution!
If any modifications to the module are performed, regardless of their nature, the manufacturer guarantee is voided.

- **Integrating the phyCORE-PXA255 into a Target Application**

Successful integration in user target circuitry greatly depends on the adherence to the layout design rules for the GND connections of the phyCORE module. For best results we recommend using a carrier board design with a full GND layer. It is important to make sure that the GND pins that have neighboring signals which are used in the application circuitry are connected. Just for the power supply of the module at least 6 GND pins that are located right next to the VCC pins must be connected.

16 U-Boot Boot Loader

Upon delivery of the phyCORE-PXA255 there is a boot loader (U-Boot) stored in the Flash memory. The boot loader is 128 kB in size and is stored in the Flash starting at address 0x00000000. The boot loader performs the initial PXA255 processor configuration following a reset. Configuration includes initialization of the SDRAM, the Flash and the port pins depending on their function. The boot loader subsequently starts the operating system or carries out low level commands in its own monitor such as `tftpboot` for loading images to the SDRAM.

16.1 Initializing the phyCORE-PXA255

The boot loader initializes the /CS signals of the PXA255 after reset. The timing parameters are subject of ongoing adaptations and should therefore be taken from the most current source code of the U-Boot boot loader.

/CS Signal	Busb Width	Usage
/CS0	32-bit	2* 16-bit Flash memory 16 to 64 MByte async / sync
/CS1	16-bit	Free (16-bit asynchonous ROM/RAM)
/CS2	16-bit	Free (16-bit VLIO interface)
/CS3	32-bit	Free (32-bit VLIO interface)
/CS4	16-bit	Free (16-bit VLIO interface)
/CS5	32-bit	Ethernet Chip 32-bit VLIO interface or free
/SDCS0	32-bit	64 MByte 2*16-bit SDRAM SA1111 mode
/SDCS1	32-bit	64 MByte 2*16-bit SDRAM SA1111 mode
/SDCS2	32-bit	Free
/SDCS3	32-bit	Free

Table 34: U-Boot Memory Configuration

The GPIO port initialization is listed in the following table.

Port	**I/O**	**Configured as**
GPIO0	I	GPIO 0
GPIO1	I	GPIO 1
GPIO2	I	GPIO 2
GPIO3	I	GPIO 3
GPIO4	I	GPIO4
GPIO5	I	GPIO5
GPIO6	I	GPIO6
GPIO7	I	GPIO7
GPIO8	I	GPIO8
GPIO9	I	GPIO9
GPIO10	I	GPIO10
GPIO11	I	GPIO11
GPIO12	I	GPIO12
GPIO13	I	GPIO13
GPIO14	I	GPIO14
GPIO15	O	/CS1
GPIO16	O	PWM0
GPIO17	O	PWM1
GPIO18	I	READY input
GPIO19	I	GPIO19
GPIO20	I	GPIO20
GPIO21	I	GPIO21
GPIO22	I	GPIO22
GPIO23	I	SCLK SPI clock
GPIO24	I	SFRM SPI frame signal
GPIO25	O	SPI TxD transmit line
GPIO26	I	SPI RxD receive line
GPIO27	I	SPI EXTCLK external master clock
GPIO28	O	AC97 BitCLK
GPIO29	I	AC97 SDATA_IN0
GPIO30	O	AC97 SDATA_OUT
GPIO31	O	AC97 SYNC
GPIO32	I	AC97 SDATA_IN1
GPIO33	O	/CS5
GPIO34	I	FF-UART RxD
GPIO35	I	FF-UART CTS
GPIO36	I	FF-UART DCD
GPIO37	I	FF-UART DSR
GPIO38	I	FF-UART RI
GPIO39	O	FF-UART TxD

Table 35: Port Configuration GPIO0-39

Port	I/O	Configured as
GPIO40	O	FF-UART DTR
GPIO41	O	FF-UART RTS
GPIO42	I	BT-UART RxD
GPIO43	O	BT-UART TxD
GPIO44	I	BT-UART CTS
GPIO45	O	BT-UART RTS
GPIO46	I	STD-UART RxD
GPIO47	O	STD-UART TxD
GPIO48	O	/POE PCMCIA
GPIO49	O	/PWE PCMCIA
GPIO50	O	/PIOR PCMCIA
GPIO51	O	/PIOW PCMCIA
GPIO52	O	/PCE1 PCMCIA
GPIO53	O	/PCE2 PCMCIA
GPIO54	O	/PKSEL PCMCIA (for selecting both PCMCIA cards)
GPIO55	O	/PREG PCMCIA
GPIO56	I	/PWAIT PCMCIA
GPIO57	I	/IOIS16 PCMCIA
GPIO58	O	LDD0, data bus to LCD display
GPIO59	O	LDD1, data bus to LCD display
GPIO60	O	LDD2, data bus to LCD display
GPIO61	O	LDD3, data bus to LCD display
GPIO62	O	LDD4, data bus to LCD display
GPIO63	O	LDD5, data bus to LCD display
GPIO64	O	LDD6, data bus to LCD display
GPIO65	O	LDD7, data bus to LCD display
GPIO66	O	LDD8, data bus to LCD display
GPIO67	O	LDD9, data bus to LCD display
GPIO68	O	LDD10, data bus to LCD display
GPIO69	O	LDD11, data bus to LCD display
GPIO70	O	LDD12, data bus to LCD display
GPIO71	O	LDD13, data bus to LCD display
GPIO72	O	LDD14, data bus to LCD display
GPIO73	O	LDD15, data bus to LCD display
GPIO74	O	LCD_FCLK, frame clock
GPIO75	O	LCD_LCLK, line clock
GPIO76	O	LCD_PCLK, pixel clock
GPIO77	O	LCD_ACBIAS BIAS oder LCD_Enable
GPIO78	O	/CS2
GPIO79	O	/CS3
GPIO80	O	/CS4

Table 36: Port Configuration GPIO40-80

Port	I/O	Configured as
GPIO81	I	GPIO 81
GPIO82	I	GPIO 82
GPIO83	I	GPIO 83
GPIO84	I	GPIO 84

Table 37: Port Configuration GPIO81-84

16.2 Communication with U-Boot

The U-Boot boot loader communicates exclusively over FF_UART with the user. It is required that at least the RS-232 signals RS_TxD, RS_TxD and GND of the phyCORE-PXA255 are connected to the PC's serial interface.

Signal on phyCORE	Signal on Host-PC
RS_TxD (Molex pin X3D23)	PC_RxD (pin 2 DB-9)
RS_RxD (Molex pin X3D22)	PC_TxD (pin 3 DB-9)
GND (e.g. Molex pin X3D24)	PC_GND (pin 5 DB-9)

Table 38: RS-232 Connection to Host-PC

A terminal program such as HyperTerminal (Windows) or miniCOM (Linux) can be used to display the output message of the U-Boot boot loader on the host-PC. The interface settings should be as follows.

- 115200 baud
- 8 data bits
- No priority
- 1 stop bit

Please note that the U-Boot boot loader only works line by line.

16.3 Important U-Boot Commands

The U-Boot boot loader provides a large number of commands that are available to the user. These are constantly being expanded and can be freely configured as well. Below are a few important commands of the U-Boot to get familiar.

- **help**

Lists all commands that are contained in the current U-Boot version and that have been configured.

help

- **Erase**

Erases a sector in the Flash. The boot loader is protected against accidental erasure by software. The following example erases the memory area of a Linux image.

erase 4000 1FFFF

- **tftpboot**

With this command an image can be loaded to the phyCORE from the >\tftpboot directory (FTP must be running). The following example stores a binary image with the name "phyImage" starting at address 0xA2000000 in the SDRAM.

tftpboot a2000000 phyImage

- **cp**

This is a copy command that can write to the Flash as well. In this example the phyImage *(see tftpboot)* can be copied from the SDRAM to the Flash.

cp.b a2000000 40000 1FFFFF

- **bootm**

This command loads an image from the Flash starting at address 0x00040000 (e.g. Linux) to the SDRAM and starts it there.

Bootm 40000

- **printenv**

This command returns the configuration data which was loaded from the I²C EEPROM to the SDRAM.

printenv

- **setenv**

This command writes a new configuration line to the SDRAM. In the example the IP address of the PC is set, from which the tftpboot acquires its image.

setenv serverip 192.168.0.1

- **saveenv**

This command writes the configuration data from the SDRAM to the I²C EEPROM. Thus the modifications are still present after power-off.

saveenv

17 Revision History

Date	Version numbers	Changes in this manual
15-Dec-2003	Manual L-655e_0 PCM-022 PCB# 1219.0	First edition.
27-Jul-2004	Manual L-655e_1 PCM-022 PCB# 1219.1	Update to match new PCB revision. Corections in section *2, Pin Description*. Paragraph describing device reset added in section *4*. Description added in section *6.3, SDRAM Memory (U13/U15)*. Description added in section *7, Ethernet Controller (U7)*. Section *8, USB OTG Controller (U3)* added. Section *10, phyCORE LEDs* added. Sections *13.2.1* and *13.4* added.
31-Jan-2005	Manual L-655e_2 PCM-022 PCB# 1219.3	Update to match new PCB revision. Corections in section *2, Pin Description* and 13.2.1 CAN Controller (U19) due to pin definition error for NSSP frame and TxD signals.
01-June-2005	Manual L-655e_3 PCM-022 PCB# 1219.3	Corections in section *2, Pin Description* for NSSP signal routing.

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