phyCORE-i.MX31

HARDWARE MANUAL

EDITION JULY 2009

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1 Preface

This phyCORE-i.MX31 Hardware Manual describes the single board computer's design and functions. Precise specifications for the Freescale i.MX31 microcontrollers can be found in the enclosed microcontroller Data Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" or "#" preceding the signal name (i.e.: /RD or #RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration of Electro Magnetic Conformity of the PHYTEC phyCORE-I.MX31

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution!
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-i.MX31 is one of a series of PHYTEC Single Board Computers that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports a variety of 8-/16- and 32-bit controllers in two ways:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform

(2) as insert-ready, fully functional phyCORE OEM modules, which can be embedded directly into the user's peripheral hardware, design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market. For more information go to:

http://www.phytec.com/services/phytec-advantage.html

1.1 Introduction

The phyCORE-i.MX31 belongs to PHYTEC's phyCORE Single Board Computer module family. The phyCORE SBCs represent the continuous development of PHYTEC Single Board Computer technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments the phyCORE board design features an increased pin package. The increased pin package allows dedication of approximately 20 % of all pin header connectors on the phyCORE boards to ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD components and laser-drilled Microvias are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCORE-i.MX31 is a subminiature (84 x 58 mm) insert-ready Single Board Computer populated with the Freescale i.MX31 microcontroller. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to high-density pitch (0.635 mm) connectors aligning two sides of the board, allowing it to be plugged like a "big chip" into a target application.

Precise specifications for the controller populating the board can be found in the applicable controller User's Manual or datasheet. The descriptions in this manual are based on the Freescale i.MX31. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCORE-i.MX31.

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The phyCORE-I.MX31 offers the following features:

- subminiature Single Board Computer (84 x 58 mm) achieved through modern SMD technology
- populated with the Freescale i.MX31 microcontroller (BGA457 packaging)
- improved interference safety achieved through multi-layer PCB technology and dedicated ground pins
- controller signals and ports extend to two 200-pin high-density (0.635 mm) Molex connectors aligning two sides of the board, enabling it to be plugged like a "big chip" into target application
- max. 400 MHz (532 MHz in overdrive Mode) core clock frequency
- boot from NOR or NAND Flash
- 32 MByte (up to 64 MByte) Intel Strata NOR Flash
- 64 MByte (up to 1 GByte) on-board NAND Flash[1]
- 128 MByte (up to 512 MByte) Mobile DDR SDRAM on-board
- RS-232 transceiver supporting one UART at data rates of up to 460 kbps
- Two full featured UART Interfaces without transceiver
- 32 KB I^2C EEPROM
- Separate I²C RTC with backup function
- 512 Kbyte (up to 2 MByte SRAM) with backup function
- battery buffered controller based RTC with automatic battery switchover
- High-Speed USB OTG transceiver
- Auto FDX/MDX 100MBit Ethernet Controller
- all controller required supplies generated on board by PMIC
- synchronous 18-bit LCD-Interface
- PCMCIA/CF card Interface
- ATA-Interface DMA-Mode 3 (up to DMA-mode 5 without level-shifter) / CMOS Camera Interface
- support of standard 20 pin debug interface through JTAG connector
- keyboard support for up to 24 keys in a 4 * 6 matrix
- two I^2C interfaces
- SD/MMC card interface with DMA
- special Power-Management IC
    - stereo line in
    - stereo line out / preamplified mono-out
    - stereo mic in
    - 4-Wire Touch interface
    - RTC
    - LCD-Backlight control
    - Battery charger
    - 6 AD-Inputs

1 Please contact PHYTEC for more information about additional module configurations.

1.2 Block Diagram

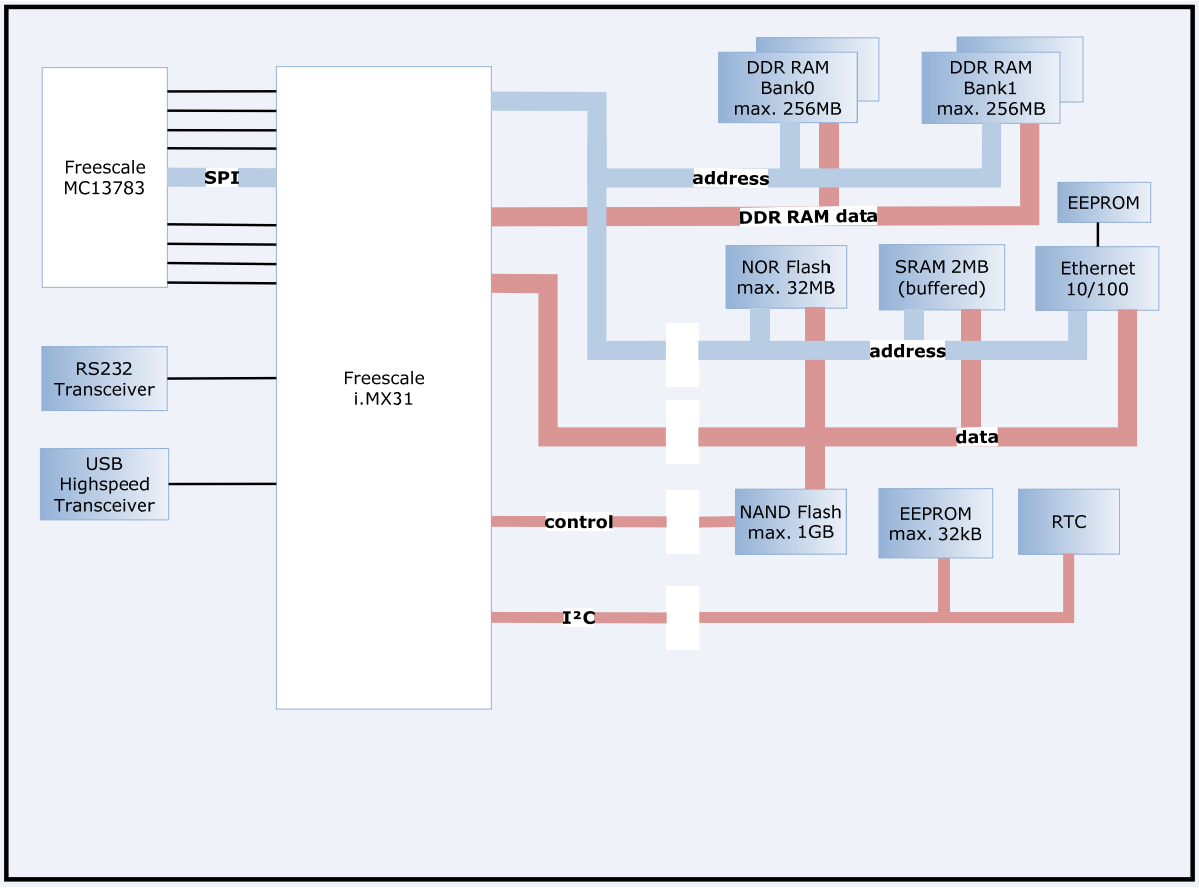

Figure 1: Block Diagram phyCORE-i.MX31

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1.3 View of the phyCORE-i.MX31

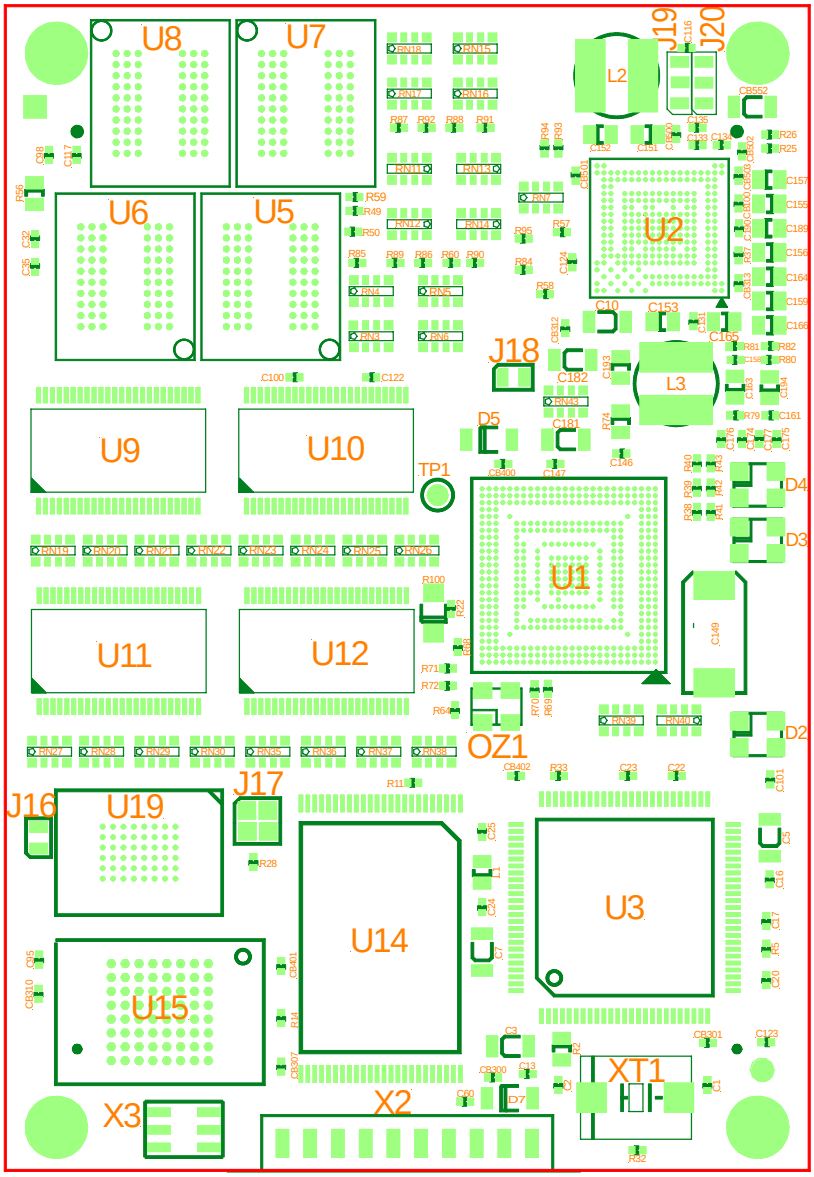

Figure 2: Top View of the phyCORE-i.MX31 (controller side)

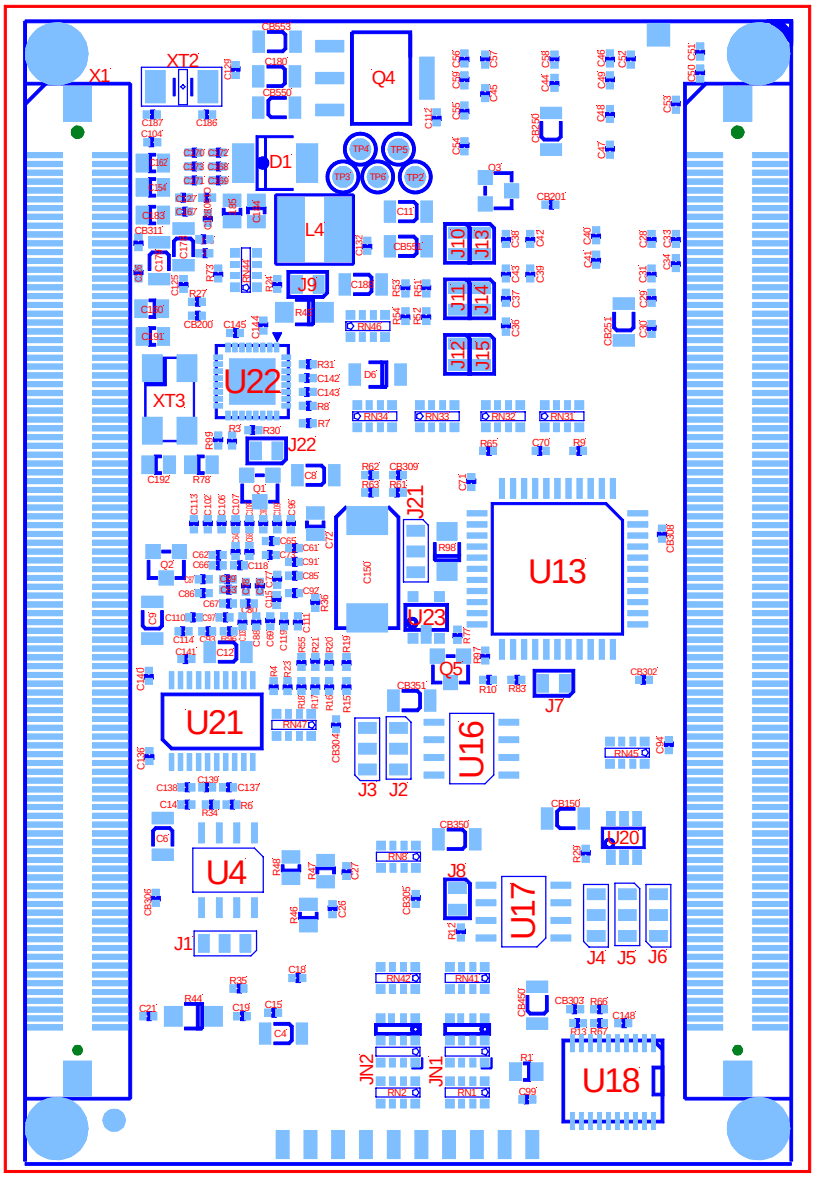

Figure 3: Bottom View of the phyCORE-i.MX31 (connector side)

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2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 4* indicates, all controller signals extend to surface mount technology (SMT) connectors (0.635 mm) lining two sides of the module (referred to as phyCORE-connector). This allows the phyCORE-i.MX31 to be plugged into any target application like a "big chip".

A new numbering scheme for the pins on the phyCORE-connector has been introduced with the phyCORE specifications. This enables quick and easy identification of desired pins and minimizes errors when matching pins on the phyCORE module with the phyCORE-connector on the appropriate PHYTEC Development Board or in user target circuitry.

The numbering scheme for the phyCORE-connector is based on a two dimensional matrix in which column positions are identified by a letter and row position by a number. Pin 1A, for example, is always located in the upper left hand corner of the matrix. The pin numbering values increase moving down on the board. Lettering of the pin connector rows progresses alphabetically from left to right (*refer to Figure 4*).

The numbered matrix can be aligned with the phyCORE-i.MX31 (viewed from above; phyCORE-connector pointing down) or with the socket of the corresponding phyCORE Development Board/user target circuitry. The upper left-hand corner of the numbered matrix (pin 1A) is thus covered with the corner of the phyCORE-i.MX31 marked with a triangle. The numbering scheme is always in relation to the PCB as viewed from above, even if all connector contacts extend to the bottom of the module.

The numbering scheme is thus consistent for both the module's phyCORE-connector as well as mating connectors on the phyCORE Development Board or target hardware, thereby considerably reducing the risk of pin identification errors.

Since the pins are exactly defined according to the numbered matrix previously described, the phyCORE-connector is usually assigned a single designator for its position (X1 for example). In this manner the phyCORE-connector comprises a single, logical unit regardless of the fact that it could consist of more than one physical socketed connector. The location of row 1 on the board is marked by a triangle on the PCB to allow easy identification.

The following figure (*Figure 4*) illustrates the numbered matrix system. It shows a phyCORE-i.MX31 with SMT phyCORE-connectors on its underside (defined as dotted lines) mounted on a Development Board. In order to facilitate understanding of the pin assignment scheme, the diagram presents a cross-view of the phyCORE module showing these phyCORE-connectors mounted on the underside of the module's PCB.

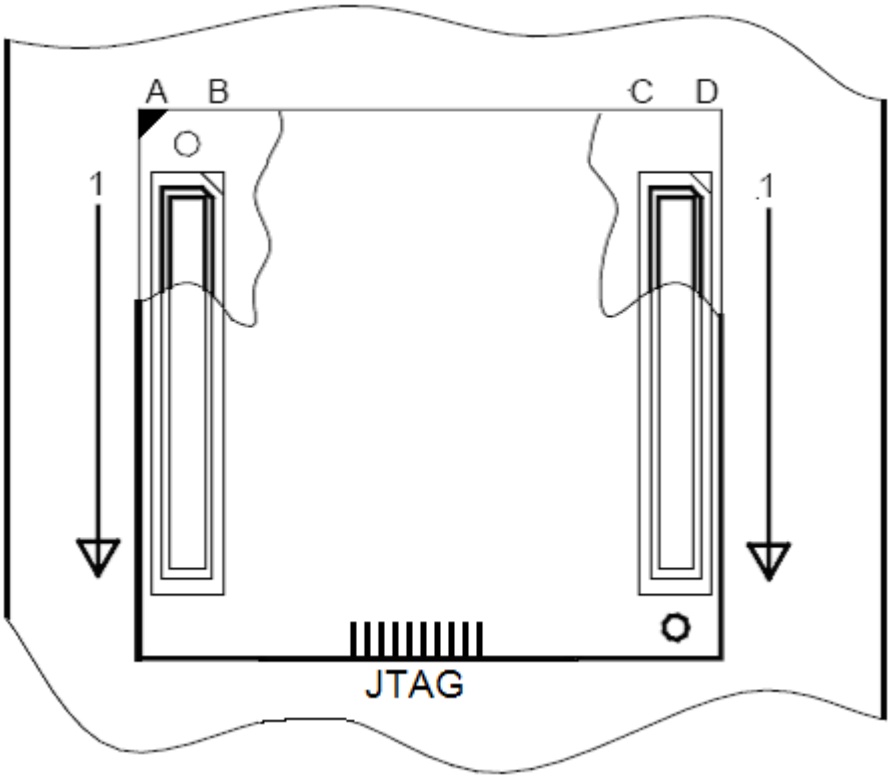

Figure 4: Pinout of the phyCORE-Connector (Top View, with Cross Section Insert)

Table 1 provides an overview of the pinout of the phyCORE-connector, as well as descriptions of possible alternative functions. *Table 1* also provides the appropriate signal level interface voltages listed in the SL (**S**ignal **L**evel) column. The Freescale i.MX31 is a multi-voltage operated microcontroller and as such special attention should be paid to the interface voltage levels to avoid unintentional damage to the microcontroller and other on-board components. *Please refer to the Freescale i.MX31 User's Manual/Data Sheet for details on the functions and features of controller signals and port pins*.

Note:
SL is short for Signal Level (V) and is the applicable logic level to interface a given pin.
Those pins marked as “N/A” have a range of applicable values that constitute proper operation.

Table 1: Pinout of the phyCORE-Connector X1

PIN ROW X1A				
PIN #	SIGNAL	I/O	SL	DESCRIPTION
1A	NVCC_7	O	NVCC_7	LCD Reference Voltage (1.5 V-3.0 V)
2A	GND	-	0	Ground 0 V
3A	x_LC_SD_D_CLK	O	NVCC_7	LCD Serial interface clock
4A	x_LC_PAR_RS	O	NVCC_7	Data/command select for parallel LCD interface
5A	x_LC_VSYNC0	I/O	NVCC_7	Display 0 vertical synchronization pulse
6A	x_LC_READ	O	NVCC_7	System-80: READ System 68K: ENABLE In byte enable mode System-80: READ_L System-68K: ENABLE_L
7A	GND	-	0	Ground 0 V
8A	x_LC_D3_REV	O	NVCC_7	REV signal for Sharp display 3
9A	x_LC_ D3_SPL	O	NVCC_7	SPL signal for Sharp display 3
10A	x_LC_ DRDY0	O	NVCC_7	Keyboard row 4 scan output pin of the µC
11A	x_LC_FPLINE	O	NVCC_7	Display 3 horizontal synchronization pulse (FPLINE/HSYNC/LP)
12A	GND	-	0	Ground 0V
13A	x_LC_D0	I/O	NVCC_7	Input/Output data to display.
14A	x_LC_D2	I/O	NVCC_7	Input/Output data to display.
15A	x_LC_D3	I/O	NVCC_7	Input/Output data to display.
16A	x_LC_D5	I/O	NVCC_7	Input/Output data to display.
17A	GND	-	0	Ground 0 V
18A	x_LC_D8	I/O	NVCC_7	Input/Output data to display.
19A	x_LC_D10	I/O	NVCC_7	Input/Output data to display.
20A	x_LC_D11	I/O	NVCC_7	Input/Output data to display.
21A	x_LC_D13	I/O	NVCC_7	Input/Output data to display.
22A	GND	-	0	Ground 0 V
23A	x_LC_D17	O	NVCC_7	Output data to display. In byte enable mode, READ_H (for sys80) or ENABLE_H (for sys68k)
24A	x_/CS0	O	3.3 V	/CS0 output (per default used by NOR-Flash)
25A	x_/CS1	O	3.3 V	/CS1 output (per default used by Ethernet)
26A	x_/CS4	O	3.3 V	/CS4 output (per default used by SRAM)
27A	GND	-	0	Ground 0 V
28A	x_/EB1	O	3.3 V	X_/EB1 corresponds to DATA_OUT[15:8] and M_DATA_OUT[15:8].
29A	x_/OE	O	3.3 V	Output Enable.

30A	x_/LBA	O	3.3 V	Load Burst Address
31A	x_/CLK	O	3.3 V	Burst Clock
32A	GND	-	0	Ground 0 V
33A	x_A2	O	3.3 V	Address-Line A2
34A	x_A4	O	3.3 V	Address-Line A4
35A	x_A5	O	3.3 V	Address-Line A5
36A	x_A7	O	3.3 V	Address-Line A7
37A	GND	-	0	Ground 0 V
38A	x_A10	O	3.3 V	Address-Line A10
39A	x_A12	O	3.3 V	Address-Line A12
40A	x_A13	O	3.3 V	Address-Line A13
41A	x_A15	O	3.3 V	Address-Line A15
42A	GND	-	0	Ground 0 V
43A	x_A18	O	3.3 V	Address-Line A18
44A	x_A20	O	3.3 V	Address-Line A20
45A	x_A21	O	3.3 V	Address-Line A21
46A	x_A23	O	3.3 V	Address-Line A23
47A	GND	-	0	Ground 0 V
48A	x_D0	I/O	3.3 V	Data-Bus D0
49A	x_D2	I/O	3.3 V	Data-Bus D2
50A	x_D3	I/O	3.3 V	Data-Bus D3
51A	x_D5	I/O	3.3 V	Data-Bus D4
52A	GND	-	0	Ground 0 V
53A	x_D8	I/O	3.3 V	Data-Bus D8
54A	x_D10	I/O	3.3 V	Data-Bus D10
55A	x_D11	I/O	3.3 V	Data-Bus D11
56A	x_D13	I/O	3.3 V	Data-Bus D13
57A	GND	-	0	Ground 0 V
58A	x_PC_BVD1	I	3.3 V	PCMCIA Battery Voltage Detect Input 1
59A	x_PC_BVD2	I	3.3 V	PCMCIA Battery Voltage Detect Input 2
60A	x_/PC_CD1	I	3.3 V	PCMCIA Card Detect Input 1
61A	x_PC_PWRON	I	3.3 V	PCMCIA Power is On Signal
62A	GND	-	0	Ground 0 V
63A	x_PCnRW	O	3.3 V	PCMCIA External Transceiver Direction Signal
64A	x_PC_VS1	I	NVCC_3_4_6	PCMCIA Voltage sense Input 1
65A	x_PC_VS2	I	NVCC_3_4_6	PCMCIA Voltage sense Input 2
66A	x_/CE1	O	NVCC_3_4_6	PCMCIA Card Enable 1 Signal
67A	GND	-	0	Ground 0 V
68A	x_IOS16	I	NVCC_3_4_6	PCMCIA I/O port is 16-bits
69A	x_CSI_D5	I	NVCC_3_4_6	Camera Sensor D5
70A	x_/ATA_CS0	O	NVCC_3_4_6	ATA bus chip select 0
71A	x_ATA_IORDY	I	NVCC_3_4_6	ATA bus IORDY
72A	GND	-	0	Ground 0 V

73A	x_/ATA_RESET	O	NVCC_3_4_6	ATA bus reset signal
74A	x_ATA_DMARQ	I	NVCC_3_4_6	ATA bus DMA request
75A	x_ATA_BUFFER_EN	O	NVCC_3_4_6	Buffer enable for external bus transceiver
76A	x_ATA_DA0	O	NVCC_3_4_6	ATA bus address line 2
77A	GND	-	0	Ground 0 V
78A	x_ATA_DATA0	I/O	NVCC_3_4_6	ATA data bus D0
79A	x_ATA_DATA2	I/O	NVCC_3_4_6	ATA data bus D2
80A	x_ATA_DATA3	I/O	NVCC_3_4_6	ATA data bus D3
81A	x_ATA_DATA5	I/O	NVCC_3_4_6	ATA data bus D5
82A	GND	-	0	Ground 0 V
83A	x_ATA_DATA8	I/O	NVCC_3_4_6	ATA data bus D8
84A	x_ATA_DATA10	I/O	NVCC_3_4_6	ATA data bus D10
85A	x_ATA_DATA11	I/O	NVCC_3_4_6	ATA data bus D11
86A	x_ATA_DATA13	I/O	NVCC_3_4_6	ATA data bus D13
87A	GND	-	0	Ground 0 V
88A	x_KEY_COL0	I/O	NVCC_3_4_6	Keypad Port Column 0
89A	x_KEY_COL1	I/O	NVCC_3_4_6	Keypad Port Column 1
90A	x_KEY_COL2	I/O	NVCC_3_4_6	Keypad Port Column 2
91A	x_KEY_ROW0	I/O	NVCC_3_4_6	Keypad Port Row 0
92A	GND	-	0	Ground 0 V
93A	x_KEY_ROW3	I/O	NVCC_3_4_6	Keypad Port Row 3
94A	x_KEY_ROW5	I/O	NVCC_3_4_6	Keypad Port Row 5
95A	x_GPIO3_1	I/O	NVCC_1	GPIO3_1
96A	NVCC_3_4_6	-	NVCC_3_4_6	ATA Reference Voltage (2.775 V)
97A	GND	-	0	Ground 0 V
98A	x_GPIO1_3	I/O	NVCC_1	GPIO1_3
99A	x_GPIO1_5	I/O	NVCC_1	GPIO1_5
100A	x_GPIO1_6	I/O	NVCC_1	GPIO1_6

PIN ROW X1B				
PIN #	SIGNAL	I/O	SL	DESCRIPTION
1B	x_LC_SD_D_I	I	NVCC_7	Data in for Serial Display
2B	x_LC_SD_D_IO	I/O	NVCC_7	Data in/out for Serial Display
3B	x_LC_SER_RS	O	NVCC_7	Data/command select for serial interface
4B	GND	-	0	Ground 0 V
5B	x_LC_FPFRAME	O	NVCC_7	Display 3 vertical synchronization pulse
6B	x_LC_WRITE	O	NVCC_7	System-80: WRITE System-68K: READ/WRITE In byte enable mode System-80: WRITE_L System-68K: READ/WRITE
7B	x_LC_CONTRAST	O	NVCC_7	Contrast control for the primary displays 0 and 3
8B	x_LC_D3_CLS	O	NVCC_7	CLS signal for Sharp display 3
9B	GND	-	0	Ground 0 V
10B	x_LC_BCLK	O	NVCC_7	Display clocking signal to the synchronous display (display 3). It matches the FPSHIFT / DOTCLC / LSCLC / DCLK / CLOCK inputs of supported displays.
11B	x_LC_x_LCS0	O	NVCC_7	Chip select signal for the for the asynchronous (smart) primary display (display 0).
12B	x_LC_x_LCS1	O	NVCC_7	Chip select signal for the for the asynchronous (smart) secondary display (display 1).
13B	x_LC_D1	I/O	NVCC_7	Input/Output data to display.
14B	GND	-	0	Ground 0 V
15B	x_LC_D4	I/O	NVCC_7	Input/Output data to display.
16B	x_LC_D6	I/O	NVCC_7	Input/Output data to display.
17B	x_LC_D7	I/O	NVCC_7	Input/Output data to display.
18B	x_LC_D9	I/O	NVCC_7	Input/Output data to display.
19B	GND	-	0	Ground 0 V
20B	x_LC_D12	I/O	NVCC_7	Input/Output data to display.
21B	x_LC_D14	I/O	NVCC_7	Input/Output data to display.
22B	x_LC_D15	I/O	NVCC_7	Input/Output data to display.
23B	x_LC_D16	O	NVCC_7	Output data to display. In byte enable mode, WRITE_H (for sys80)
24B	GND	-	0	Ground 0 V
25B	x_/CS3	O	3.3 V	/CS3 output (not used)
26B	x_/CS5	O	3.3 V	/CS5 output (per default used by CAN on Baseboard)
27B	x_/EB0	O	3.3 V	X_/EB0 corresponds to DATA_OUT[7:0] and M_DATA_OUT[7:0].
28B	x_/WR	O	3.3 V	/Write Signal.
29B	GND	-	0	Ground 0 V
30B	x_WAIT	I	3.3 V	End current burst / WAIT

31B	x_A0	O	3.3 V	Address-Line A0
32B	x_A1	O	3.3 V	Address-Line A1
33B	x_A3	O	3.3 V	Address-Line A3
34B	GND	-	0	Ground 0 V
35B	x_A6	O	3.3 V	Address-Line A6
36B	x_A8	O	3.3 V	Address-Line A8
37B	x_A9	O	3.3 V	Address-Line A9
38B	x_A11	O	3.3 V	Address-Line A11
39B	GND	-	0	Ground 0 V
40B	x_A14	O	3.3 V	Address-Line A14
41B	x_A16	O	3.3 V	Address-Line A16
42B	x_A17	O	3.3 V	Address-Line A17
43B	x_A19	O	3.3 V	Address-Line A19
44B	GND	-	0	Ground 0 V
45B	x_A22	O	3.3 V	Address-Line A22
46B	x_A24	O	3.3 V	Address-Line A24
47B	x_A25	O	3.3 V	Address-Line A25
48B	x_D1	I/O	3.3 V	Data-Bus D1
49B	GND	-	0	Ground 0 V
50B	x_D4	I/O	3.3 V	Data-Bus D4
51B	x_D6	I/O	3.3 V	Data-Bus D6
52B	x_D7	I/O	3.3 V	Data-Bus D7
53B	x_D9	I/O	3.3 V	Data-Bus D9
54B	GND	-	0	Ground 0 V
55B	x_D12	I/O	3.3 V	Data-Bus D12
56B	x_D14	I/O	3.3 V	Data-Bus D14
57B	x_D15	I/O	3.3 V	Data-Bus D15
58B	x_/FL_WP	I	3.3 V	Flash Protection Signal
59B	GND	-	0	Ground 0 V
60B	x_/PC_CD2	I	NVCC_3_4_6	PCMCIA Card Detect Input 2
61B	x_PCPOE	O	NVCC_3_4_6	PCMCIA buffers output enable
62B	x_PC_READY	I	NVCC_3_4_6	PCMCIA Ready
63B	x_PC_RST	O	NVCC_3_4_6	PCMCIA Card Reset.
64B	GND	-	0	Ground 0 V
65B	x_/PC_WAIT	I	NVCC_3_4_6	PCMCIA Extend bus cycle. Input
66B	x_/CE2	O	NVCC_3_4_6	PCMCIA Card Enable 2 Signal
67B	NVCC_3_4_6	-	NVCC_3_4_6	PCMCIA Reference Voltage (2.775 V)
68B	x_CSI_D4	O	NVCC_3_4_6	Camera Sensor D4
69B	GND	-	0	Ground 0 V
70B	x_/ATA_CS1	O	NVCC_3_4_6	ATA bus chip select 1
71B	x_ATA_INTRQ	I	NVCC_3_4_6	ATA bus interrupt request
72B	x_/ATA_DIOR	O	NVCC_3_4_6	ATA bus read strobe
73B	x_/ATA_DIOW	O	NVCC_3_4_6	ATA bus write strobe

74B	GND	-	0	Ground 0 V
75B	x_/ATA_DMACK	O	NVCC_3_4_6	ATA bus DMA acknowledge
76B	x_ATA_DA1	O	NVCC_3_4_6	ATA bus address line 1
77B	x_ATA_DA2	O	NVCC_3_4_6	ATA bus address line 2
78B	x_ATA_DATA1	I/O	NVCC_3_4_6	ATA data bus D1
79B	GND	-	0	Ground 0 V
80B	x_ATA_DATA4	I/O	NVCC_3_4_6	ATA data bus D4
81B	x_ATA_DATA6	I/O	NVCC_3_4_6	ATA data bus D6
82B	x_ATA_DATA7	I/O	NVCC_3_4_6	ATA data bus D7
83B	x_ATA_DATA9	I/O	NVCC_3_4_6	ATA data bus D9
84B	GND	-	0	Ground 0 V
85B	x_ATA_DATA12	I/O	NVCC_3_4_6	ATA data bus D12
86B	x_ATA_DATA14	I/O	NVCC_3_4_6	ATA data bus D14
87B	x_ATA_DATA15	I/O	NVCC_3_4_6	ATA data bus D15
88B	NVCC_3_4_6	-	NVCC_3_4_6	ATA Reference Voltage (2.775 V)
89B	GND	-	0	Ground 0 V
90B	x_KEY_COL3	I/O	NVCC_3_4_6	Keypad Port Column 3
91B	x_KEY_ROW1	I/O	NVCC_3_4_6	Keypad Port Row 1
92B	x_KEY_ROW2	I/O	NVCC_3_4_6	Keypad Port Row 2
93B	x_KEY_ROW4	I/O	NVCC_3_4_6	Keypad Port Row 4
94B	GND	-	0	Ground 0 V
95B	x_GPIO1_0	I/O	NVCC_1	GPIO1_0
96B	x_GPIO1_1	I/O	NVCC_1	GPIO1_1
97B	x_GPIO1_2	I/O	NVCC_1	GPIO1_2
98B	x_GPIO1_4	I/O	NVCC_1	GPIO1_4
99B	GND	-	0	Ground 0 V
100B	x_CLKO	I/O	NVCC_1	Clock Output

PIN ROW X1C				
PIN #	SIGNAL	I/O	SL	DESCRIPTION
1C	VIN	-	Power	Main Power Input (3.3 V-4.65 V)
2C	VIN	-	Power	Main Power Input (3,.3 V-4.65 V)
3C	GND	-	0	Ground 0 V
4C	VIN	-	Power	Main Power Input (3.3 V-4.65 V)
5C	VIN	-	Power	Main Power Input (3.3 V-4.65 V)
6C	x_VBAT	-	Power	Backup Voltage of SRAM and I²C-RTC
7C	GND	-	0	Ground 0 V
8C	VCC_3V3	-	Power	Power for 3.3 V devices
9C	VCC_3V3	-	Power	Power for 3.3 V devices
10C	VCC_3V3	-	Power	Power for 3.3 V devices
11C	VCC_3V3	-	Power	Power for 3.3 V devices
12C	GND	-	0	Ground 0 V
13C	x_Power_BATT	I	VATLAS (2.50 V-2.86 V)	1. Battery positive terminal 2. Battery current sensing point 2 3. Battery supply voltage sense
14C	x_BATTISNS	I	VATLAS	Battery current sensing point 1
15C	x_BATTFET	O	VATLAS	Driver output for battery path FET
16C	x_CHRGISNSP	I	VATLAS	Charge current sensing point 1
17C	GND	-	0	Ground 0 V
18C	x_LICELL	I	MV	1. Coincell supply input 2. Coincell charger output
19C	x_CHRGLED	O	EHV	Trickle LED driver output
20C	x_CHRGMOD0	I	VATLAS	Selection of the mode of charging
21C	x_CHRGMOD1	I	VATLAS	Selection of the mode of charging
22C	GND	-	0	Ground 0 V
23C	x_RXOUTL_LSPP	O	VAUDIO	J19=1+2: Low power receive output for accessories left channel J19=2+3: Loudspeaker positive terminal
24C	x_RXOUTR_LSPM	O	VAUDIO	J20=2+3: Low power receive output for accessories right channel J20=2+3: Loudspeaker minus terminal
25C	x_RXINL	I	VAUDIO	Receive input left channel
26C	x_RXINR	I	VAUDIO	Receive input right channel
27C	GND	-	0	Ground 0 V
28C	x_MC1RIN	I	VAUDIO	right microphone amplifier input
29C	x_MC1LIN	I	VAUDIO	left microphone amplifier input
30C	x_/ON1	I	LV	Power on/off button connection 1
31C	x_/ON2	I	LV	Power on/off button connection 2
32C	GND	-	0	Ground 0 V

33C	x_/LED2	O	3.3 V	Ethernet Link & Activity Indicator (Open Drain)
34C	x_/LED1	O	3.3 V	Ethernet Speed Indiator (Open Drain)
35C	x_ETH_TPI-	I/O	3.3 V	Receive negative input (normal) Transmit negative output (reversed)
36C	x_ETH_TPO-	I/O	3.3 V	Transmit negative output (normal) Receive negative input (reversed)
37C	GND	-	0	Ground 0 V
38C	x_ETH_Wkp	O	3.3 V	Wakeup Indicator output (Open Drain)
39C	x_CPU_/DE	I	NVCC_3_4_6	JTAG Debug Enable
40C	x_CPU_RTCK	O	NVCC_3_4_6	JTAG ARM Debug Test Clock
41C	x_CPU_/TRST	I	NVCC_3_4_6	JTAG reset
42C	GND	-	0	Ground 0 V
43C	x_/BATTDET	O	LV (VIOLO)	Battery thermistor presence detect output
44C	x_ADIN5	O	LV (VIOLO)	Analog Input Channel 5
45C	x_ADIN6	O	LV (VIOLO)	Analog Input Channel 6
46C	x_ADIN7	O	LV (VIOLO)	Analog Input Channel 7
47C	GND	-	0	Ground 0 V
48C	x_ADOUT	O	LV (VIOLO)	ADC trigger output
49C	X_ADTRIG	I	LV (VIOLO)	ADC trigger input
50C	x_/LOWBAT	O	LV (VIOLO)	Low battery indicator signal or end of life indicator signal
51C	x_USEROFF	I	LV (VIOLO)	User off signalling from processor
52C	GND	-	0	Ground 0 V
53C	x_VBUS	I/O	5 V	USB VBUS voltage
54C	x_UDM	I/O	3.3 V	USB transceiver cable interface, D-
55C	x_UDP	I/O	3.3 V	USB transceiver cable interface, D+
56C	x_UID	I/O	3.3 V	USB on the go transceiver cable ID resistor connection
57C	GND	-	0	Ground 0 V
58C	x_USB_OC	I	NVCC_5_10	USB Generic Over Current input
59C	x_USB_PWR	O	NVCC_5_10	USB Generic Power switch output
60C	x_USBHOST2_CLK	I	NVCC_5_10	USB Host transceiver ULPI clock signal
61C	x_USBHOST2_DIR	I	NVCC_5_10	USB Host transceiver ULPI direction signal
62C	GND	-	0	Ground 0 V
63C	x_USBHOST2_DA2	I/O	NVCC_5_10	USB Host transceiver ULPI data signal D2
64C	x_USBHOST2_DA4	I/O	NVCC_5_10	USB Host transceiver ULPI data signal D4
65C	x_USBHOST2_DA6	I/O	NVCC_5_10	USB Host transceiver ULPI data signal D6
66C	NVCC_5_10	-	NVCC_5_10	USB Reference Voltage (2.775 V)
67C	GND	-	0	Ground 0 V
68C	x_SD1_DATA0	I/O	NVCC_3_4_6	SD/MMC Data line both in 1-bit and 4-bit mode
69C	x_SD1_DATA1	I/O	NVCC_3_4_6	SD/MMC Data line or interrupt in 4-bit mode Interrupt in 1-bit mode
70C	x_SD1_DATA2	I/O	NVCC_3_4_6	SD/MMC Data line or interrupt in 4-bit mode Interrupt in 1-bit mode

71C	x_SD1_DATA3	I/O	NVCC_3_4_6	SD/MMC Card detect in power up, Data line in 4-bit mode, Not used in 1-bit mode
72C	GND	-	0	Ground 0 V
73C	x_RTS_DCE1_TTL	I	NVCC_8	Request to send UART1
74C	x_CTS_DCE1_TTL	O	NVCC_8	Clear to send UART1
75C	x_RI_DCE1_TTL	O	NVCC_8	Ring indicator UART1
76C	x_DCD_DCE1_TTL	O	NVCC_8	Data carrier detected UART1
77C	GND	-	0	Ground 0 V
78C	x_TXD_DTE2_TTL	O	NVCC_8	Serial data transmit UART2
79C	x_CTS_DTE2_TTL	O	NVCC_8	Clear to send UART2
80C	x_DSR_DTE2_TTL	I	NVCC_8	Data set ready UART2
81C	x_DCD_DTE2_TTL	I	NVCC_8	Data carrier detected UART2
82C	GND	-	0	Ground 0 V
83C	x_I2C2_SCL	I/O	NVCC_5_10	I²C 2 Serial Clock
84C	x_I2C2_SDA	I/O	NVCC_5_10	I²C 2 Serial Data
85C	x_I2C3_SDA	I/O	NVCC_5_10	I²C 3 Serial Data
86C	x_CSPI1_SCLK	I/O	NVCC_3_4_6	SPI 1 clock
87C	GND	-	0	Ground 0 V
88C	x_CSPI1_SS1	I/O	NVCC_3_4_6	SPI 1 Chip select 1
89C	x_CSPI1_SS3	I/O	NVCC_3_4_6	SPI 1 Chip select 3
90C	x_CSPI1_SPI_RDY	I/O	NVCC_3_4_6	SPI 1 SPI data ready in Master mode
91C	x_MCU1_26	I/O	NVCC_5_10	GPIO MCU1_26
92C	GND	-	0	Ground 0 V
93C	x_MCU2_0	I/O	NVCC_3_4_6	GPIO MCU2_0 (NVCC_9)
94C	x_MCU2_2	I/O	NVCC_3_4_6	GPIO MCU2_2 (NVCC_9)
95C	x_MCU2_3	I/O	NVCC_3_4_6	GPIO MCU2_3 (NVCC_9)
96C	x_MCU3_3	I/O	NVCC_3_4_6	GPIO MCU3_3 (NVCC_9)
97C	GND	-	0	Ground 0 V
98C	x_BOOT_MODE2	I/O	NVCC_1	Boot-Mode 2
99C	x_COMPARE	I/O	NVCC_1	Timer Output Compare for timers 1 2 3.
100C	NVCC1	-	NVCC_1	USB Reference Voltage (1.8 V)

PIN ROW X1D				
PIN #	SIGNAL	I/O	SL	DESCRIPTION
1D	VIN	-	Power	Main Power Input (3.3 V-4.65 V)
2D	VIN	-	Power	Main Power Input (3,.3 V-4.65 V)
3D	GND	-	0	Ground 0 V
4D	x_/RESET_3V3	O	3.3 V	3.3 V Version of x_/RESET
5D	x_/RESET	I/O	NVCC_1	Reset Input/Output
6D	x_/RESET_MCU	I/O	NVCC_1	Reset Input/Output directly connected to the uC
7D	x_iMX31_FUSE	I	3.0 V	Fusebox write (program) Supply Voltage (3.0 V)
8D	x_TOUT	O	3.3 V	Open-Drain Thermostat Output of U16 (DS75)
9D	GND	-	0	Ground 0 V
10D	x_Charger_Input	I	EHV (max. 20 V)	Charger Input
11D	x_Charger_Input	I	EHV	Charger Input
12D	x_Charger_Input	I	EHV	Charger Input
13D	x_Charger_Input	I	EHV	Charger Input
14D	GND	-	0	Ground 0 V
15D	x_CHRGISNSN	I	VATLAS	Charge current sensing point 2
16D	x_BFET	O	EHV	1. Driver output for dual path regulated BP FET 2. Driver output for separate USB charger path FET
17D	x_CHRGCTL	O	EHV	Driver output for charger path FET's
18D	x_PWRRDY	O	LV	Power ready signal after DVS and power gate transition
19D	GND	-	0	Ground 0 V
20D	x_GPO1	O	LV	General purpose output 1
21D	x_GPO2	O	LV	General purpose output 2
22D	x_RXD3_RS232	O	RS232 / NVCC_3_4_6	Serial data receive line UART3
23D	x_TXD3_RS232	O	RS232 / NVCC_3_4_6	Serial data transmit line UART3
24D	GND	-	0	Ground 0 V
25D	x_RTS3_RS232	O	RS232 / NVCC_3_4_6	Request to send UART3
26D	x_CTS3_RS232	O	RS232 / NVCC_3_4_6	Clear to send UART3
27D	x_GPO3	O	LV	General purpose output 3
28D	x_GPO4	O	LV	General purpose output 4
29D	GND	-	0	Ground 0 V
30D	x_TSX1	O	LV	ADC generic input channel 12 or touchscreen input X1, group 2
31D	x_TSX2	O	LV	ADC generic input channel 13 or touchscreen input X2, group 2

32D	x_TSY1	O	LV	ADC generic input channel 14 or touchscreen input Y1, group 2
33D	x_TSY2	O	LV	ADC generic input channel 15 or touchscreen input Y2, group 2
34D	GND	-	0	Ground 0 V
35D	x_ETH_TPI+	I/O	3.3 V	Receive positive input (normal) Transmit positive output (reversed)
36D	x_ETH_TPO+	I/O	3.3 V	Transmit positive output (normal) Receive positive input (reversed)
37D	x_/ON3	I	LV	Power on/off button connection 3
38D	x_CPU_TCK	I	NVCC_3_4_6	JTAG clock
39D	GND	-	0	Ground 0 V
40D	x_CPU_TDI	I	NVCC_3_4_6	JTAG Data In
41D	x_CPU_TDO	O	NVCC_3_4_6	JTAG Data Out
42D	x_CPU_TMS	I	NVCC_3_4_6	JTAG Mode select
43D	x_CPU_SJC_MOD	I	NVCC_3_4_6	JTAG Mode
44D	GND	-	0	Ground 0 V
45D	x_ADIN8	O	LV (VIOLO)	Analog Input Channel 8
46D	x_ADIN9	O	LV (VIOLO)	Analog Input Channel 9
47D	x_ADIN10	O	LV (VIOLO)	Analog Input Channel 10
48D	x_ADIN11	O	LV (VIOLO)	Analog Input Channel 11
49D	GND	-	0	Ground 0 V
50D	x_USBOTG_DA0	I/O	NVCC_5_10	USB OTG data signal 0
51D	x_USBOTG_DA3	I/O	NVCC_5_10	USB OTG data signal 3
52D	x_USBOTG_DA4	I/O	NVCC_5_10	USB OTG data signal 4
53D	x_USBOTG_DA5	I/O	NVCC_5_10	USB OTG data signal 5
54D	GND	-	0	Ground 0 V
55D	NVCC_5_10	-	NVCC_5_10	USB Reference Voltage (2.775 V)
56D	x_USB_HS_/PSW	O	5 V	USB-OTG Power switch output open drain
57D	x_USB_HS_FAULT	I	5 V	USB-OTG over current input signal
58D	x_USB_BYP	I	NVCC_5_10	USB Generic bypass input
59D	GND	-	0	Ground 0 V
60D	x_USBHOST2_STP	O	NVCC_5_10	USB Host transceiver ULPI stop signal
61D	x_USBHOST2_NXT	I	NVCC_5_10	USB Host transceiver ULPI next signal
62D	x_USBHOST2_DA0	I/O	NVCC_5_10	USB Host transceiver ULPI data signal D0
63D	x_USBHOST2_DA1	I/O	NVCC_5_10	USB Host transceiver ULPI data signal D1
64D	GND	-	0	Ground 0 V
65D	x_USBHOST2_DA3	I/O	NVCC_5_10	USB Host transceiver ULPI data signal D3
66D	x_USBHOST2_DA5	I/O	NVCC_5_10	USB Host transceiver ULPI data signal D5
67D	x_USBHOST2_DA7	I/O	NVCC_5_10	USB Host transceiver ULPI data signal D7
68D	x_SD1_CMD	I/O	NVCC_3_4_6	SD/MMC CMD line connect to card
69D	GND	-	0	Ground 0 V
70D	x_SD1_CLK	O	NVCC_3_4_6	SD/MMC Clock for MMC/SD/SDIO card

71D	NVCC_3_4_6	-	NVCC_3_4_6	SD/MMC Reference Voltage (2.775 V)
72D	x_TXD_DCE1_TTL	O	NVCC_8	Serial data transmit signal UART1
73D	x_RXD_DCE1_TTL	I	NVCC_8	Serial data receive signal UART1
74D	GND	-	0	Ground 0V
75D	x_DSR_DCE1_TTL	O	NVCC_8	Data set ready UART1
76D	x_DTR_DCE1_TTL	I	NVCC_8	Data terminal ready UART1
77D	x_RXD_DTE2_TTL	I	NVCC_8	Serial data receive UART2
78D	x_RTS_DTE2_TTL	I	NVCC_8	Request to send UART2
79D	GND	-	0	Ground 0 V
80D	x_RI_DTE2_TTL	I	NVCC_8	Ring indicator UART2
81D	x_DTR_DTE2_TTL	O	NVCC_8	Data terminal ready UART2
82D	x_MCU2_16	I/O	NVCC_3_4_6	GPIO MCU2_16 (NVCC_9)
83D	NVCC8	-	NVCC_8	Serial Interface Reference Voltage (2.775 V)
84D	GND	-	0	Ground 0 V
85D	x_I2C3_SCL	I/O	NVCC_5_10	I²C 3 Serial Clock
86D	x_CSPI1_MOSI	I/O	NVCC_3_4_6	SPI 1 Chip select 1
87D	x_CSPI1_MISO	I/O	NVCC_3_4_6	SPI 1 Master data in; slave data out
88D	x_CSPI1_SS2	I/O	NVCC_3_4_6	SPI 1 Chip select 2
89D	GND	-	0	Ground 0 V
90D	x_MCU1_25	I/O	NVCC_5_10	GPIO MCU1_25
91D	x_1Wire	I/O	NVCC_5_10	1-Wire bus.
92D	NVCC_5_10	-	NVCC_5_10	1-Wire Reference Voltage (2.775 V)
93D	x_MCU2_1	I/O	NVCC_3_4_6	GPIO MCU2_1 (NVCC_9)
94D	GND	-	0	Ground 0 V
95D	x_MCU3_2	I/O	NVCC_3_4_6	GPIO MCU3_2 (NVCC_9)
96D	VSIM	-	VSIM	VSIM Suply Voltage
97D	x_CLKSS	I/O	NVCC_1	Clock Source select input.
98D	x_BOOT_MODE4	I/O	NVCC_1	Boot-Mode 4
99D	GND	-	0	Ground 0 V
100D	x_CAPTURE	I	NVCC_1	Timer input Capture or Timer1 input clock

3 Jumpers

For configuration purposes, the phyCORE-i.MX31 has 22 solder jumpers, some of which have been installed prior to delivery. *Figure 5* illustrates the numbering of the solder jumper pads, while *Figure 6* and *Figure 7* indicate the location of the solder jumpers on the board. Six solder jumpers are located on the top side of the module (opposite side of connectors). *Figure 5* below provides a functional summary of the solder jumpers, their default positions, and possible alternative positions and functions. A detailed description of each solder jumper can be found in the applicable section listed in the table.

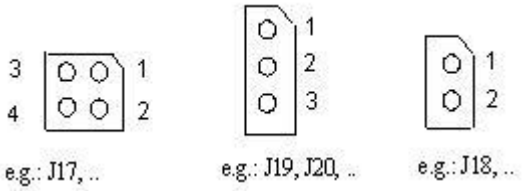

Figure 5: Numbering of the Jumper Pads

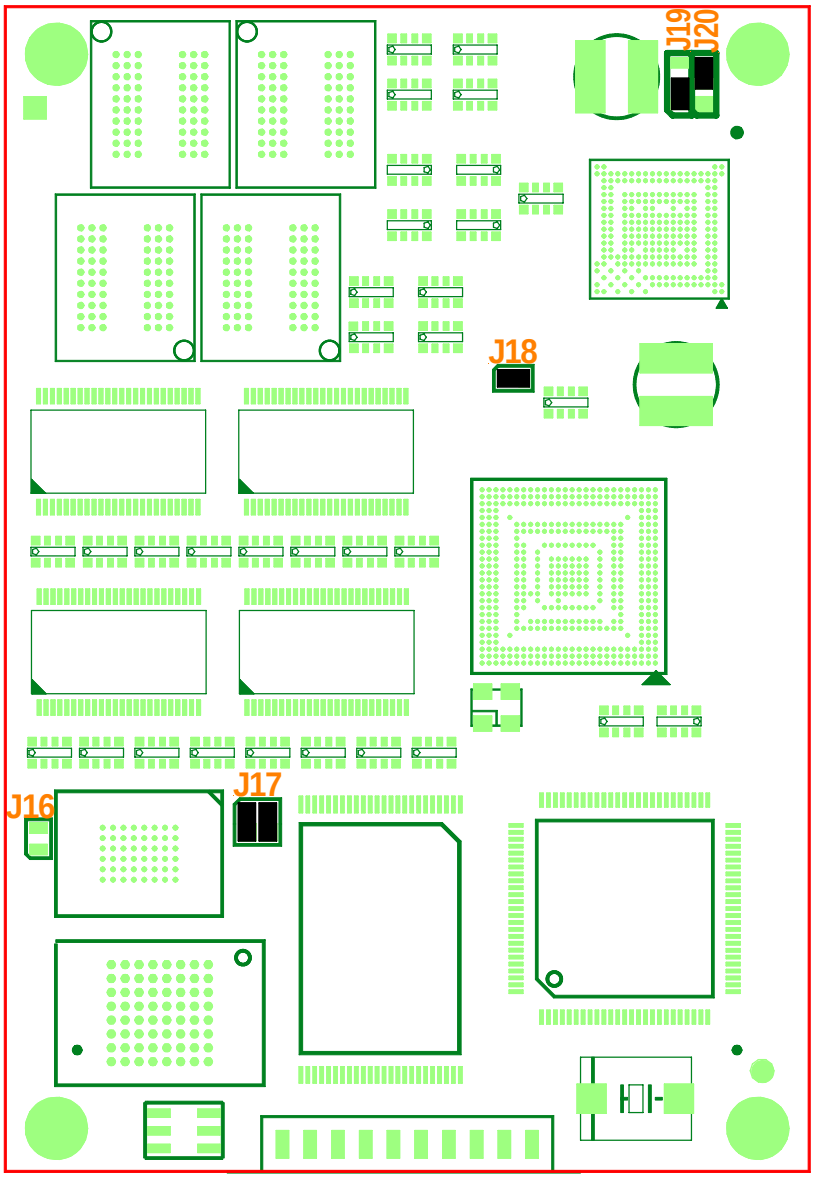

Figure 6: Location of the Jumpers (Top View)

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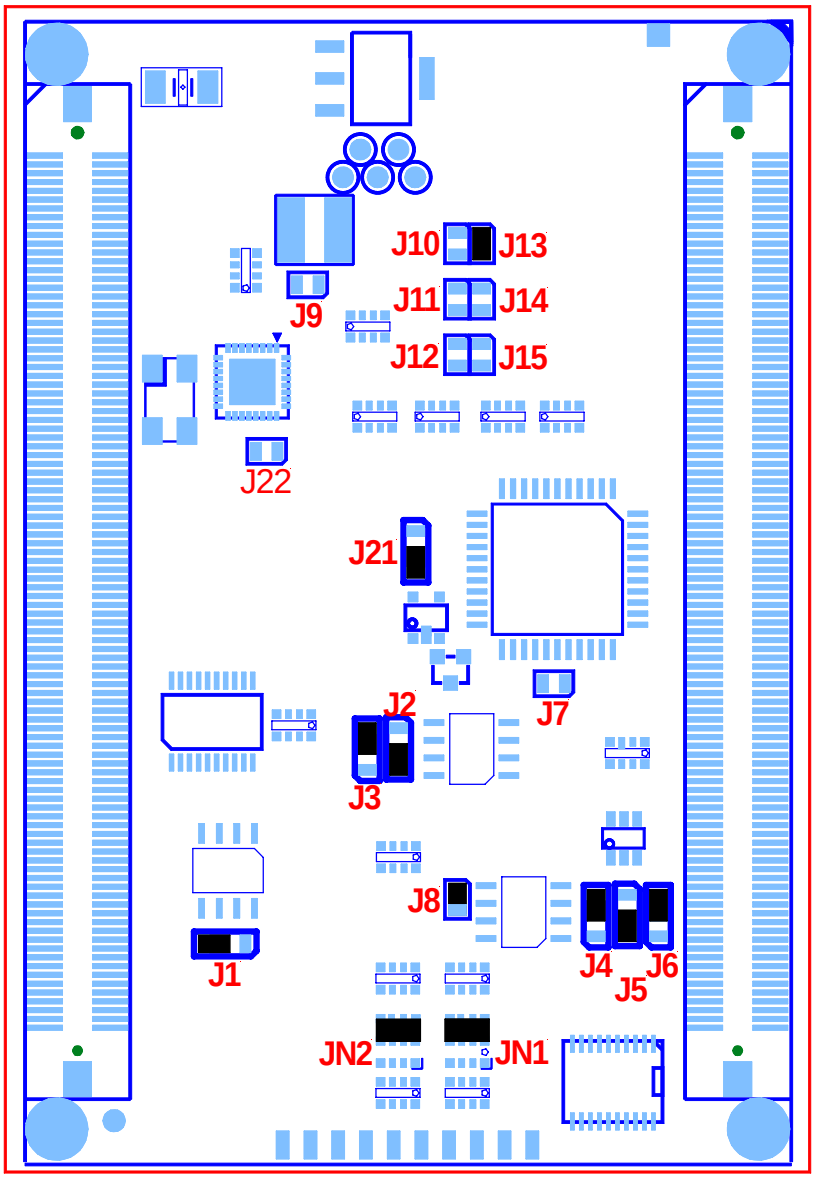

Figure 7: Location of the Jumpers (Bottom View)

The jumpers (J = solder jumper) have the following functions:

Table 2: Jumper Settings

	Default Setting		Alternative Setting		See Section
J1	2 + 3	Selects x8 organization of Ethernet EEPROM U4.	1 + 2	Selects x16 organization of Ethernet EEPROM U4.	
J2	2 + 3	Thermal Sensor U16 address bit A1 connected to VCC	1 + 2	Thermal Sensor U16 address bit A1 connected to GND	
J3	2 + 3	Thermal Sensor U16 address bit A2 connected to GND	1 + 2	Thermal Sensor U16 address bit A2 connected to VCC	
J4	2 + 3	EEPROM U17 address bit A0 connected to GND	1 + 2	EEPROM U17 address bit A0 connected to VCC	7.5.1.
J5	2 + 3	EEPROM U17 address bit A1 connected to VCC	1 + 2	EEPROM U17 address bit A1 connected to GND	
J6	2 + 3	EEPROM U17 address bit A2 connected to GND	1 + 2	EEPROM U17 address bit A2 connected to VCC	
J8	closed	EEPROM U17 is not write protected.	open	EEPROM U17 is write protected.	7.5.2.
J7	open	RAM-Bank input is high. (only DDR-RAM bank 0 is populated)	closed	RAM-Bank input is low. (DDR-RAM bank's 0 & 1 are populated)	
J9	open	WDRESET output from i.MX31 is not connected to WDI input of MC13783. Therefore Watchdog is disabled.	closed	WDRESET output from i.MX31 is connected to WDI input of MC13783. Therefore Watchdog is enabled.	
J10	open	Power up Mode select (PUMS1) is floating.	closed	Power up Mode select (PUMS1) is connected to VATLAS (high).	4
J11	open	Power up Mode select (PUMS1) is floating.	closed	Power up Mode select (PUMS1) is connected to GND (low).	
J12	open	Power up Mode select (PUMS2) is floating.	closed	Power up Mode select (PUMS2) is connected to VATLAS (high).	
J13	closed	Power up Mode select (PUMS2) is connected to GND (low).	open	Power up Mode select (PUMS2) is floating.	
J14	open	Power up Mode select (PUMS3) is floating.	closed	Power up Mode select (PUMS3) is connected to VATLAS (high).	
J15	open	Power up Mode select (PUMS3) is floating.	closed	Power up Mode select (PUMS3) is connected to GND (low).	
J16	open	Pin U19-E3 is left floating.	closed	Pin U19-E3 is connected to GND.	
J17	1 + 3	x_/EB1 is connected to /SRAM_LB.	1 + 2	x_/EB0 is connected to /SRAM_LB.	
J17	2 + 4	x_/EB0 is connected to /SRAM_UB.	3 + 4	x_/EB1 is connected to /SRAM_UB.	

J18	closed	CHRGMOD1 is connected to VATLAS (high)	open	CHRGMOD1 is floating (high-z)	
J19	1 + 2	RXOUTL is connected to X1 pin 23C.	2 + 3	LSPP is connected to X1 pin 23C.	
J20	2 + 3	RXOUTR is connected to X1 pin 24C.	2 + 3	LSPM is connected to X1 pin 24C.	
J21	2 + 3	FVCC is supplied by U23	1 + 2	FVCC is supplied by MC13783 VDIG	
J22	open	/RESET input of USB transceiver U22 is not connected to x_MCU2_1 and therefore pulled high.	closed	/RESET input of USB transceiver U22 is connected to x_MCU2_1 and can be controlled by the i.MX31.	

4 Power Requirements

The phyCORE-i.MX31 normally operates off two different voltage supplies denoted as VIN and VCC_3V3. The MC13783 primary on-board voltage regulator operates off VIN and generates all on-board supply voltages except 3.3 V. The VCC_3V3 input supplies this required voltage.

Because of its wide input voltage range VIN is ideally suited for a battery. VCC_3V3, however, has a very narrow input voltage range and must not be connected to a battery. A well regulated supply should be used for VCC_3V3.

The phyCORE-i.MX Carrier Board generates VCC_3V3 from VIN with a 3.3 V voltage regulator on the Carrier Board. VIN is sourced from either the wall socket input, or a battery. The Carrier Board also controls charging the battery when the wall socket is used. You should refer to this example circuitry when designing your own Carrier Board.

If your system does not require a battery then you can connect VIN and VCC_3V3 together and supply both inputs with a 3.3 V input voltage. This will simplify the design and reduce the component count. In this case make sure that the X_Charger_Input is connected to a power supply >4.4V. You also have to design a 0.02R resistor between X_POWER_BATT and X_BATTISNS and a 22µF capacitor at X_POWER_BATT. Put both components as close as possible to the module connector. (*see Figure 8 and Table 3*)

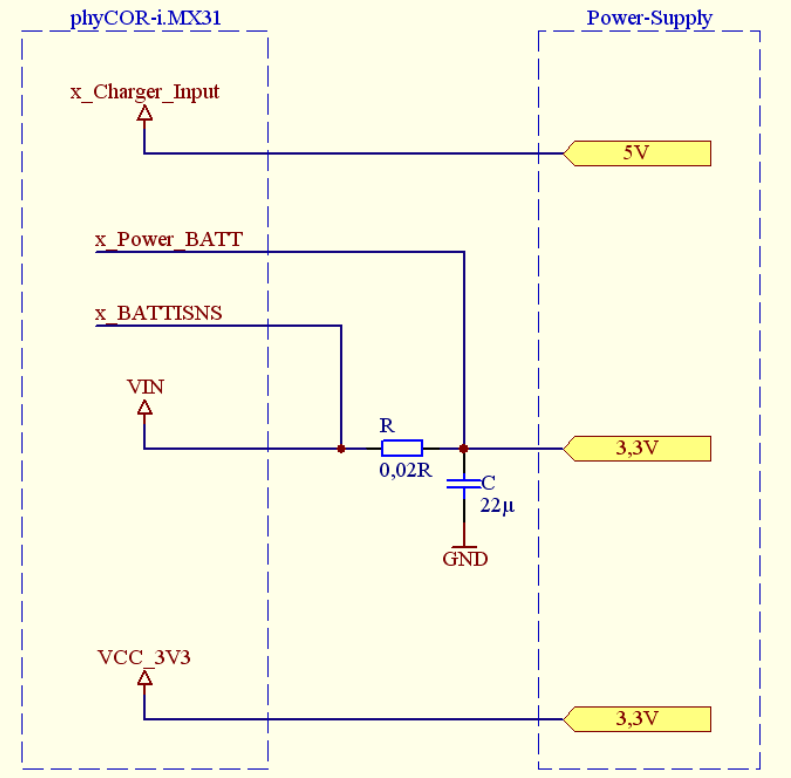

Figure 8: Minimum Circuit

Table 3: Power Supply for the Minimum Circuit

power supply	min.	typ.	max.
5 V (x_Charger_Input)	4.4 V	5 V	20 V
3.3 V (VIN)	3.25 V	3.3 V	4.5 V
3.3 V (VCC_3V3)	3,15 V	3.3 V	3.45 V

The input voltage range of VIN is from 3.1 V.. 4.65 V allowing a current draw of at least ***3*** A. VCC_3V3 should be in a range of 3.3 V ± 0.15 V (±0.05 V if VCC_3V3 is connected to VIN) with a nominal current allowance of at least 1.5 A.

See *Table 1* from *section 2* above for applicable VIN / VCC_3V3 power pins on the phyCORE-connector.

Caution!
Connect all VIN and VCC_3V3 input pins to your power supplies.

As a general design rule we recommend connecting all GND pins neighboring signals which are being used in the application circuitry.

The i.MX31 CPU is supplied by 21 different power domains. Some of them are connected together. The startup voltage levels are selected by the Power up Mode selection inputs (PUMS1..3) of the PMIC device MC13783. With the default settings of the input pins PUMS1..3 the voltages are the following:

Table 4: i.MX31 Default Power Input Voltages

MC13783 Power Output	**Power-Domain**	**startup Voltage-Level**
VAUDIO	internally used by MC13783	2.775 V
VIOLO	NVCC_1	1.8 V
VIOHI	NVCC_3_4_6	2.775 V
VDIG	FVCC / MVCC / UVCC / SVCC	1.5 V
VRFDIG	IOQVDD	1.875 V
VRFREF	NVCC_8	2.775 V
VSIM		off
VESIM	NVCC_9	2.775 V
VCAM	NVCC_7	2.775 V
VRF1	NVCC_5_10	2.775 V

In general you should not need to adjust the Power up Mode settings. The configuration has been optimized for the phyCORE-i.MX31 together with the phyCORE-i.MX Carrier Board.

5 Real Time Clock U18 / SRAM U19 Battery

The connection of a battery is not essential to the functioning of the phyCORE-i.MX31. The battery, interfaced as voltage supply signal x_VBAT through X1 pin 6C on the phyCORE-connector, provides power to the I²C Real Time Clock U18 (RTC8564JE) and the low power SRAM U19. This provides a means of time/memory keeping in the absence of power at the VCC_3V3 pins while drawing minimal power from the battery.

The x_VBAT (2.0 V < x_VBAT < VCC_3V3) input operating limits are listed in **Fehler! Verweisquelle konnte nicht gefunden werden.*Fehler! Verweisquelle konnte nicht gefunden werden.*** below.

Table 5: x_VBAT Operating Limits

	MIN	TYP	MAX	UNITS
x_VBAT	2.0	3.1 V	3.3 V	V

Caution!
Operation with x_VBAT greater than VCC_3V3 could cause unintentional discharge of the battery.

If you choose not to use a battery with the phyCORE-i.MX31 then x_VBAT should be connected to VCC_3V3 external to the phyCORE-i.MX31.

See section 12 for battery power consumption.

6 System Configuration

Although most features of the Freescale phyCORE-i.MX31 microcontroller are configured and/or programmed during the initialization routine, other features, which impact program execution, must be configured prior to initialization via pin termination.

6.1 System Startup Configuration

During the reset cycle the i.MX31 processor reads the state of selected controller signals to determine the basic system configuration. The configuration circuitries (pull-up or pull-down resistors) are located on the phyCORE module. They are already set, so no further settings are necessary.

6.1.1 Power-Up-Mode-Select (PUMS)

The Power-Management-IC (M13783) has three Power-Up-Mode-Selects. PUMS1 and PUMS2 determine the initial setup for the voltage level of the switchers and regulators and if they get enabled or not. With PUMS3 three different power up sequences are selectable.

The three states of the PUMS settings are:

- Pull-up (connected to VATLAS)
- Pull-down (connected to GND)
- Open (no jumper populated/left open)

For detailed information about PUMS and the power up sequence, refer to the MC13783 IC User's Guide, chapter 5.3 Power up.

The i.MX31 module (PCM-037) comes with a standard Power-Up-Mode-Select (see table below).

Table 6: Default PUMS for i.MX31 Module

PUMS1	**GND**
PUMS2	**GND**
PUMS3	**Open**

Note:
The i.MX31 controller has a defined power up sequence. *Refer to the i.MX31 Data Sheet, chapter 4.2.1 Powering Up.*

6.1.2 Boot Mode Select

The i.MX31 controller has different boot modes, which can be selected. The system boot mode of the processor is determined by the configuration of the five external input pins, BOOT[4:0].

Table 7: Boot Modes of i.MX31 Module

BOOT MODE SELECTION	BOOT MODE/DEVICE	TYPE
00000	Bootloader UART/USB	Internal
00001	8-bit NAND Flash (2Kbyte per page)	
00010	8-bit NAND Flash (512 Kbyte per page)	
00011	16-bit NAND Flash (2 Kbyte per page)	
00100	16-bit NAND Flash (512 bytes per page)	
00101	16-bit CS0 at D[15:0]	
00110-00111	Reserved	
01001	M-Systems Disk On Chip	
01001-01111	Reserved	
10000	8-bit NAND Flash (2Kbyte per page)	External
10001	8-bit NAND Flash (512 byte per page)	
10010	16-bit NAND Flash (2 Kbyte per page)	
10011	16-bit NAND (512 byte per page)	
10100	16-bit CS0 at D[15:0]	
10101-10110	Reserved	
10111	Reserved	
11xxx	Reserved	

The phyCORE-i.MX31 module comes with a standard boot configuration of **‘10100’**, so the system will boot from the 16-bit NOR-Flash at CS0.

7 System Memory

The phyCORE-i.MX31 provides three types of on-board memory:

- LP-DDR-SDRAM: 128 MByte (up to 256 MByte)
- SRAM: 512 KByte (up to 2 MByte)
- NAND Flash: 64 MByte (up to 1 GByte)
- NOR Flash: 32 MByte (upt to 64 MByte)
- I²C-EEPROM: 4 KB (up to 32 KByte)

It should be noted that the LP-DDR-SDRAM has a dedicated memory bus to the i.MX31 microcontroller. The LP-DDR-SDRAM is therefore not made available at the phyCORE-connector X1.

7.1 Memory Model

The i.MX31 memory map is summarized in *Table 8* below. *For a detailed view of the memory map please consult the Freescale's i.MX31 User's Manual*.

Table 8: i.MX31 Memory Map

ADDRESS	CHIP-SELECT	FUNCTION
0x8000 00000 – 0x8FFF FFFF	/CSD0 (/CS2)	LP-DDR-SDRAM Bank 0 (U5, U7)
0x9000 00000 – 0x9FFF FFFF	/CSD1 (/CS3)	LP-DDR-SDRAM Bank 1 (U6, U8)
0xA000 00000 – 0xA7FF FFFF	/CS0	NOR-Flash (U15)
0xA800 00000 – 0xAFFF FFFF	/CS1	Ethernet Controller (U3)
0xB400 00000 – 0xB5FF FFFF	/CS4	SRAM (U19)
0xB600 00000 – 0xB6FF FFFF	/CS5	not used on phyCORE-i.MX31 (SJA1000 on baseboard)

7.2 LP-DDR-SDRAM (U5-U8)

The phyCORE-i.MX31 has the possibility to use two LP-DDR-SDRAM banks with 133 MHz. They are configured for 32-bit access using two 16-bit wide RAM chips at Bank 0 (U5,U7) and Bank 1 (U6,U8).

The i.MX31 is capable of addressing two RAM bank's located at memory address 0x8000 0000 (/CSD0) and 0x9000 0000 (/CSD1). If RAM bank U6/U8 is not populated the chip select line can be used as /CS3.

LP-DDR-SDRAM initialization is performed by a boot loader or the operating system following a power-on reset and must not be changed at a later point by any application code. When writing custom code independent of an operating system or boot loader, SDRAM must be initialized by accessing the appropriate SDRAM configuration registers on the i.MX31 controller. *Refer to the i.MX31 User Manual for accessing and configuring these registers.*

7.3 NOR-Flash (U15)

The phyCORE-i.MX31 can be populated with an Intel Strata Flash on U15. This NOR-Flash is connected to /CS0 which is located at memory address 0xA000 0000.
The entire Flash can be write protected by pulling the signal x_/FL_WP pin on X1 58B low.

The following NOR-Flash devices can be used on the phyCORE-i.MX31:

Table 9: Compatible NOR Flash Devices

MANUFACTURER	NOR FLASH P/N	DENSITY (MBYTE)
Intel	PC28F640P33	8 MBYTE
Intel	PC28F128P33	16 MBYTE
Intel	PC28F256P33	32 MBYTE

7.4 NAND Flash Memory (U14)

Use of Flash as non-volatile memory on the phyCORE-i.MX31 provides an easily reprogrammable means of code storage. The following Flash devices can be used on the phyCORE-i.MX31:

Table 10: Compatible NAND Flash Devices

MANUFACTURER	NAND FLASH P/N	DENSITY (MBYTE)
ST Microelectronics	NAND512W3A2CN6	64

Additionally, any parts that are footprint (TSOP48) and functionally compatible with the NAND Flash devices listed above may also be used with the phyCORE-i.MX31.

These Flash devices are programmable with 3.3 V. No dedicated programming voltage is required.

As of the printing of this manual, these NAND Flash devices generally have a life expectancy of at least 100,000 erase/program cycles and a data retention rate of 10 years.

7.4.1 8/16-Bit-NAND Flash Usage (JN1,JN2,RN41,RN42)

The i.MX31 is capable of using 8-Bit and 16-Bit NAND Flash devices. To select between 8-and 16-bit NAND-Flash's, the Jumpers/Resistor-Networks has to be populated as follows:

Table 11: JN1/2,RN41/42 Nand-Flash Bit Width Selection[1]

NAND-FLASH BIT WIDTH	JN1/2	RN41/42
8-bit	**2-3/5-6/8-9/11-12**	**not populated**
16-it	1-2/4-5/7-8/10-11	populated

7.5 I²C EEPROM (U17)

The phyCORE-i.MX31 is populated with a ST 24W32C[2] non-volatile 4 KByte EEPROM (U17) with an I²C interface to store configuration data or other general purpose data. This device is accessed through I²C port 2 on the i.MX31. The serial clock signal and serial data signal for I²C port 2 are made available at the phyCORE-connector as x_I2C2_SDA on X1 pin 84C and x_I2C2_SCL on X1 pin 83C.

Three solder jumpers are provided to set the lower address bits: J4, J5, and J6. *Refer to section 3 for details on setting these jumpers.*

Write protection to the device is accomplished via jumper J8. By default this jumper is closed, allowing write access to the EEPROM memory. Removing this jumper will cause the EEPROM to enter write protect mode, thereby disabling write access to the device. *Refer to section 7.5.2for further details on setting this jumper.*

1 Default settings are in **bold blue** text

2 See the manufacturer's data sheet for interfacing and operation.

7.5.1Setting the EEPROM Lower Address Bits (J4, J5, J6)

The 4 KByte I²C EEPROM populating U17 on the phyCORE-module has the capability of configuring the lower address bits A0, A1, and A2. The four upper address bits of the device are fixed at '1010' (*see ST 24W32C data sheet).* The remaining three lower address bits of the seven bit I²C device address are configurable using jumpers J4, J5 and J6. J4 sets address bit A0, J5 address bit A1, and J6 address bit A2. *Table 12* below shows the resulting seven bit I²C device address for the eight possible jumper configurations.

The following configurations are possible:

Table 12: J4, J5, J6 EEPROM Lower Address Bits[1]

I²C DEVICE ADDRESS	J6	J5	J4
1010 010	**2 + 3**	**2 + 3**	**2 + 3**
1010 011	2 + 3	2 + 3	1 + 2
1010 000	2 + 3	1 + 2	2 + 3
1010 001	2 + 3	1 + 2	1 + 2
1010 110	1 + 2	2 + 3	2 + 3
1010 111	1 + 2	2 + 3	1 + 2
1010 100	1 + 2	1 + 2	2 + 3
1010 101	1 + 2	1 + 2	1 + 2

1 Default settings are in **bold blue** text

7.5.2EEPROM Write Protection Control (J8)

Jumper J8 controls write access to the EEPROM (U17) device. Closing this jumper allows write access to the device, while opening this jumper enables write protection.

The following configurations are possible:

Table 13: J8, EEPROM Write Protection States[1]

EEPROM Write Protection State	J8
Write Access Allowed	**closed**
Write Protected	open

1 Default settings are in **bold blue** text

8 Serial Interface

8.1 RS-232 Transceiver (U21)

One high-speed RS-232 transceiver supporting 460kbps data rates populate the phyCORE-i.MX31 at U21. These device convert the signal levels for:

- RXD3/TXD3/RTS3/CTS3 (UART3 U1)

The RS-232 interface enable connection of the module to a COM port on a host-PC. In this instance the RxD line of the transceiver is connected to the TxD line of the COM port; while the TxD line is connected to the RxD line of the COM port. The Ground potential of the phyCORE-i.MX31 circuitry needs to be connected to the applicable Ground pin on the COM port as well.

The phyCORE-i.MX31 does not convert the remaining two available UARTs (UART1, UART2) provided by the i.MX31 MCU to RS-232 levels. The TTL level signals are made available at the phyCORE-connector X1 (*see Table 1*). External RS-232 transceivers must be supplied by the user if additional UART's require RS-232 levels.

The maximum baud rate of UART3 is limited to 460,800 bps when used with the on-board MAX3380 RS-232 transceiver.

8.1.1 UART3 Routing (RN47)

RN47 is used to route the signals of UART3 serial interface through the RS-232 transceiver or around the RS-232 transceiver when not populated. When RN47 is not populated RXD3_TTL,TXD3_TTL,RTS3_TTL and CTS3_TTL are routed through the RS-232 transceiver U21 and come out as x_RXD3_RS232, x_TXD3_RS232, x_RTS3_RS232 and x_CTS3_RS232 at the phyCORE-connector pins X1 pin 22D, X1 pin 23D, X1 pin 25D, X1 pin 26D. If U21 does not populate the module, RN47 is populated to route the TTL level signals to these same pins.

The standard phyCORE-i.MX31 module will have U21 populated, thereby routing the RS-232 level signals to the phyCORE-connector. Be sure the phyCORE-i.MX31 configuration you are working with before interfacing these signals outside of the module as incorrect voltage levels will likely cause damage to on-board and off-board components.

The following configurations are possible:

Table 14: RN47 UART3 Routing[1]

SIGNAL CONFIGURATION	RN47
x_RXD3_RS232, x_TX3_RS232, x_ RTS3_RS232, x_ CTS3_RS232 as RS-232 level signals at X1 pin 22D, X1 pin 23D, X1 pin 47D and X1 46D	**not populated**
x_RXD3_RS232, x_TX3_RS232, x_ RTS3_RS232, x_ CTS3_RS232 as TTL level signals at X1 pin 22D, X1 pin 23D, X1 pin 47D and X1 46D	populated

1 Default settings are in **bold blue** text

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9 USB-OTG Transceiver (U22)

The phyCORE-i.MX31 comes populated with a NXP ISP1504 USB On-The-Go High-Speed transceiver (U22) supporting high speed, full speed, and low speed data rates. The ISP1504 functions as the transceiver between the i.MX31 Host Controller, Device Controller, and On-The-Go Controller. An external USB Standard-A (for USB host), USB Standard-B (for USB device), or USB mini-AB (for USB OTG) connector is all that is needed to interface the phyCORE-i.MX31 USB functionality. The applicable interface signals (D+/D-/VBUS/ID) can be found in the phyCORE-connector pinout *Table 1.*

10 Ethernet Controller (U3)

Connection of the phyCORE-i.MX31 to the world wide web (WWW) or a local area network (LAN) is possible with the on-board SMSC LAN9215/17 10/100 Mbps Ethernet controller with HP Auto-MDIX populating the module at U3. This Ethernet controller features an integrated PHY layer. Thus the external components required to connect the phyCORE-i.MX31 to a LAN are limited to the transformer, the RJ45 socket and a few discrete components. Support for this Ethernet chip is available by a wide range of operating systems, such as Linux and WinCE.

The Ethernet controller is connected to the address/data bus with a 16-bit width and x_GPIO3_1 as interrupt. The interrupt is being used as active low edge triggered.

The /CS signal for the LAN9215/17 Ethernet controller at U3 is connected to the i.MX31 processor's x_/CS1 signal. The Ethernet controller's offset of 0x300 has to be noted when accessing the chip.

The Ethernet controller provides a PME output that can be externally connected to an GPIO input of the controller for signalling an system Wake-up event.

The physical memory area for the Ethernet chip is defined in the following table (*see Table 15*). An offset of 0x300 has to be added to the address of x_/CS1.

Table 15: Memory Area Ethernet Controller

Ethernet	**Start Address**
x_/CS1 + OFFSET	0xA800 00000 + 0x0000 0300 = 0xA800 0300

Connection to an external Ethernet transformer should be done using very short signal lines. The lines TPI+/TPI- and TPO+/TPO- should be routed in pairs. The same applies for the signal lines after the transformer circuit. The carrier board layout should avoid any other signal lines crossing the Ethernet signals. Furthermore, the impedance of the signal lines should be taken into considertaion during the design and layout process.

Caution!
Please note the design specifications provided by SMSC when creating the Ethernet transformer circuitry.

11 JTAG Interface X2

The phyCORE-i.MX31 is equipped with a JTAG interface for downloading program code into the external flash, internal controller RAM or for debugging programs currently executing. The JTAG interface extends out to 2.0 mm pitch pin header rows X2 on the controller side of the module. *Figure 9* and *Figure 10* show the position of the debug interface (JTAG connector X2) on the phyCORE module.

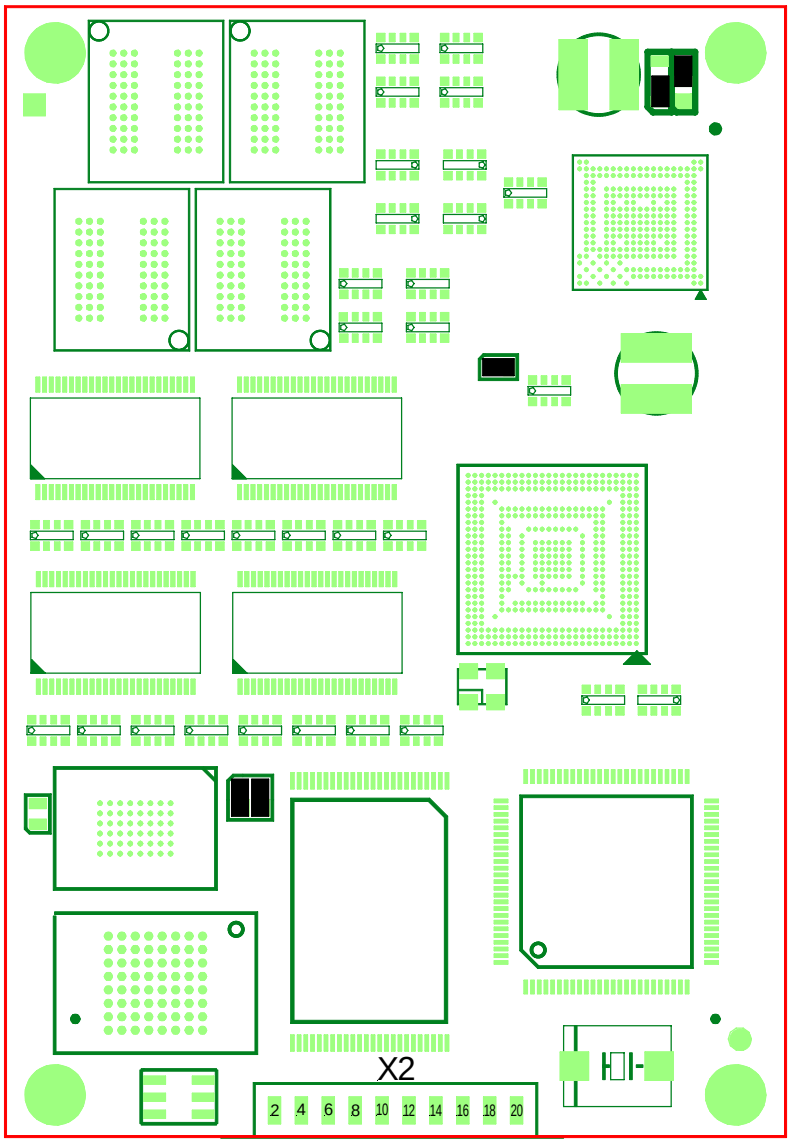

Figure 9: JTAG Interface X2 (Top View)

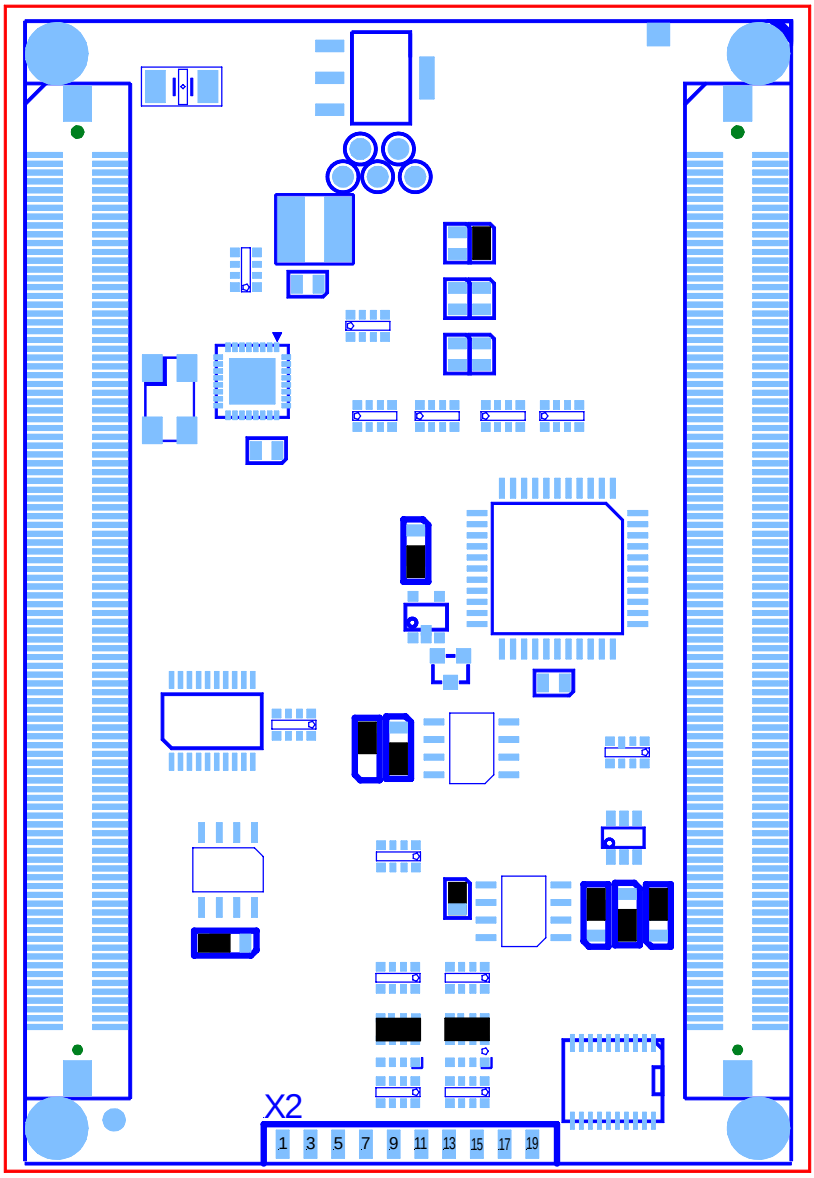

Figure 10: JTAG Interface X2 (Bottom View)

Pin 1 of the JTAG connector X2 is on the connector side of the module. Pin 2 of the JTAG connector is on the controller side of the module.

Note:
The JTAG connector X2 only populates phyCORE-i.MX31 modules with order code PCM-037-D. JTAG connector X2 is not populated on phyCORE modules with order code PCM-037. However, all JTAG signals are also accessible at the phyCORE-connector X1 (Molex connectors). We recommend integration of a standard (2.54 mm pitch) pin header connector in the user target circuitry to allow easy program updates via the JTAG interface. *See Table 16 for details on the JTAG signal pin assignment.*

Table 16: JTAG Connector X2 Signal Assignment

SIGNAL	PIN ROW*		SIGNAL
	A	B	
VCC(NVCC_3_4_6)	2	1	VTref (NVCC_3_4_6 via 100 Ohm)
GND	4	3	x_CPU_/TRST
GND	6	5	x_CPU_TDI
GND	8	7	x_CPU_TMS
GND	10	9	x_CPU_TCK
GND	12	11	x_CPU_RTCK
GND	14	13	x_CPU_TDO
GND	16	15	x_/RESET_MCU
GND	18	17	x_CPU_/DE
GND	20	19	J_DBGACK (10k Ohm pulldown)

*Note:
Row A is on the controller side of the module and row B is connector side of the module

PHYTEC offers a JTAG-Emulator adapter (order code JA-002) for connecting the phyCORE-i.MX31 to a standard emulator. The JTAG-Emulator adapter extends the signals of the module's JTAG connector to a standard ARM connector with 2.54 mm pin pitch. The JA-002 therefore functions as an adapter for connecting the module's non-ARM-compatible JTAG connector X2 to standard Emulator connectors.

12 Technical Specifications

The physical dimensions of the phyCORE-i.MX31 are represented in *Figure 11*. The module's profile is approximately ***8.4 mm*** thick, with a maximum component height of ***4.0 mm*** on the bottom (connector) side of the PCB and approximately ***3.0 mm*** on the top (microcontroller) side. The board itself is approximately ***1.4 mm*** thick.

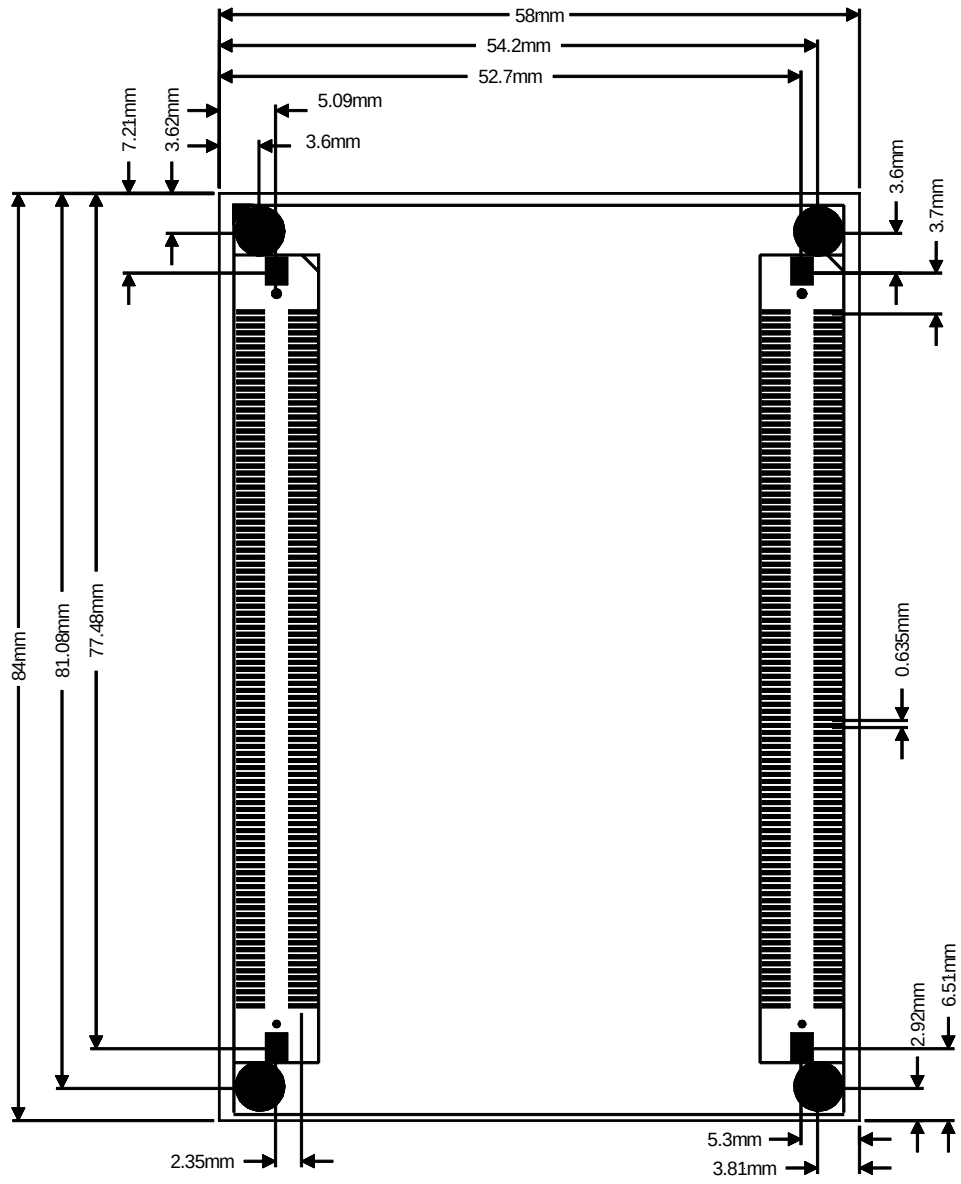

Figure 11: Physical Dimensions

Additional specifications:

• *Dimensions:*	*58 mm x 84 mm*
• *Weight:*	*approximately 35 g with all optional components mounted on the circuit board*
• *Storage temperature:*	*-40°C to +125°C*
• *Operating temperature:*	*0°C to +70°C (commercial)* *0°C to +70°C (industrial)*
• *Humidity:*	*95 % r.F. not condensed*
• *Operating voltage:*	*VIN 3.1 V to 4.6 V*
• *Power consumption:* *VCC 3.3 V / 140 mA typical* *VIN / 280 mA typical*	*Conditions:* ***VCC = 3.3 V, VIN = 4.25 V*** *2 MByte SRAM, 32 MByte Flash, 128 MB LP-DDR-RAM, 64MB NAND-Flash, Ethernet, 532 MHz CPU frequency at 20°C*

These specifications describe the standard configuration of the phyCORE-i.MX31 as of the printing of this manual.

13 Hints for Handling the phyCORE-i.MX31

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

14 The phyCORE i.MX31 on the i.MX Carrier Board

In this chapter you will find the information about using the phyCORE-i.MX31 module with the phyCORE i.MX Carrier Board.
You will get an overview of how the phyCORE-i.MX31 module works with the phyCORE-i.MX Carrier Board, how both boards are connected together over the phyMAPPER and you will also find all settings that have to be done for a speedy and secure start-up of your i.MX31 module.

In this chapter you will only find specialized information of how the phyCORE-i.MX31 module works with the phyCORE-i.MX Carrier Board. *For further information about the Carrier Board please refer to the i.MX Carrier Board Hardware Manual.*

14.1 Concept of the phyCORE-i.MX Development Kits

Phytec decided to use one i.MX Carrier Board for different i.MX modules. Because every i.MX module has different features and therefore a different pinning it is necessary to map the signals of the modules to the right place on the Carrier Board.
For this every i.MX module comes with a phyMAPPER that is mapping the signals of the i.MX module to the i.MX Carrier Board.
An example of the concept is shown in *Figure 12* below. For further information about the concept of the i.MX Carrier Board refer to the i.MX Carrier Board Hardware Manual.

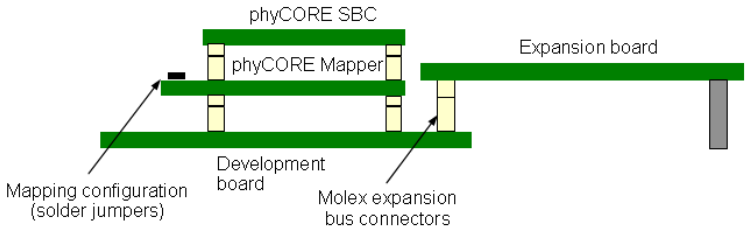

Figure 12: phyCORE-i.MX31 Carrier Board connection using the phyMAP-i.MX31

Fehler! Verweisquelle konnte nicht gefunden werden. below illustrates the modular development platform concept:

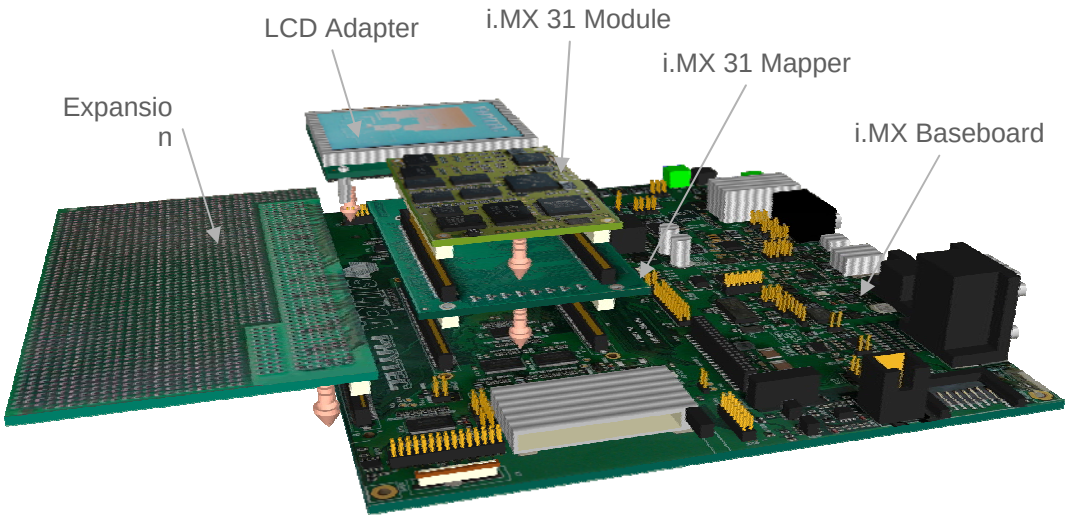

Figure 13: Modular development and Expansion Board Concept with phyCORE-i.MX31

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14.2 phyMAP-i.MX31

The phyMAP-i.MX31 is responsible for mapping the signals from the various phyCORE-i.MX modules to the phyCORE-i.MX Carrier Board. Signal differences at the connectors on the phyCORE-i.MX modules, along with signal differences between the phyCORE-i.MX module connectors and i.MX Carrier Board connector do not allow for direct connection of the phyCORE-i.MX modules into a single, standardized Carrier Board. To allow for the use of a single Carrier Board, despite the signal differences, the phyMAP-i.MX31 board serves as the gateway to properly map signals from the i.MX Carrier Board Molex connectors to the various phyCORE-i.MX module connectors.

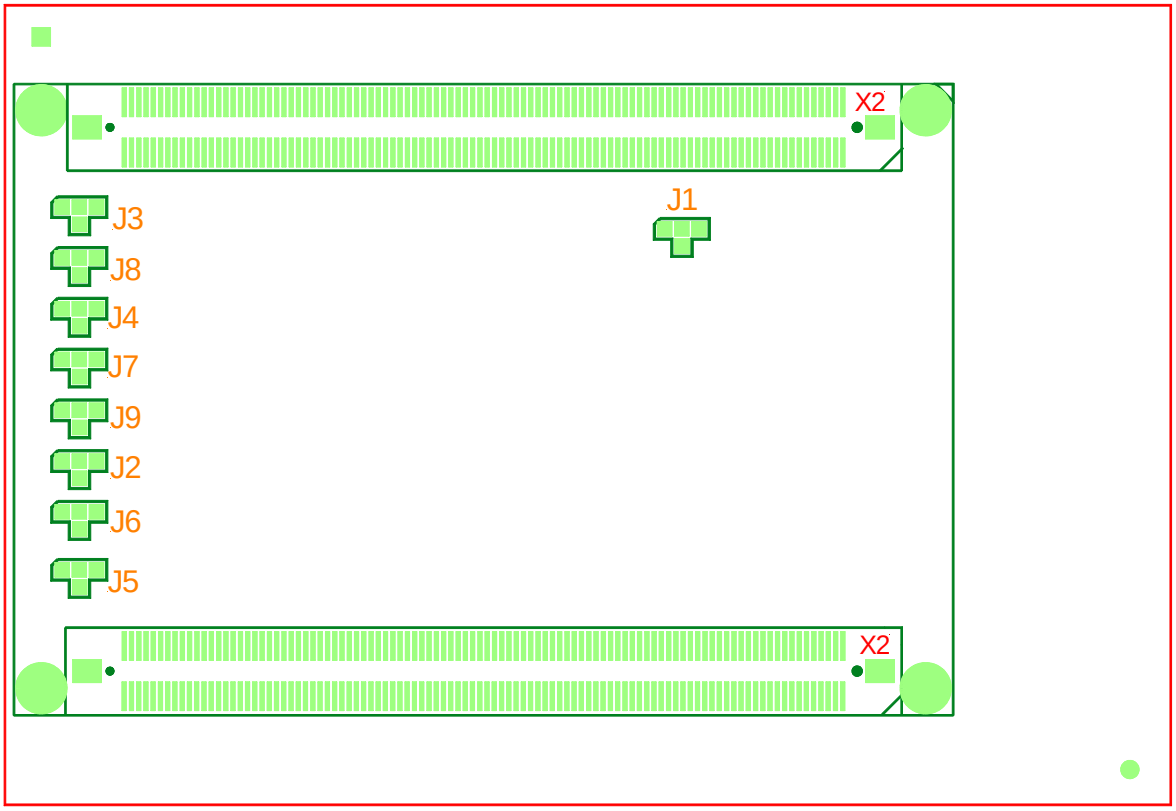

Figure 14: phyMAP-i.MX31 Top View

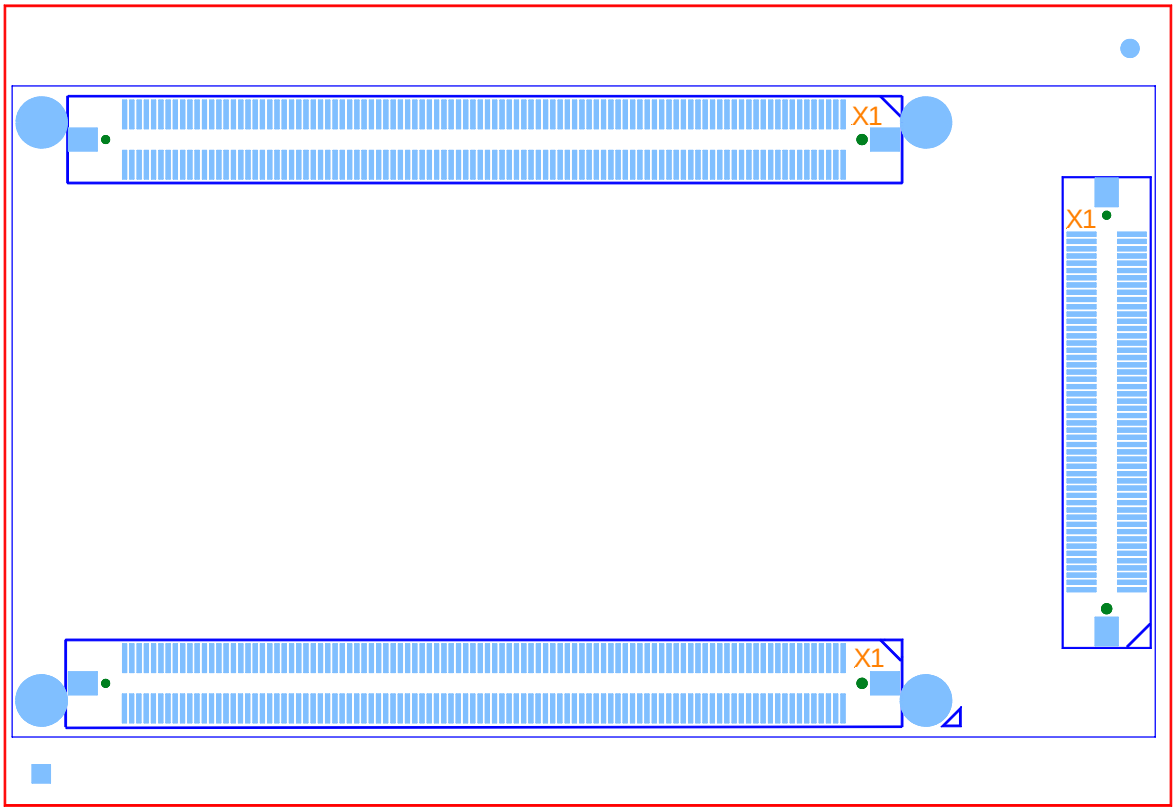

Figure 15: phyMAP-i.MX31 Bottom View

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14.2.1 phyMAP-i.MX31 Jumper Settings

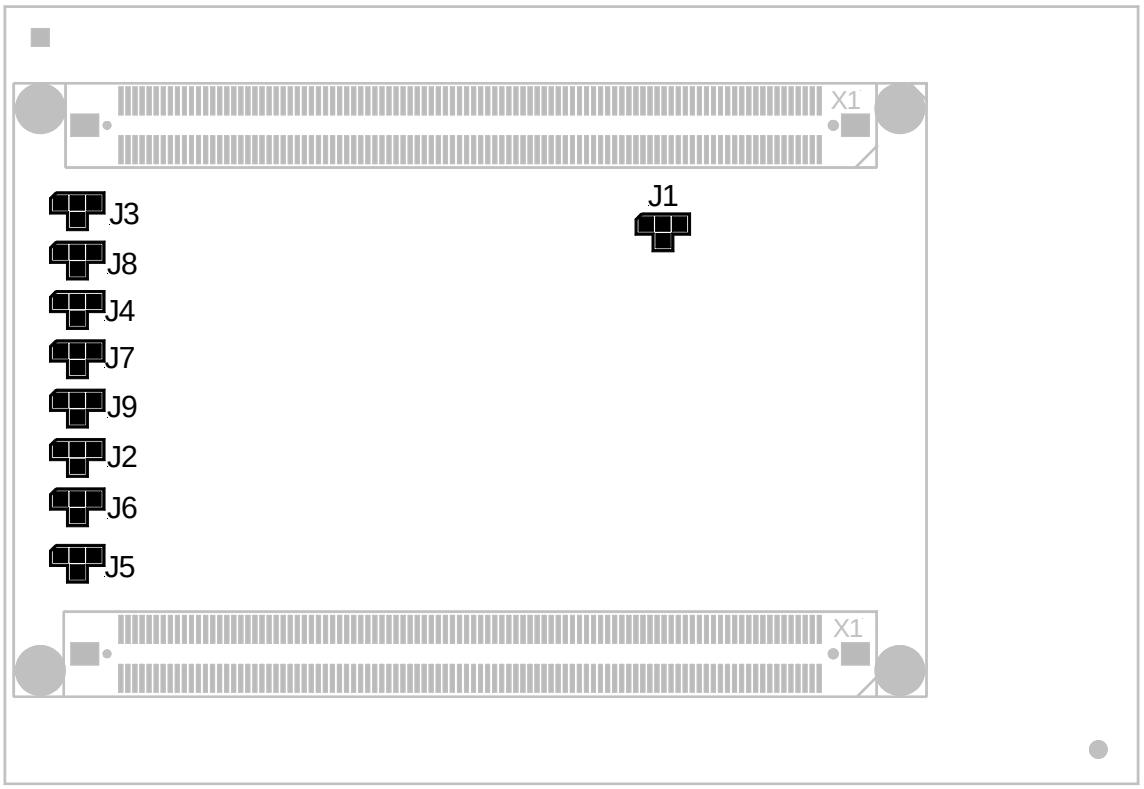

Figure 16: Jumper location on PMA-001

There are 9 solder jumpers (0805) available on the phyMAP-i.MX31 Mapper. They are used to set different functions partially in relation with the i.MX Carrier Board.
An individual description of the jumpers and a list of all jumper settings you will find subsequent.

J1 With this jumper a chip select signal of the i.MX31 can be selected to manage the CAN interface on the phyCORE-i.MX Carrier Board. If J1 is set to 1+2 chip select signal x_/CS4 is selected. When the jumper is set to 3+2 chip select signal x_/CS3 is selected and when set to 4+2 signal x_/CS5 is selected.

J2 The setting of jumper J2 selects the GPIO that should manage an interrupt signal of the CAN controller (U5) of the i.MX Carrier Board. Setting 1+2 selects GPIO x_MCU3_2 to manage the interrupt. When set to 3+2 GPIO x_MCU2_1 manages the interrupt and if J2 is set to 4+2 GPIO x_MCU2_16 is selected.

J3 With this jumper a GPIO of the i.MX31 controller can be selected to provide the x_TRIGGER signal for the camera interface on the i.MC Carrier Board. Setting J3 to 1+2 selects GPIO x_MCU3_2. In position 3+2 GPIO x_MCU2_1 is selected and in position 4+2 GPIO x_/ATA_RESET (MCU3_31) is selected.

J4 With this jumper a GPIO of the i.MX31 controller can be selected to provide the x_SNAPSHOT signal for the camera interface on the i.MX Carrier Board. Setting J4 to 1+2 selects GPIO x_MCU3_3. In position 3+2 GPIO x_MCU2_2 is selected and in position 4+2 GPIO x_/ATA_DMACK (MCU3_30) is selected..

J5 Jumper J5 selects a GPIO of the i.MX31 controller that manages the camera enable signal x_CSI_ENALBE. Setting 1+2 selects GPIO x_MCU2_0 to manage the camera enable. When set to 3+2 GPIO x_MCU2_3 manages the camera enable and if J2 is set to 4+2 GPIO x_CSI_D5 (MCU3_5) is selected.

J6 There is a User LED located on the i.MX Carrier Board. With J6 a GPIO can be selected that is able to drive the LED high or low. If J6 is set to 1+2 GPIO x_MCU2_0 is selected. Setting J6 to 3+2 selects GPIO x_GPO1 and in position 4+2 GPIO x_MCU3_3 is selected.

J7 With J7 a GPIO can be selected that manages the SD card detect signal of the i.MX Carrier Board. Setting J7 to 1+2 selects GPIO x_GPIO1_2. In position 3+2 GPIO x_GPIO1_0 is selected and if J6 is set to 4+2 GPIO x_MCU1_25 is used to manage the SD card detect signal.

J8 With J8 a GPIO can be selected that manages the SD card write protect signal of the i.MX Carrier Board. Setting J8 to 1+2 selects GPIO x_GPIO1_3. In position 3+2 GPIO x_GPIO1_1 is selected and if J6 is set to 4+2 GPIO x_MCU1_26 is used to manage the SD card write protect signal.

J9 This jumper selects a GPIO of the i.MX31 that should manage the x_/IRQ signal of the i.MX Carrier Board. Formerly the x_/IRQ signal was used in a function of the phyCORE-i.MX Carrier Board that is not available any longer. However, the x_/IRQ signal can be used as a GPIO on an Expansion Board.

A detailed list of all jumper settings is available in the following table.

Table 17: Jumper settings of PMA-001[1]

JUMPER	SETTING	DESCRIPTION
J1	1+2	CAN chip select x_/CS_CAN is managed by x_/CS4
	4+2	**CAN chip select x_/CS_CAN is managed by x_/CS5**
	3+2	CAN chip select x_/CS_CAN is managed by x_/CS3
J2	1+2	CAN interrupt x_CAN_INT is managed by GPIO x_MCU3_2
	4+2	**CAN interrupt x_CAN_INT is managed by GPIO x_MCU2_16**
	3+2	CAN interrupt x_CAN_INT is managed by GPIO x_MCU2_1
J3	1+2	Signal x_TRIGGER is managed by GPIO x_MCU3_2
	4+2	**Signal x_TRIGGER is managed by GPIO x_/ATA_RESET (MCU3_31)**
	3+2	Signal x_TRIGGER is managed by GPIO x_MCU2_1
J4	1+2	Signal x_SNAPSHOT is managed by GPIO x_MCU3_3
	4+2	**Signal x_SNAPSHOT is managed by GPIO x_/ATA_DMACK (MCU3_30)**
	3+2	Signal x_SNAPSHOT is managed by GPIO x_MCU2_2
J5	1+2	Camera enable x_CSI_ENABLE is managed by GPIO x_MCU2_0
	4+2	**Camera enable x_CSI_ENABLE is managed by GPIO x_CSI_D5 (MCU3_5)**
	3+2	Camera enable x_CSI_ENABLE is managed by GPIO x_MCU2_3
J6	1+2	User LED x_LED is managed by GPIO x_MCU2_0
	4+2	**User LED x_LED is managed by GPIO x_MCU3_3**
	3+2	User LED x_LED is managed by GPIO x_GPO1
J7	1+2	SD card detect x_SD_D is managed by GPIO x_GPIO1_2
	4+2	**SD card detect x_SD_D is managed by GPIO x_MCU1_25**
	3+2	SD card detect x_SD_D is managed by GPIO x_GPIO1_0
J8	1+2	SD card write protect x_SD_W is managed by GPIO x_GPIO1_3
	4+2	**SD card write protect x_SD_W is managed by GPIO x_MCU1_26**
	3+2	SD card write protect x_SD_W is managed by GPIO x_GPIO1_1
J9	1+2	Signal x_/IRQ is managed by GPIO x_MCU2_1
	4+2	**Signal x_/IRQ is managed by GPIO x_MCU3_1**
	3+2	Signal x_/IRQ is managed by GPIO x_MCU2_2

1 Default settings are in **bold blue** text

14.2.2 phyMAP-i.MX31 Signal Mapping

In the following table you will find all signals of the phyCORE-i.MX31 module (PCM-037) connected through the phyMAP-i.MX31 mapper (PMA-001) to the phyCORE-i.MX Carrier Board (PCM-970).
Take care that there are some signals connected to jumpers on the phyMAP-i.MX31 mapper. With this signals it depends on the individual jumper setting where this signals are connected to. This signals are in **bold** text.

Table 18: PMA-001 Mapping List

Signal Name on PCM-037 Module	Signal Name on PMA-002 Mapper	X2 Pin #	mapped to	X1 Pin #	Signal Name on i.MX Carrier Board
x_1Wire	x_1Wire	91D	<->	58D	x_1Wire
x_/ATA_CS0	x_/ATA_CS0	70A	<->	6F	x_EXP009
x_/ATA_CS1	x_/ATA_CS1	70B	<->	7F	x_EXP010
x_/ATA_DIOR	x_/ATA_DIOR	72B	<->	9E	x_EXP013
x_/ATA_DIOW	x_/ATA_DIOW	73B	<->	10F	x_EXP015
x_/ATA_DMACK	**x_/ATA_DMACK**	75B	<->	15F, 71A	x_EXP023, x_SNAPSHOT
x_/ATA_RESET	**x_/ATA_RESET**	73A	<->	15E, 70A	x_EXP022, x_TRIGGER
x_/BATTDET	x_/BATTDET	43C	<->	25E	x_EXP038
x_/CE1	x_/CE1	66A	<->	57B	x_/CE1
x_/CE2	x_/CE2	66B	<->	58B	x_/CE2
x_/CLK	x_/CLK	31A	<->	4E	x_EXP005
x_/CS0	x_/CS0	24A	<->	1E	x_EXP000
x_/CS1	x_/CS1	25A	<->	1F	x_EXP001
x_/CS3	**x_/CS3**	25B	<->	2F, 58A	x_EXP002, X_/CS_CAN
x_/CS4	**x_/CS4**	26A	<->	3E, 58A	x_EXP003, X_/CS_CAN
x_/CS5	**x_/CS5**	26B	<->	3F, 58A	x_EXP004, X_/CS_CAN
x_/EB0	x_/EB0	27B	<->	55B	x_/EB0
x_/EB1	x_/EB1	28A	<->	56B	x_/EB1
x_/FL_WP	x_/FL_WP	58B	<->	49E	x_EXP077
x_/LED1	x_/LED1	34C	<->	32D	x_ETH_/LED1
x_/LED2	x_/LED2	33C	<->	33D	x_ETH_/LED2
x_/LOWBAT	x_/LOWBAT	50C	<->	31E	x_EXP048
x_/OE	x_/OE	29A	<->	53A	x_/OE
x_/ON1	x_/ON1	30C	<->	55D	x_/ON1
x_/ON2	x_/ON2	31C	<->	56C	x_/ON2
x_/ON3	x_/ON3	37D	<->	56D	x_/ON3
x_/PC_CD1	x_/PC_CD1	60A	<->	66A	x_/PC_CD1
x_/PC_CD2	x_/PC_CD2	60B	<->	66B	x_/PC_CD2

x_PC_nRW	x_/PC_RW	63A	<->	64A	x_/PC_RW
x_/PC_WAIT	x_/PC_WAIT	65B	<->	61B	x_/PC_WAIT
x_/RESET	x_/RESET	5D	<->	5D, 48F	x_/Reset_Btn, x_EXP076
x_/RESET_3V3	x_/RESET_3V3	4D	<->	4D	x_/RESET_3V3
x_/RESET_MCU	x_/RESET_MCU	6D	<->	44C	x_JTAG_SRST
x_/WR	x_/WR	28B	<->	55A	x_/WR
x_A0	x_A0	31B	<->	27B	x_A0
x_A1	x_A1	32B	<->	28A	x_A1
x_A2	x_A2	33A	<->	28B	x_A2
x_A3	x_A3	33B	<->	29A	x_A3
x_A4	x_A4	34A	<->	30A	x_A4
x_A5	x_A5	35A	<->	30B	x_A5
x_A6	x_A6	35B	<->	31A	x_A6
x_A7	x_A7	36A	<->	31B	x_A7
x_A8	x_A8	36B	<->	32B	x_A8
x_A9	x_A9	37B	<->	33A	x_A9
x_A10	x_A10	38A	<->	33B	x_A10
x_A11	x_A11	38B	<->	34A	x_A11
x_A12	x_A12	39A	<->	35A	x_A12
x_A13	x_A13	40A	<->	35B	x_A13
x_A14	x_A14	40B	<->	36A	x_A14
x_A15	x_A15	41A	<->	36B	x_A15
x_A16	x_A16	41B	<->	37B	x_A16
x_A17	x_A17	42B	<->	38A	x_A17
x_A18	x_A18	43A	<->	38B	x_A18
x_A19	x_A19	43B	<->	39A	x_A19
x_A20	x_A20	44A	<->	40A	x_A20
x_A21	x_A21	45A	<->	40B	x_A21
x_A22	x_A22	45B	<->	41A	x_A22
x_A23	x_A23	46A	<->	41B	x_A23
x_A24	x_A24	46B	<->	42B	x_A24
x_A25	x_A25	47B	<->	43A	x_A25
x_ADIN5	x_ADIN5	44C	<->	25F	x_EXP039
x_ADIN6	x_ADIN6	45C	<->	26E	x_EXP040
x_ADIN7	x_ADIN7	46C	<->	26F	x_EXP041
x_ADIN8	x_ADIN8	45D	<->	27F	x_EXP042
x_ADIN9	x_ADIN9	46D	<->	28E	x_EXP043
x_ADIN10	x_ADIN10	47D	<->	28F	x_EXP044
x_ADIN11	x_ADIN11	48D	<->	29E	x_EXP045
x_ADOUT	x_ADOUT	48C	<->	30E	x_EXP046
x_ADTRIG	x_ADTRIG	49C	<->	30F	x_EXP047
x_ATA_BUFFER_EN	x_ATA_BUFFER_EN	75A	<->	10E	x_EXP014

x_ATA_DA0	x_ATA_DA0	76A	<->	11F	x_EXP017
x_ATA_DA1	x_ATA_DA1	76B	<->	12F	x_EXP018
x_ATA_DA2	x_ATA_DA2	77B	<->	13E	x_EXP019
x_ATA_DATA0	x_ATA_DATA0	78A	<->	73A	x_CSI_D0
x_ATA_DATA1	x_ATA_DATA1	78B	<->	74A	x_CSI_D1
x_ATA_DATA2	x_ATA_DATA2	79A	<->	75A	x_CSI_D2
x_ATA_DATA3	x_ATA_DATA3	80A	<->	75B	x_CSI_D3
x_ATA_DATA4	x_ATA_DATA4	80B	<->	76A	x_CSI_D4
x_ATA_DATA5	x_ATA_DATA5	81A	<->	76B	x_CSI_D5
x_ATA_DATA6	x_ATA_DATA6	81B	<->	77B	x_CSI_D6
x_ATA_DATA7	x_ATA_DATA7	82B	<->	78A	x_CSI_D7
x_ATA_DATA8	x_ATA_DATA8	83A	<->	78B	x_CSI_D8
x_ATA_DATA9	x_ATA_DATA9	83B	<->	79A	x_CSI_D9
x_ATA_DATA10	x_ATA_DATA10	84A	<->	69A	x_CSI_MCLK
x_ATA_DATA11	x_ATA_DATA11	85A	<->	72B	x_CSI_VSYNC
x_ATA_DATA12	x_ATA_DATA12	85B	<->	73B	x_CSI_HSYNC
x_ATA_DATA13	x_ATA_DATA13	86A	<->	71B	x_CSI_PCLK
x_ATA_DATA14	x_ATA_DATA14	86B	<->	13F	x_EXP020
x_ATA_DATA15	x_ATA_DATA15	87B	<->	14E	x_EXP021
x_ATA_DMARQ	x_ATA_DMARQ	74A	<->	11E	x_EXP016
x_ATA_INTRQ	x_ATA_INTRQ	71B	<->	8F	x_EXP012
x_ATA_IORDY	x_ATA_IORDY	71A	<->	8E	x_EXP011
x_BATTFET	x_BATTFET	15C	<->	15C	x_BATTFET
x_BATTISNS	x_BATTISNS	14C	<->	14C	x_BATTISNS
x_BFET	x_BFET	16D	<->	17D	x_BFET
x_BOOT_MODE2	x_BOOT_MODE2	98C	<->	53C	x_BOOT_MODE0
x_BOOT_MODE4	x_BOOT_MODE4	98D	<->	53D	x_BOOT_MODE1
x_CAPTURE	x_CAPTURE	100D	<->	50F	x_EXP079
x_Charger_Input	x_Charger_Input	10D, 11D, 12D, 13D	<->	10D, 11D, 12D, 13D	Charger_Input -> x_Charger_Input
x_CHRGCTL	x_CHRGCTL	17D	<->	18D	x_CHRGCTL
x_CHRGISNSN	x_CHRGISNSN	15D	<->	16D	x_CHRGISNSN
x_CHRGISNSP	x_CHRGISNSP	16C	<->	16C	x_CHRGISNSP
x_CHRGLED	x_CHRGLED	19C	<->	19C	x_CHRGLED
x_CHRGMOD0	x_CHRGMOD0	20C	<->	20C	x_CHRGMOD0
x_CLKO	x_CLKO	100B	<->	20F	x_EXP031
x_CLKSS	x_CLKSS	97D	<->	55C	x_CLKSS
x_COMPARE	x_COMPARE	99C	<->	50E	x_EXP078
x_CPU_/DE	x_CPU_/DE	39C	<->	41D	x_CPU_/DE
x_CPU_/TRST	x_CPU_/TRST	41C	<->	43D	x_CPU_/TRST
x_CPU_RTCK	x_CPU_RTCK	40C	<->	42D	x_CPU_RTCK
x_CPU_SJC_MOD	x_CPU_SJC_MOD	43D	<->	43C	x_CPU_SJC_MOD

x_CPU_TCK	x_CPU_TCK	38D	<->	40D	x_CPU_TCK
x_CPU_TDI	x_CPU_TDI	40D	<->	39C	x_CPU_TDI
x_CPU_TDO	x_CPU_TDO	41D	<->	40C	x_CPU_TDO
x_CPU_TMS	x_CPU_TMS	42D	<->	41C	x_CPU_TMS
x_CSI_D4	x_CSI_D4	68B	<->	5F	x_EXP007
x_CSI_D5	**x_CSI_D5**	69A	<->	70B	x_CSI_ENABLE
x_CSPI1_MISO	x_CSPI1_MISO	87D	<->	96B	x_MISO
x_CSPI1_MOSI	x_CSPI1_MOSI	86D	<->	95B	x_MOSI
x_CSPI1_SCLK	x_CSPI1_SCLK	86C	<->	97B	x_SPICLK
x_CSPI1_SPI_RDY	x_CSPI1_SPI_RDY	90C	<->	41F	x_EXP065
x_CSPI1_SS1	x_CSPI1_SS1	88C	<->	98B	x_CE
x_CSPI1_SS2	x_CSPI1_SS2	88D	<->	40F	x_EXP063
x_CSPI1_SS3	x_CSPI1_SS3	89C	<->	41E	x_EXP064
x_CTS3_RS232	x_CTS3_RS232	26D	<->	65C	x_CTS_RS232
x_CTS_DCE1_TTL	x_CTS_DCE1_TTL	74C	<->	61D	x_CTS_DCE1_TTL
x_CTS_DTE2_TTL	x_CTS_DTE2_TTL	79C	<->	37F	x_EXP058
x_D0	x_D0	48A	<->	43B	x_D0
x_D1	x_D1	48B	<->	44A	x_D1
x_D2	x_D2	49A	<->	45A	x_D2
x_D3	x_D3	50A	<->	45B	x_D3
x_D4	x_D4	50B	<->	46A	x_D4
x_D5	x_D5	51A	<->	46B	x_D5
x_D6	x_D6	51B	<->	47B	x_D6
x_D7	x_D7	52B	<->	48A	x_D7
x_D8	x_D8	53A	<->	48B	x_D8
x_D9	x_D9	53B	<->	49A	x_D9
x_D10	x_D10	54A	<->	50A	x_D10
x_D11	x_D11	55A	<->	50B	x_D11
x_D12	x_D12	55B	<->	51A	x_D12
x_D13	x_D13	56A	<->	51B	x_D13
x_D14	x_D14	56B	<->	52B	x_D14
x_D15	x_D15	57B	<->	53B	x_D15
x_DCD_DCE1_TTL	x_DCD_DCE1_TTL	76C	<->	63D	x_DCD_DCE1_TTL
x_DCD_DTE2_TTL	x_DCD_DTE2_TTL	81C	<->	38F	x_EXP060
x_DSR_DCE1_TTL	x_DSR_DCE1_TTL	75D	<->	63C	x_DSR_DCE1_TTL
x_DSR_DTE2_TTL	x_DSR_DTE2_TTL	80C	<->	38E	x_EXP059
x_DTR_DCE1_TTL	x_DTR_DCE1_TTL	76D	<->	64C	x_DTR_DCE1_TTL
x_DTR_DTE2_TTL	x_DTR_DTE2_TTL	81D	<->	36E	x_EXP056
x_ETH_TPI+	x_ETH_TPI+	35D	<->	30C	x_ETH_TPI+
x_ETH_TPI-	x_ETH_TPI-	35C	<->	31C	x_ETH_TPI-
x_ETH_TPO+	x_ETH_TPO+	36D	<->	30D	x_ETH_TPO+
x_ETH_TPO-	x_ETH_TPO-	36C	<->	31D	x_ETH_TPO-
x_ETH_Wkp	x_ETH_Wkp	38C	<->	24E	x_EXP037

x_GPIO1_0	**x_GPIO1_0**	95B	<->	16E, 94A	x_EXP024, x_SD_D
x_GPIO1_1	**x_GPIO1_1**	96B	<->	16F, 95A	x_EXP025, x_SD_W
x_GPIO1_2	**x_GPIO1_2**	97B	<->	17F, 94A	x_EXP026, x_SD_D
x_GPIO1_3	**x_GPIO1_3**	98A	<->	18E, 95A	x_EXP027, x_SD_W
x_GPIO1_4	x_GPIO1_4	98B	<->	18F	x_EXP028
x_GPIO1_5	x_GPIO1_5	99A	<->	19E	x_EXP029
x_GPIO1_6	x_GPIO1_6	100A	<->	20E	x_EXP030
x_GPIO3_1	x_GPIO3_1	95A	<->	68C	x_EXP080
x_GPO1	**x_GPO1**	20D	<->	21F, 58C	x_EXP033, x_LED
x_GPO2	x_GPO2	21D	<->	22F	x_EXP034
x_GPO3	x_GPO3	27D	<->	23E	x_EXP035
x_GPO4	x_GPO4	28D	<->	23F	x_EXP036
x_I2C2_SCL	x_I2C2_SCL	83C	<->	39E	x_EXP061
x_I2C2_SDA	x_I2C2_SDA	84C	<->	40E	x_EXP062
x_I2C3_SCL	x_I2C3_SCL	85D	<->	99A	x_I2C_SCL
x_I2C3_SDA	x_I2C3_SDA	85C	<->	100A	x_I2C_SDA
x_iMX31_FUSE	x_iMX31_FUSE	7D	<->	6D	x_iMX_FUSE
x_IOS16	x_IOS16	68A	<->	65A	x_IOS16
x_KEY_COL0	x_KEY_COL0	88A	<->	48D	x_KEY_COL0
x_KEY_COL1	x_KEY_COL1	89A	<->	49C	x_KEY_COL1
x_KEY_COL2	x_KEY_COL2	90A	<->	50C	x_KEY_COL2
x_KEY_COL3	x_KEY_COL3	90B	<->	50D	x_KEY_COL3
x_KEY_ROW0	x_KEY_ROW0	91A	<->	45C	x_KEY_ROW0
x_KEY_ROW1	x_KEY_ROW1	91B	<->	45D	x_KEY_ROW1
x_KEY_ROW2	x_KEY_ROW2	92B	<->	46C	x_KEY_ROW2
x_KEY_ROW3	x_KEY_ROW3	93A	<->	46D	x_KEY_ROW3
x_KEY_ROW4	x_KEY_ROW4	93B	<->	47D	x_KEY_ROW4
x_KEY_ROW5	x_KEY_ROW5	94A	<->	48C	x_KEY_ROW5
x_LBA	x_LBA	30A	<->	54A	x_LBA
x_LC_BCLK	x_LC_BCLK	10B	<->	10B	x_LC_BCLK
x_LC_CONTRAST	x_LC_CONTRAST	7B	<->	7B	x_LC_CONTRAST
x_LC_D0	x_LC_D0	13A	<->	13A	x_LC_D0
x_LC_D1	x_LC_D1	13B	<->	13B	x_LC_D1
x_LC_D2	x_LC_D2	14A	<->	14A	x_LC_D2
x_LC_D3	x_LC_D3	15A	<->	15A	x_LC_D3
x_LC_D3_CLS	x_LC_D3_CLS	8B	<->	8B	x_LC_D3_CLS
x_LC_D3_REV	x_LC_D3_REV	8A	<->	8A	x_LC_D3_REV
x_LC_D3_SPL	x_LC_D3_SPL	9A	<->	9A	x_LC_D3_SPL
x_LC_D4	x_LC_D4	15B	<->	15B	x_LC_D4

x_LC_D5	x_LC_D5	16A	<->	16A	x_LC_D5
x_LC_D6	x_LC_D6	16B	<->	16B	x_LC_D6
x_LC_D7	x_LC_D7	17B	<->	17B	x_LC_D7
x_LC_D8	x_LC_D8	18A	<->	18A	x_LC_D8
x_LC_D9	x_LC_D9	18B	<->	18B	x_LC_D9
x_LC_D10	x_LC_D10	19A	<->	19A	x_LC_D10
x_LC_D11	x_LC_D11	20A	<->	20A	x_LC_D11
x_LC_D12	x_LC_D12	20B	<->	20B	x_LC_D12
x_LC_D13	x_LC_D13	21A	<->	21A	x_LC_D13
x_LC_D14	x_LC_D14	21B	<->	21B	x_LC_D14
x_LC_D15	x_LC_D15	22B	<->	22B	x_LC_D15
x_LC_D16	x_LC_D16	23B	<->	23B	x_LC_D16
x_LC_D17	x_LC_D17	23A	<->	23A	x_LC_D17
x_LC_DRDY0	x_LC_DRDY0	10A	<->	10A	x_LC_DRDY0
x_LC_FPFRAME	x_LC_FPFRAME	5B	<->	5B	x_LC_FPFRAME
x_LC_FPLINE	x_LC_FPLINE	11A	<->	11A	x_LC_FPLINE
x_LC_PAR_RS	x_LC_PAR_RS	4A	<->	4A	x_LC_PAR_RS
x_LC_READ	x_LC_READ	6A	<->	6A	x_LC_READ
x_LC_SD_D_CLK	x_LC_SD_D_CLK	3A	<->	3A	x_LC_SD_D_CLK
x_LC_SD_D_I	x_LC_SD_D_I	1B	<->	1B	x_LC_SD_D_I
x_LC_SD_D_IO	x_LC_SD_D_IO	2B	<->	2B	x_LC_SD_D_IO
x_LC_SER_RS	x_LC_SER_RS	3B	<->	3B	x_LC_SER_RS
x_LC_VSYNC0	x_LC_VSYNC0	5A	<->	5A	x_LC_VSYNC0
x_LC_WRITE	x_LC_WRITE	6B	<->	6B	x_LC_WRITE
x_LC_x_LCS0	x_LC_x_LCS0	11B	<->	11B	x_LC_x_LCS0
x_LC_x_LCS1	x_LC_x_LCS1	12B	<->	12B	x_LC_x_LCS1
x_LICELL	x_LICELL	18C	<->	18C	x_LICELL
x_MC1LIN	x_MC1LIN	29C	<->	29C	x_MC1LIN
x_MC1RIN	x_MC1RIN	28C	<->	28C	x_MC1RIN
x_MCU1_25	**x_MCU1_25**	90D	<->	46F, 94A	x_EXP073, x_SD_D
x_MCU1_26	**x_MCU1_26**	91C	<->	47F, 95A	x_EXP074, x_SD_W
x_MCU2_0	**x_MCU2_0**	93C	<->	42F, 70B, 58C	x_EXP066, x_CSI_ENABLE, x_LED
x_MCU2_1	**x_MCU2_1**	93D	<->	43E, 59A, 70A	x_EXP067, x_CAN_INT, x_TRIGGER
x_MCU2_2	**x_MCU2_2**	94C	<->	43F, 71A, 96A	x_EXP068, x_SNAPSHOT, x_/IRQ
x_MCU2_3	**x_MCU2_3**	95C	<->	44E, 70B	x_EXP069, x_CSI_ENABLE
x_MCU2_16	**x_MCU2_16**	82D	<->	59A	x_CAN_INT

x_MCU3_2	**x_MCU3_2**	95D	<->	45F, 59A, 70A	x_EXP071, x_CAN_INT, x_TRIGGER
x_MCU3_3	**x_MCU3_3**	96C	<->	46E, 71A, 58C	x_EXP072, x_SNAPSHOT, x_LED
x_PCOE	x_PCOE	61B	<->	62B	x_PCOE
x_PC_BVD1	x_PC_BVD1	58A	<->	60A	x_PC_BVD1
x_PC_BVD2	x_PC_BVD2	59A	<->	61A	x_PC_BVD2
x_PC_PWRON	x_PC_PWRON	61A	<->	63A	x_PC_PWRON
x_PC_READY	x_PC_READY	62B	<->	63B	x_PC_READY
x_PC_RST	x_PC_RST	63B	<->	65B	x_PC_RST
x_PC_VS1	x_PC_VS1	64A	<->	67B	x_PC_VS1
x_PC_VS2	x_PC_VS2	65A	<->	68B	x_PC_VS2
x_Power_BATT	x_Power_BATT	13C	<->	15D	x_Power_BATT
x_PWRRDY	x_PWRRDY	18D	<->	6E	x_EXP008
x_RI_DCE1_TTL	x_RI_DCE1_TTL	75C	<->	62D	x_RI_DCE1_TTL
x_RI_DTE2_TTL	x_RI_DTE2_TTL	80D	<->	35F	x_EXP055
x_RTS3_RS232	x_RTS3_RS232	25D	<->	66C	x_RTS_RS232
x_RTS_DCE1_TTL	x_RTS_DCE1_TTL	73C	<->	60D	x_RTS_DCE1_TTL
x_RTS_DTE2_TTL	x_RTS_DTE2_TTL	78D	<->	35E	x_EXP054
x_RXD3_RS232	x_RXD3_RS232	22D	<->	65D	x_RXD_RS232
x_RXD_DCE1_TTL	x_RXD_DCE1_TTL	73D	<->	61C	x_RXD_DCE1_TTL
x_RXD_DTE2_TTL	x_RXD_DTE2_TTL	77D	<->	34E	x_EXP053
x_RXINL	x_RXINL	25C	<->	25C	x_RXINL
x_RXINR	x_RXINR	26C	<->	26C	x_RXINR
x_RXOUTL_LSPP	x_RXOUTL	23C	<->	23C	x_RXOUTL
x_RXOUTR_LSPM	x_RXOUTR	24C	<->	24C	x_RXOUTR
x_SD1_CLK	x_SD1_CLK	70D	<->	91A	x_SD1_CLK
x_SD1_CMD	x_SD1_CMD	68D	<->	90B	x_SD1_CMD
x_SD1_DATA0	x_SD1_DATA0	68C	<->	91B	x_SD1_DATA0
x_SD1_DATA1	x_SD1_DATA1	69C	<->	92B	x_SD1_DATA1
x_SD1_DATA2	x_SD1_DATA2	70C	<->	93A	x_SD1_DATA2
x_SD1_DATA3	x_SD1_DATA3	71C	<->	93B	x_SD1_DATA3
x_Tout	x_Tout	8D	<->	48E	x_EXP075
x_TSX1	x_TSX1	30D	<->	25D	x_TSX1
x_TSX2	x_TSX2	31D	<->	26D	x_TSX2
x_TSY1	x_TSY1	32D	<->	27D	x_TSY1
x_TSY2	x_TSY2	33D	<->	28D	x_TSY2
x_TXD3_RS232	x_TXD3_RS232	23D	<->	66D	x_TXD_RS232
x_TXD_DCE1_TTL	x_TXD_DCE1_TTL	72D	<->	60C	x_TXD_DCE1_TTL
x_TXD_DTE2_TTL	x_TXD_DTE2_TTL	78C	<->	36F	x_EXP057
x_UDM	x_UDM	54C	<->	34C	x_UDM
x_UDP	x_UDP	55C	<->	35C	x_UDP

x_UID	x_UID	56C	<->	36C	x_UID
x_USBHOST2_CLK	x_USBHOST2_CLK	60C	<->	83A	x_USBHOST2_CLK
x_USBHOST2_DA0	x_USBHOST2_DA0	62D	<->	85A	x_USBHOST2_DA0
x_USBHOST2_DA1	x_USBHOST2_DA1	63D	<->	85B	x_USBHOST2_DA1
x_USBHOST2_DA2	x_USBHOST2_DA2	63C	<->	86A	x_USBHOST2_DA2
x_USBHOST2_DA3	x_USBHOST2_DA3	65D	<->	86B	x_USBHOST2_DA3
x_USBHOST2_DA4	x_USBHOST2_DA4	64C	<->	87B	x_USBHOST2_DA4
x_USBHOST2_DA5	x_USBHOST2_DA5	66D	<->	88A	x_USBHOST2_DA5
x_USBHOST2_DA6	x_USBHOST2_DA6	65C	<->	88B	x_USBHOST2_DA6
x_USBHOST2_DA7	x_USBHOST2_DA7	67D	<->	89A	x_USBHOST2_DA7
x_USBHOST2_DIR	x_USBHOST2_DIR	61C	<->	84A	x_USBHOST2_DIR
x_USBHOST2_NXT	x_USBHOST2_NXT	61D	<->	83B	x_USBHOST2_NXT
x_USBHOST2_STP	x_USBHOST2_STP	60D	<->	82B	x_USBHOST2_STP
x_USBOTG_DA0	x_USBOTG_DA0	50D	<->	31F	x_EXP049
x_USBOTG_DA3	x_USBOTG_DA3	51D	<->	32F	x_EXP050
x_USBOTG_DA4	x_USBOTG_DA4	52D	<->	33E	x_EXP051
x_USBOTG_DA5	x_USBOTG_DA5	53D	<->	33F	x_EXP052
x_USB_BYP	x_USB_BYP	58D	<->	80A	x_USB_BYP
x_USB_HS_/PSW	x_USB_HS_/PSW	56D	<->	35D	x_USB_HS_/PSW
x_USB_HS_FAULT	x_USB_HS_FAULT	57D	<->	36D	x_USB_HS_FAULT
x_USB_OC	x_USB_OC	58C	<->	81A	x_USB_OC
x_USB_PWR	x_USB_PWR	59C	<->	80B	x_USB_PWR
x_USEROFF	x_USEROFF	51C	<->	21E	x_EXP032
x_VBAT	x_VBAT	6C	<->	6C	x_VBAT
x_VBUS	x_VBUS	53C	<->	33C	x_VBUS
x_WAIT	x_WAIT	30B	<->	5E	x_EXP006

Note:
Signals in **bold** text are connected to jumpers. The mapping of this signals could differ from the mapping list. Please check the positions of the affected jumpers to find out how the signals are mapped.

14.2.3 phyMAP-i.MX31 Mapper Physical Dimensions

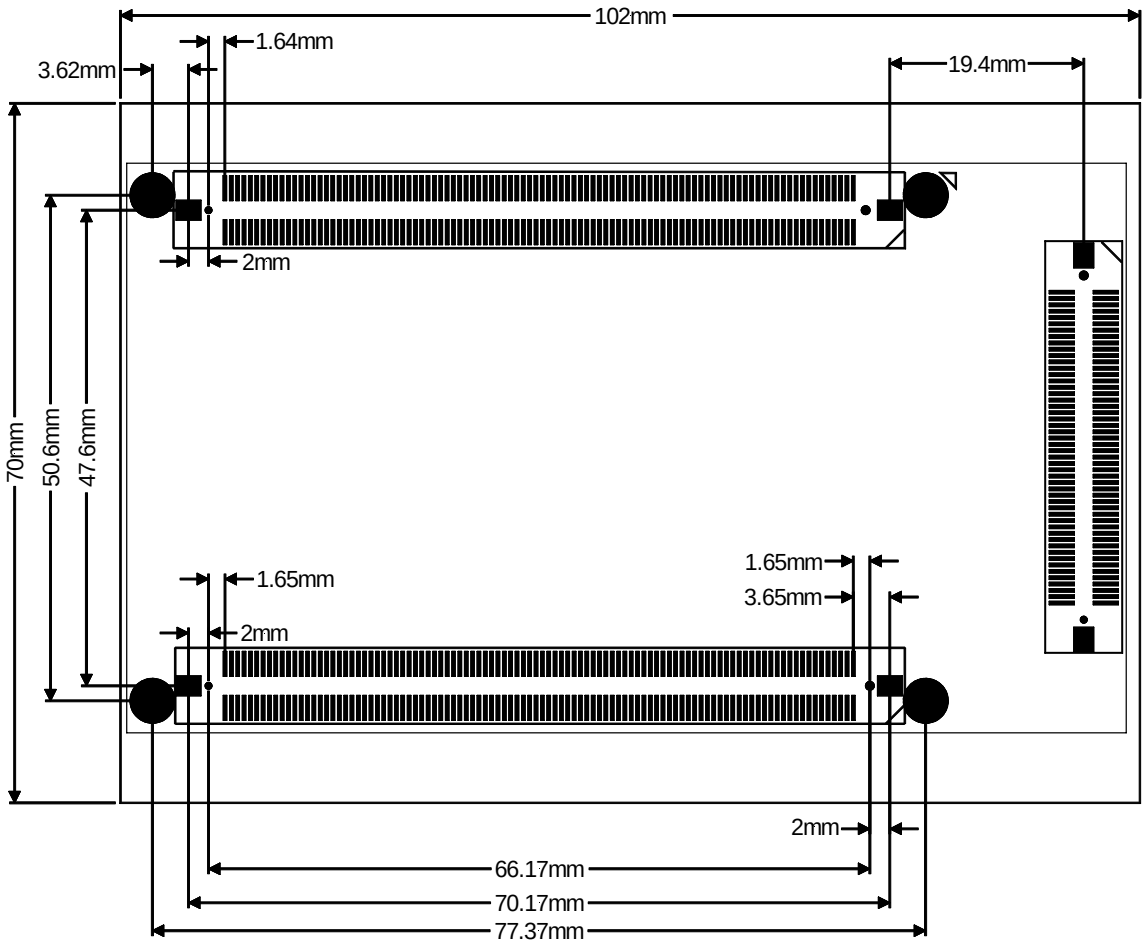

Figure 17: Physical Dimensions of phyMAP-i.MX31 Mapper

14.3 Cooperation of phyCORE-i.MX31 and phyCORE-i.MX Carrier Board

In this chapter you will find specific information and settings to adapt the i.MX Carrier Board to the i.MX31 module.
For information about the general functionality of the various interfaces of the phyCORE-i.MX Carrier Board, please refer to the phyCORE-i.MX Carrier Board Hardware Manual.

14.3.1 Power Supply

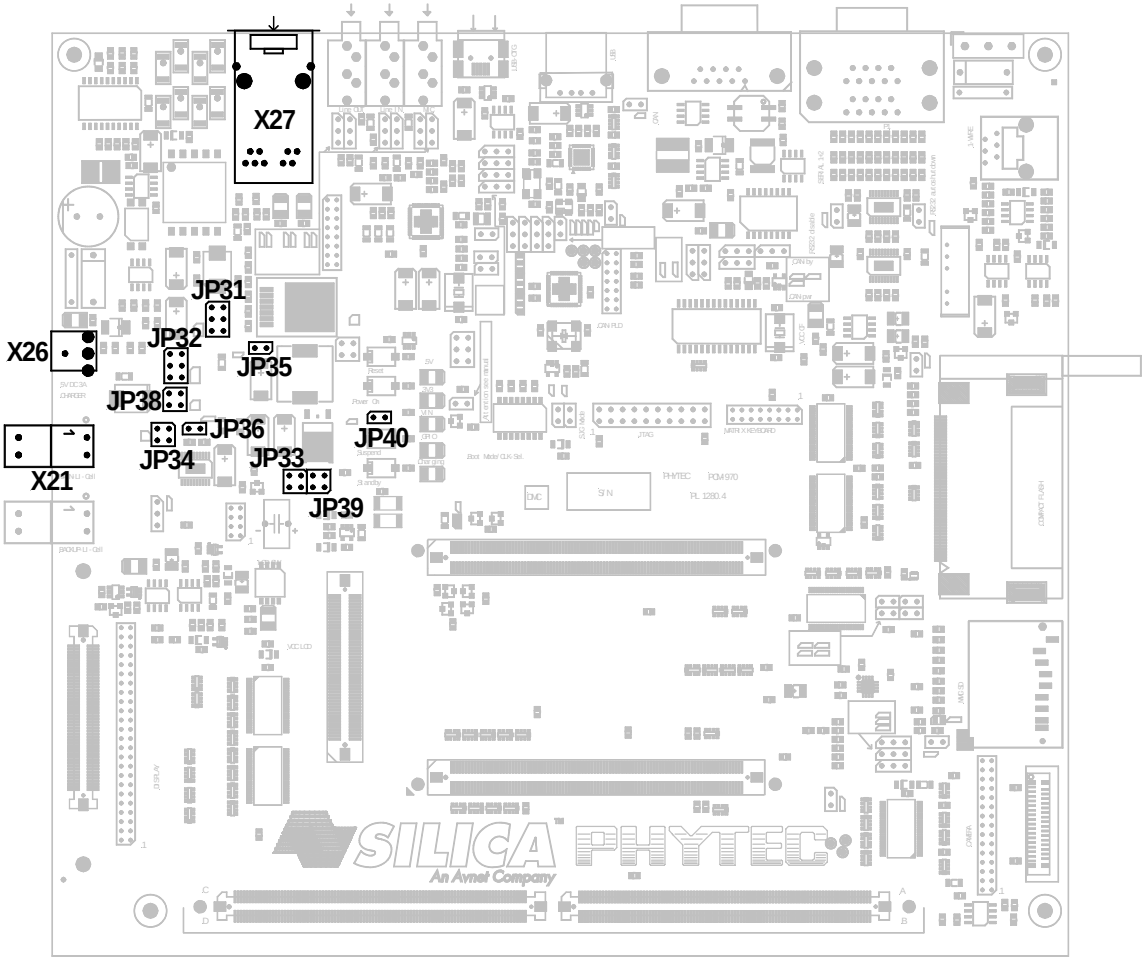

Figure 18: pyhCORE-i.MX Carrier Board and phyCORE-i.MX31 Power Supply

Subsequent you will find the different jumper settings for the three power supply modes described in the phyCORE-i.MX Carrier Board Hardware Manual.

Note:
With the phyCORE-i.MX31 module the Power Management IC MC13783 is provided so battery charging is also provided with the i.MX31 module.

14.3.1.1 Power Supply via Power Plug

Table 19 below shows the jumper settings to supply the phyCORE-i.MX31 module and the phyCORE-i.MX Carrier Board with a wall charger at X26 of the i.MX Carrier Board.

Table 19: Jumper settings for i.MX31 power supply via power plug[1]

JUMPER	SETTING	DESCRIPTION
JP31	1+3,2+4 **3+5,4+6**	Power source is Power Over Ethernet (POE) **Power source is 5V adapter**
JP32	1+3,2+4 **3+5,4+6**	No power switching, direct supply of VCC_3V3 **Separate supply path**
JP33	1+2,3+4 **open,open**	No power switching, direct supply from VCC_3V3 **Separate supply path**
JP34	1+2,3+4 **open,open**	No power switching, direct supply from VCC_3V3 **Separate supply path**
JP35	**open** closed	**VCC_5V Power Supply is enabled** VCC_5V Power Supply is disabled
JP36	open **closed**	VCC_3V3 Power Supply is disabled **VCC_3V3 Power Supply is enabled**
JP38	**1+2,3+4** open,open	**Power switching, supply from 5V adapter or POE** No power switching, direct supply from VCC_3V3
JP39	**1+2,3+4** open,open	**Power switching active, Battery charge path closed** No power switching, direct supply from VCC_3V3
JP40	open **closed**	No power switching active, minimum circuit **Power switching active**

1 *Settings for the phyCORE-i.MX31 power supply via power plug are in **bold blue***

14.3.1.2 Power Supply via Power over Ethernet

Table 20 below shows the jumper settings to supply the phyCORE-i.MX31 module and the phyCORE-i.MX Carrier Board with Power over Ethernet at X27.

Table 20: Jumper settings for i.MX31 power supply via POE[1]

JUMPER	SETTING	DESCRIPTION
JP31	**1+3,2+4** 3+5,4+6	**Power source is Power Over Ethernet (POE)** Power source is 5V adapter
JP32	1+3,2+4 **3+5,4+6**	No power switching, direct supply of VCC_3V3 **Separate supply path**
JP33	1+2,3+4 **open,open**	No power switching, direct supply from VCC_3V3 **Separate supply path**
JP34	1+2,3+4 **open,open**	No power switching, direct supply from VCC_3V3 **Separate supply path**
JP35	**open** closed	**VCC_5V Power Supply is enabled** VCC_5V Power Supply is disabled
JP36	open **closed**	VCC_3V3 Power Supply is disabled **VCC_3V3 Power Supply is enabled**
JP38	**1+2,3+4** open,open	**Power switching, supply from 5V adapter or POE** No power switching, direct supply from VCC_3V3
JP39	**1+2,3+4** open,open	**Power switching active, Battery charge path closed** No power switching, direct supply from VCC_3V3
JP40	open **closed**	No power switching active, minimum circuit **Power switching active**

1 Settings for the phyCORE-i.MX31 power supply via Power over Ethernet are in **bold blue**

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14.3.1.3 Power Supply via Battery

Table 21 below shows the jumper settings to supply the phyCORE-i.MX31 module and the phyCORE-i.MX Carrier Board with a battery at X21 of the i.MX Carrier Board.

Table 21: Jumper settings for i.MX31 power supply via battery[1]

JUMPER	SETTING	DESCRIPTION
JP31	1+3,2+4	Power source for battery charging is Power Over Ethernet (POE)
	3+5,4+6	**Power source for battery charging is 5 V adapter**
JP32	1+3,2+4	No power switching, direct supply of VCC_3V3
	3+5,4+6	**Separate supply path**
JP33	1+2,3+4	No power switching, direct supply from VCC_3V3
	open,open	**Separate supply path**
JP34	1+2,3+4	No power switching, direct supply from VCC_3V3
	open,open	**Separate supply path**
JP35	**open**	**VCC_5V Power Supply is enabled**
	closed	VCC_5V Power Supply is disabled
JP36	open	VCC_3V3 Power Supply is disabled
	closed	**VCC_3V3 Power Supply is enabled**
JP38	**1+2,3+4**	**Power switching, supply from 5 V adapter or POE**
	open,open	No power switching, direct supply from VCC_3V3
JP39	**1+2,3+4**	**Power switching active, Battery charge path closed**
	open,open	No power switching, direct supply from VCC_3V3
JP40	open	No power switching active, minimum circuit
	closed	**Power switching active**

1 Settings for the phyCORE-i.MX31 power supply via battery are in **bold blue**

14.3.2 CAN Interface

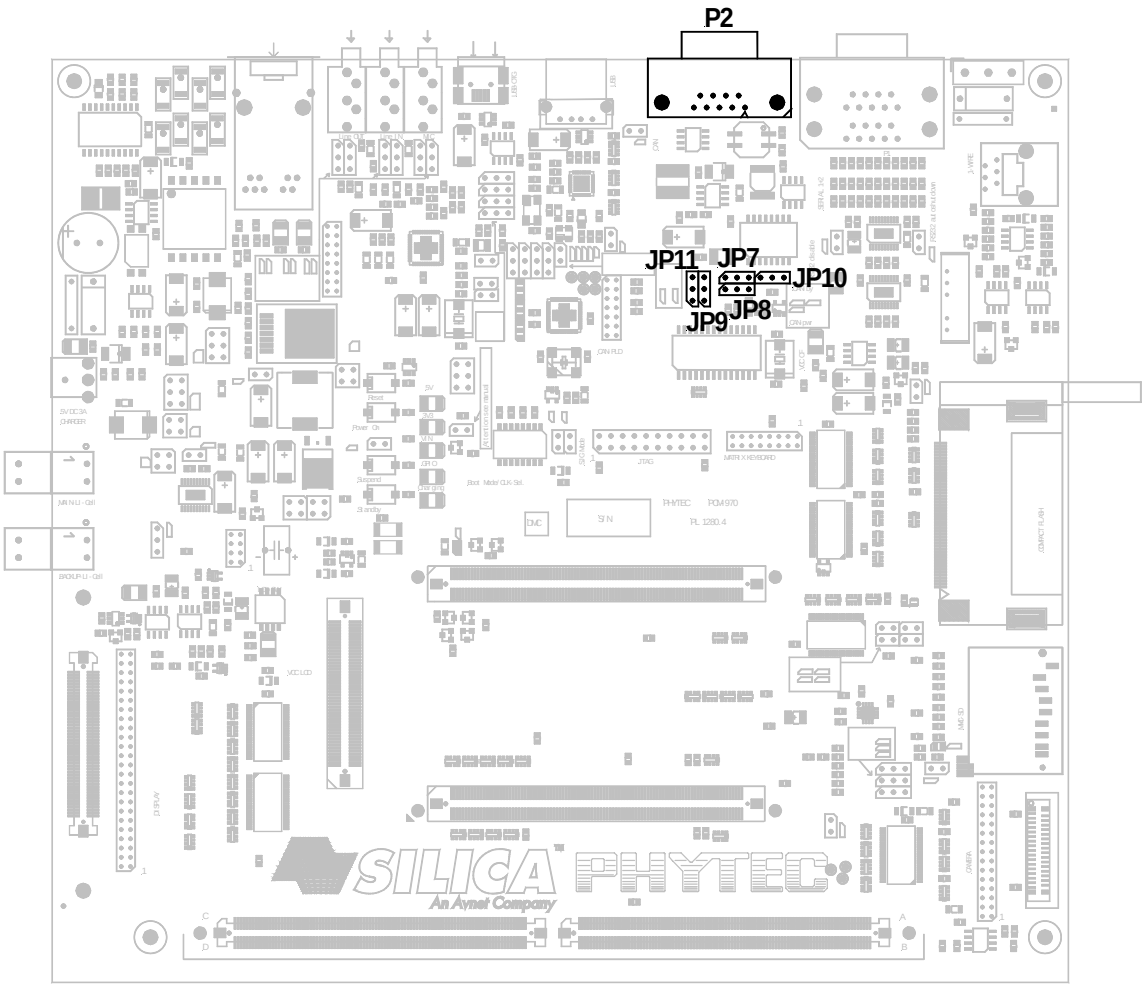

Figure 19: phyCORE-i.MX Carrier Board CAN Interface

The phyCORE-i.MX31 does not provide a CAN controller. For CAN support there is a CAN controller available on the Carrier Board that is connected to the data-/address bus of the phyCORE-i.MX31.
Please refer to Table 22 below for the jumper settings to use the CAN interface with the i.MX31 module.

Table 22: CAN interface jumper settings[1]

JUMPER	SETTING	DESCRIPTION
JP7	**1 + 2** 2 + 3	**CANTxD signal is routed to the CAN transceiver** x_CAN_TxD signal is routed to the CAN transceiver
JP8	1 + 2 **2 + 3**	Digital Isolator is supplied by VCC_CAN **Digital Isolator supply is VCC_5V**
JP9	**1 + 2** 2 + 3	**CANV- is connected to GND of i.MX Carrier Board** CANV- is not connected to GND of i.MX Carrier Board
JP10	**1 + 2** 2 + 3	**CANRxd signal is routed to the CAN transceiver** x_CAN_RxD signal is routed to the CAN transceiver
JP11	**1 + 2** 2 + 3	**CANV+ is connected to VCC_5V of i.MX Carrier Board** CANV+ is connected to CAN_OUT (external supply)

1 Default settings for the phyCORE-i.MX31 CAN interface on the i.MX Carrier Board are in **bold blue**

14.3.3 Push Buttons and LEDs

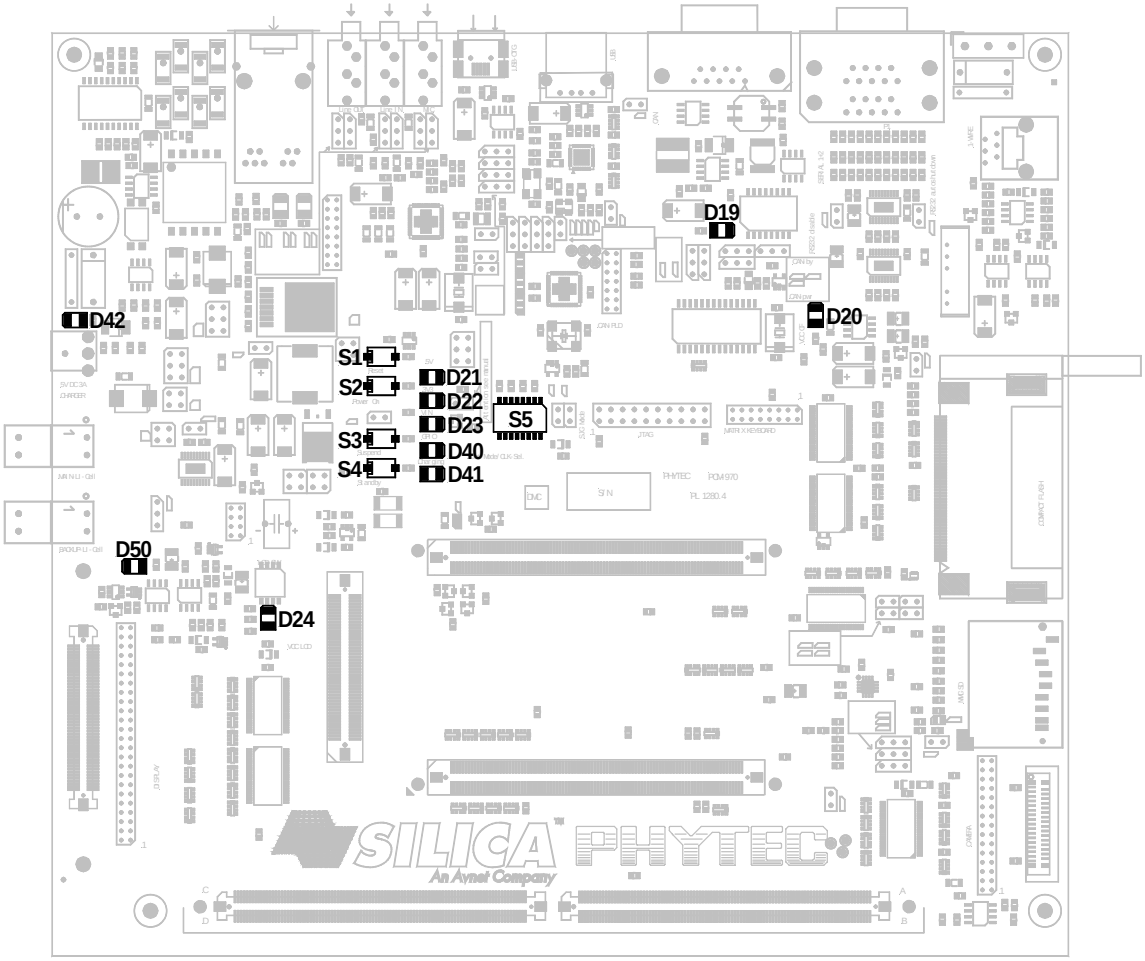

Figure 20: phyCORE-i.MX Carrier Board Buttons and LEDs

There are 3 GPIO signals of the i.MX31 module that can used to drive the User-LED D40 high or low. These GPIOs are x_MCU2_0, x_GPO1 and x_MCU3_3. Which of these GPIO signals should be used can be selected by jumper J6 of the phyMAP-i.MX31 Mapper. *For further details about the setting of this jumper please refer to chapter 3.*

14.3.3.1 Boot-Mode and Clock Selection

There is a possibility to choose whether the 32kHz or the 26MHz clock of the phyCORE-i.MX31 module is used as clock source for the i.MX31. Which of the clock source should be used can be selected with the dip switch S5 on the i.MX Carrier Board. (*see Table 23)*

Note:
There is already a standard configuration set on the phyCORE-i.MX31. In this configuration the 26MHz clock source is used. To use the standard configuration both switches have to be in OFF position.

Table 23: Clock selection

STATE OF SW NUMBER 1	STATE OF SW NUMBER 2	STATE OF X_CLKSS
ON	OFF	0 => CKIL (32kHz) is used as clock source
OFF	ON	1 => CKIH (26MHz) is used as clock source

The i.MX31 controller is able to boot from different devices as described *in chapter* ***Fehler! Verweisquelle konnte nicht gefunden werden.****, "****Fehler! Verweisquelle konnte nicht gefunden werden.****".* To have a choice from which device the controller should boot the boot signals BOOT_MODE_2 and BOOT_MODE_4 are connected to the dip-switch S5 on the i.MX Carrier Board.

With S5 on the i.MX Carrier Board it is possible to select the status of BOOT_MODE_2 and BOOT_MODE_4. *For detailed information see Table 24 and Table 25 below.*

Note:
A standard Boot Configuration is already set on the i.MX31 module. Here you can change the Boot Mode to an alternatively mode. For standard Boot Configuration all dip switches have to be in OFF position.

Table 24: x_BOOT_MODE0 Selection

STATE OF SW NUMBER 3	STATE OF SW NUMBER 4	STATE OF X_BOOT_MODE2
ON	OFF	0
OFF	ON	1

Table 25: x_BOOT_MODE1 Selection

STATE OF SW NUMBER 5	STATE OF SW NUMBER 6	STATE OF X_BOOT_MODE4
ON	OFF	0
OFF	ON	1

Switches 7 and 8 of dip switch S5 are not used with the phyCORE-i.MX31. This switches may be used with other i.MX modules on the phyCORE-i.MX Carrier Board.

Table 26: x_switch (not used)

STATE OF SW NUMBER 7	STATE OF SW NUMBER 8	STATE OF X_SWITCH
ON	OFF	0
OFF	ON	1

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14.3.4 Compact Flash Card

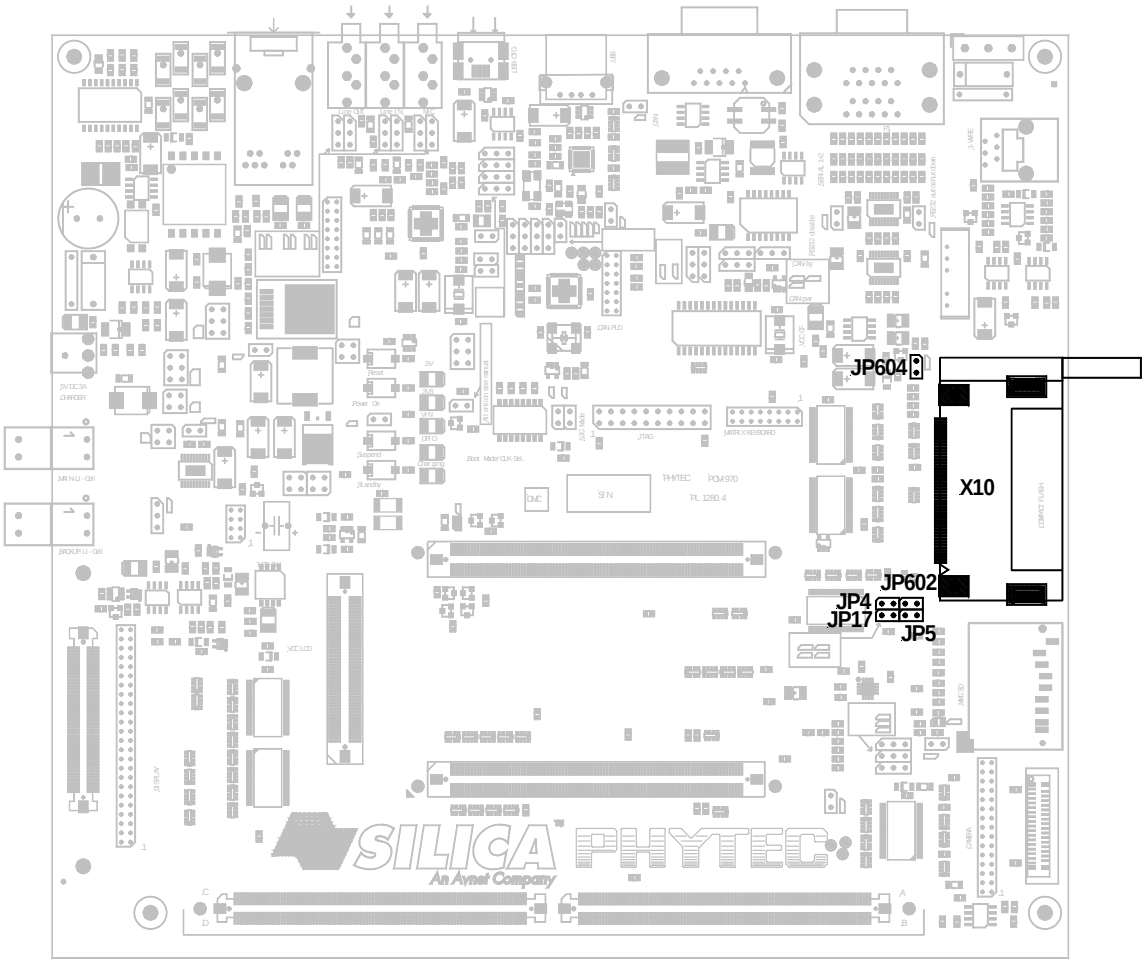

Figure 21: Compact Flash Card Interface

The GPIO signal of the i.MX31 module connected to signal x_EXP007 of the i.MX Carrier Board is x_CSI_D4 (MCU3_4). With GPIO x_CSI_D4 (MCU3_4) the power supply of the CF interface can be managed.

Table 27: CF interface jumper settings[1]

JUMPER	SETTING	DESCRIPTION
JP4	**closed** open	**/PC_RW signal can manage the data direction of U13** Data direction of U13 is from controller to CF
JP5	**closed** open	**Compact Flash is Master** Compact Flash is Slave
JP17	**open** closed	**Output 2 of U15 is active** Output 2 of U15 is disabled
JP602	closed **open**	PC_RW non-inverted **PC_RW inverted**
JP604	**closed** open	**Power supply of CF is forced active** Power supply of CF can be managed by GPIO signal x_EXP007

1 Default settings for the phyCORE-i.MX31 CF interface on the i.MX Carrier Board are in **bold blue**

14.3.5 Security Digital Card/ MultiMedia Card

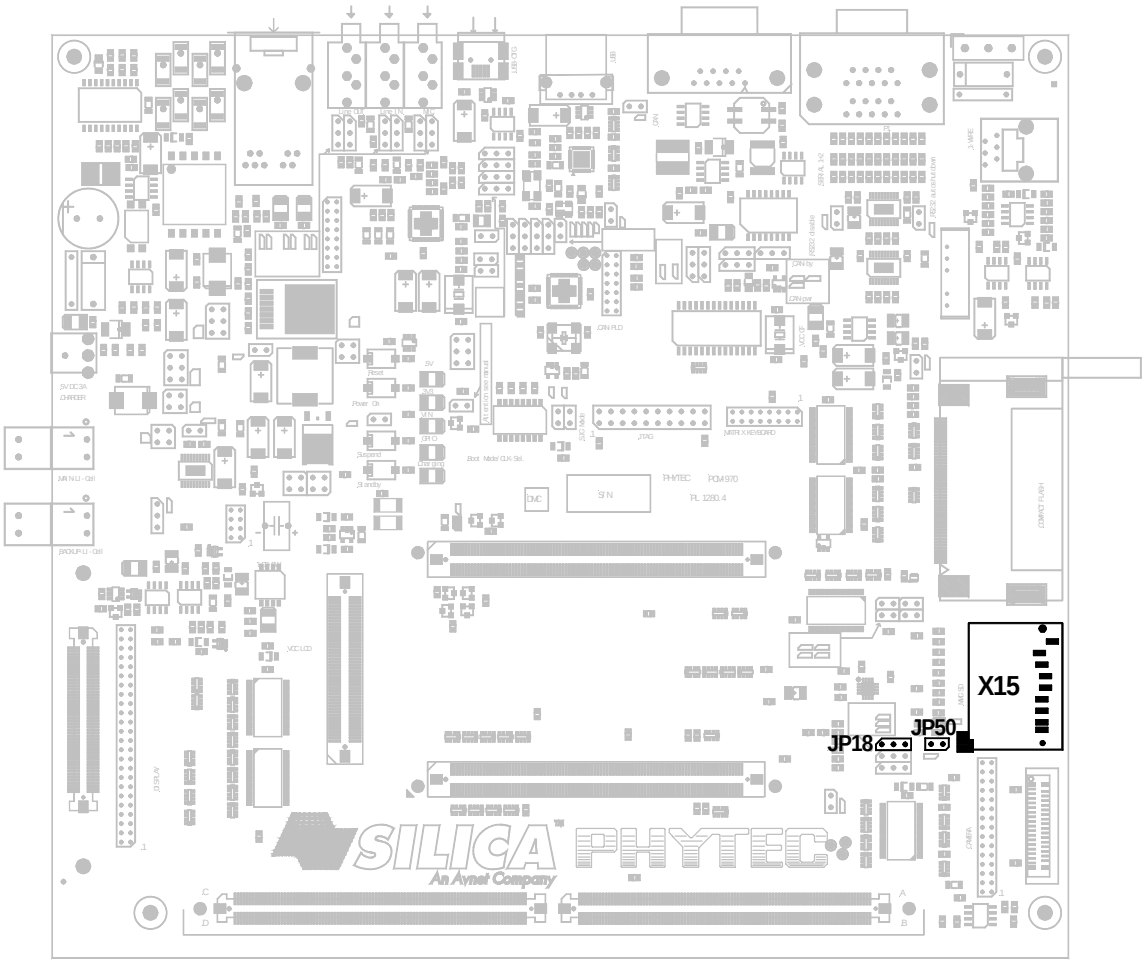

Figure 22: SD Card Interface

The MMC_DETECT or also x_SD_D signal of the i.MX Carrier Board is connected to one of three GPIO signals of the i.MX31 controller. These three GPIOs are GPIO1_0, x_GPIO1_2 and x_MCU1_25. Which of these GPIOs is used can be set by jumper J7 on the phyMAP-i.MX31 mapper. In standard configuration GPIO signal x_MCU1_25 is used.

The MMC_WP or also x_SD_W signal of the i.MX Carrier Board is also connected to one of three GPIO signals of the i.MX31 controller. These three GPIOs are GPIO1_1, x_GPIO1_3 and x_MCU1_26. Which of these GPIOs is used can be set by jumper J8 on the phyMAP-i.MX31 mapper. In standard configuration GPIO signal x_MCU1_26 is used.

Table 28: SD/MMC Interface Jumper Settings for i.MX31 Module[1]

JUMPER	SETTING	DESCRIPTION
JP50	**closed** open	**MMC_WP signal of SD/MMC Interface is connected to GPIO** MMC_WP signal of SD/MMC Interface is not connected to GPIO
JP18	**2 + 3** 1 + 2	**Level shifter U25 is enabled** Level shifter U25 is disabled

1 Default settings for the phyCORE-i.MX31 SD/MMC interface are in **bold blue**

14.3.6 Audio and Touchscreen

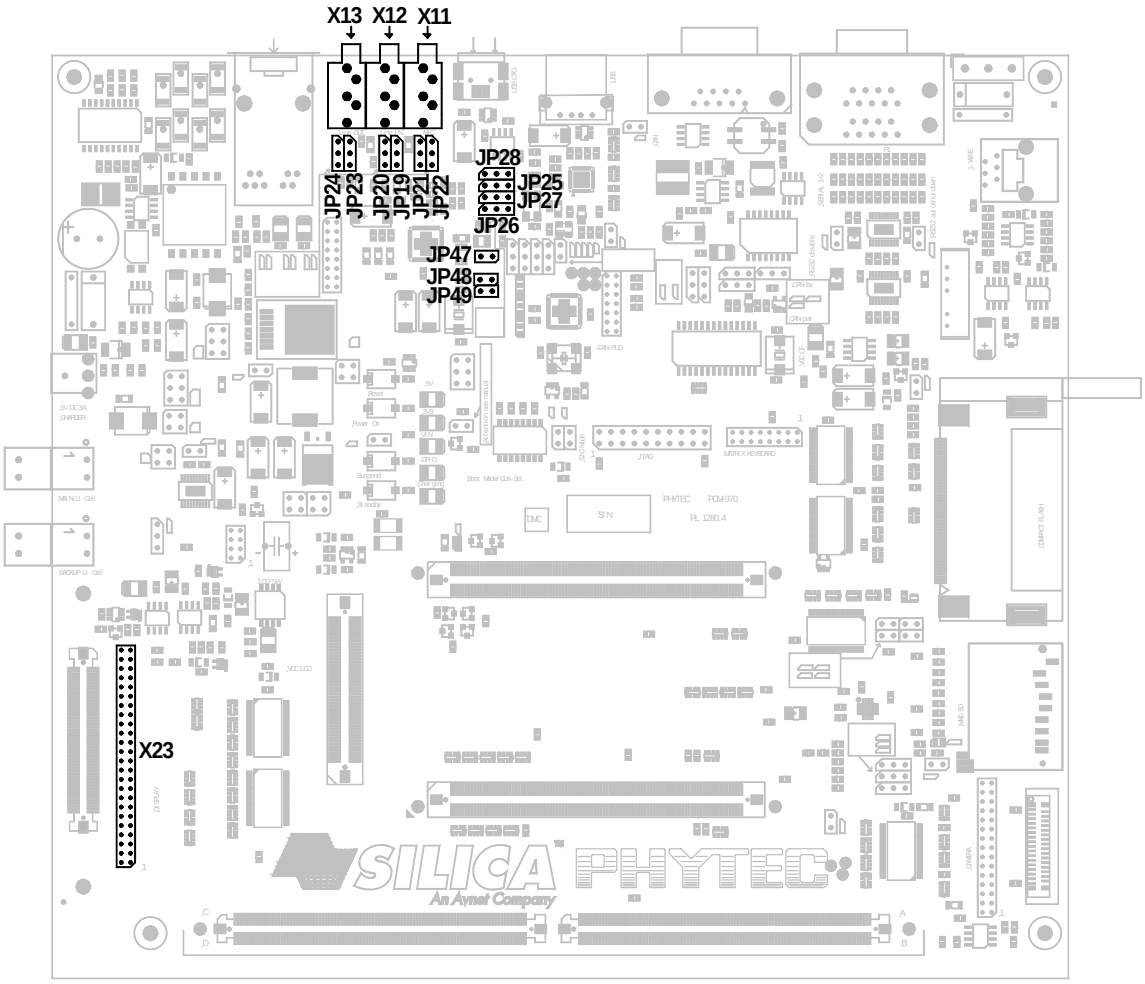

Figure 23: phyCORE-i.MX Carrier Board Audio/Touch Interface

With the phyCORE-i.MX31 module the MC13783 Power Management IC is used that has audio and touch functions integrated. So the i.MX31 module does not have to use the audio/touchscreen device (U24) on the i.MX Carrier Board.
To select that the PMIC audio and touch should be used, there are a variety of jumpers which have to be set.

A detailed list of all jumper settings you will find in *Table 29* below.

Table 29: Audio/Touchscreen Interface Jumper Settings[1]

JUMPER	SETTING	DESCRIPTION
JP19	1 + 2 **2 + 3**	Stereo output is managed on the baseboard **Stereo output is managed on the module**
JP20	1 + 2 **2 + 3**	Stereo output is managed on the baseboard **Stereo output is managed on the module**
JP21	1 + 2 **2 + 3**	Stereo MIC is managed on the baseboard **Stereo MIC is managed on the module**
JP22	1 + 2 **2 + 3**	Stereo MIC is managed on the baseboard **Stereo MIC is managed on the module**
JP23	1 + 2 **2 + 3**	Stereo LINE IN is managed on the baseboard **Stereo LINE IN is managed on the module**
JP24	1 + 2 **2 + 3**	Stereo LINE IN is managed on the baseboard **Stereo LINE IN is managed on the module**
JP25	1 + 2 **2 + 3**	Touch screen is managed on the baseboard **Touch screen is managed on the module**
JP26	1 + 2 **2 + 3**	Touch screen is managed on the baseboard **Touch screen is managed on the module**
JP27	1 + 2 **2 + 3**	Touch screen is managed on the baseboard **Touch screen is managed on the module**
JP28	1 + 2 **2 + 3**	Touch screen is managed on the baseboard **Touch screen is managed on the module**
JP47	**open** closed	**Reset is held high, no asserting by GPIO of i.MX module** Reset can be asserted by GPIO of i.MX module
JP48	**open** closed	**No access to IRQ via GPIO of i.MX module** Access to IRQ via GPIO of i.MX module
JP49	**open** closed	**No access to PENDOWN via GPIO of i.MX module** Access to PENDOWN via GPIO of i.MX module

Caution!
Jumper JP47 to JP49 always have to be opened with the phyCORE-i.MX31. Functions behind this jumpers are not available for the i.MX31 module.

1 Settings for the phyCORE-i.MX31 audio/touchscreen interface are in **bold blue**

14.3.7 USB Host

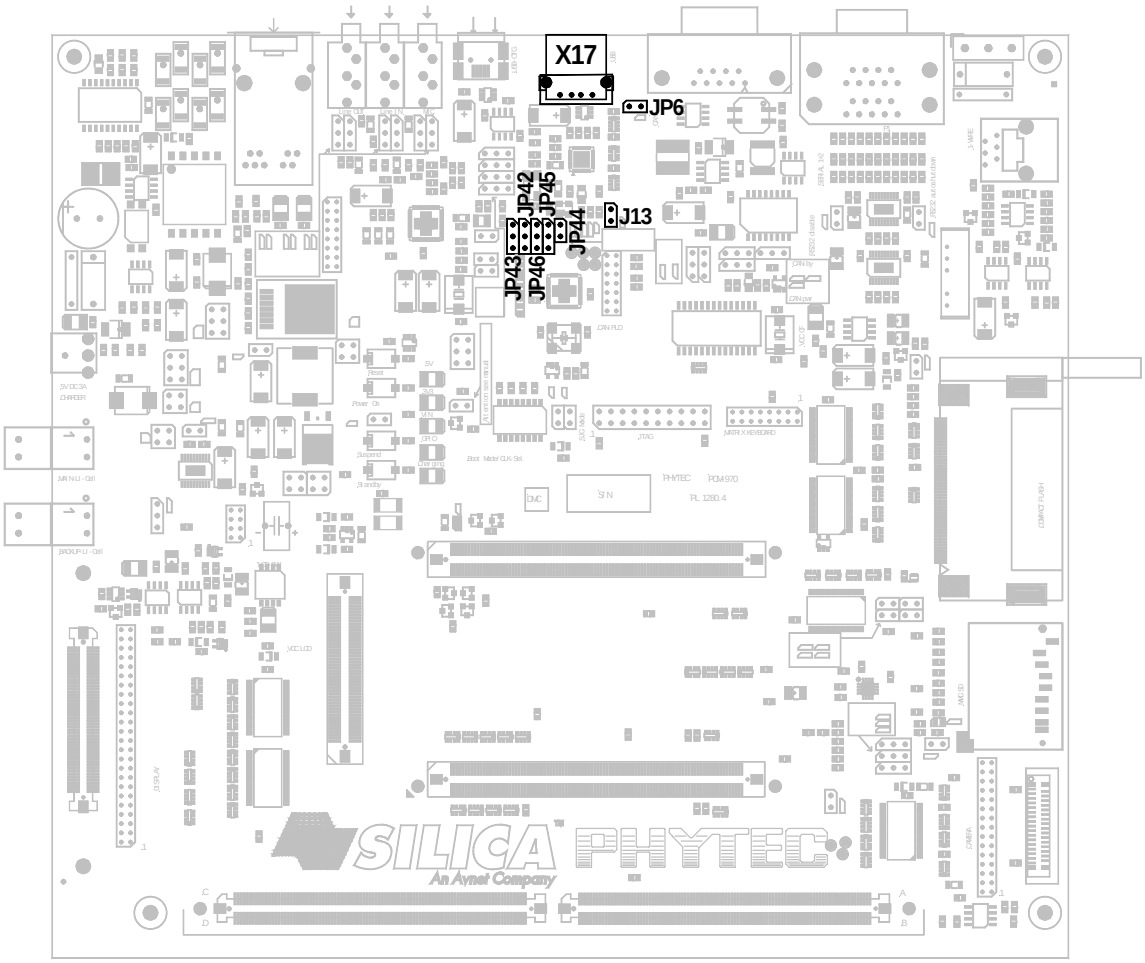

Figure 24: phyCORE-iMX Carrier Board USB-Host Interface

The i.MX31 controller supports control of input USB devices such as keyboard, mouse or USB key. To realize a USB Host interface the i.MX31 USB Host Controller (USBH2) uses the USB Host Transceiver (U26) of the i.MX Carrier Board.

For further details and jumper settings have a look at *section 3.*

Table 30: UBS Host interface jumper settings for i.MX31 module[1]

JUMPER	SETTING	DESCRIPTION
JP13	open **closed**	USB Host transceiver U26 is disabled, USB Host is out of operation **USB Host transceiver U26 is active, USB Host is in operation**
JP6	**open** closed	**Reset pin is held HIGH, no Reset asserted** Reset pin is connected to GPIO, Reset can be asserted
JP42	**1+2** 2+3	**USB Host is managed on the i.MX baseboard** USB Host is managed on the i.MX module
JP43	**1+2** 2+3	**USB Host is managed on the i.MX baseboard** USB Host is managed on the i.MX module
JP44	open **closed**	USB Host is managed on the i.MX module **USB Host is managed on the i.MX baseboard**
JP45	**1+2** 2+3	**USB Host is managed on the i.MX baseboard** USB Host is managed on the i.MX module
JP46	**1+2** 2+3	**USB Host is managed on the i.MX baseboard** USB Host is managed on the i.MX module

Caution!
With the phyCORE-i.MX31 jumper JP6 and JP42 to JP46 always have to be set as described in the table above. The alternative functions of this jumpers are not available for the i.MX31 module.

1 Settings for the phyCORE-i.MX31 USB-Host interface are in **bold blue**

14.3.8 LCD Connectors

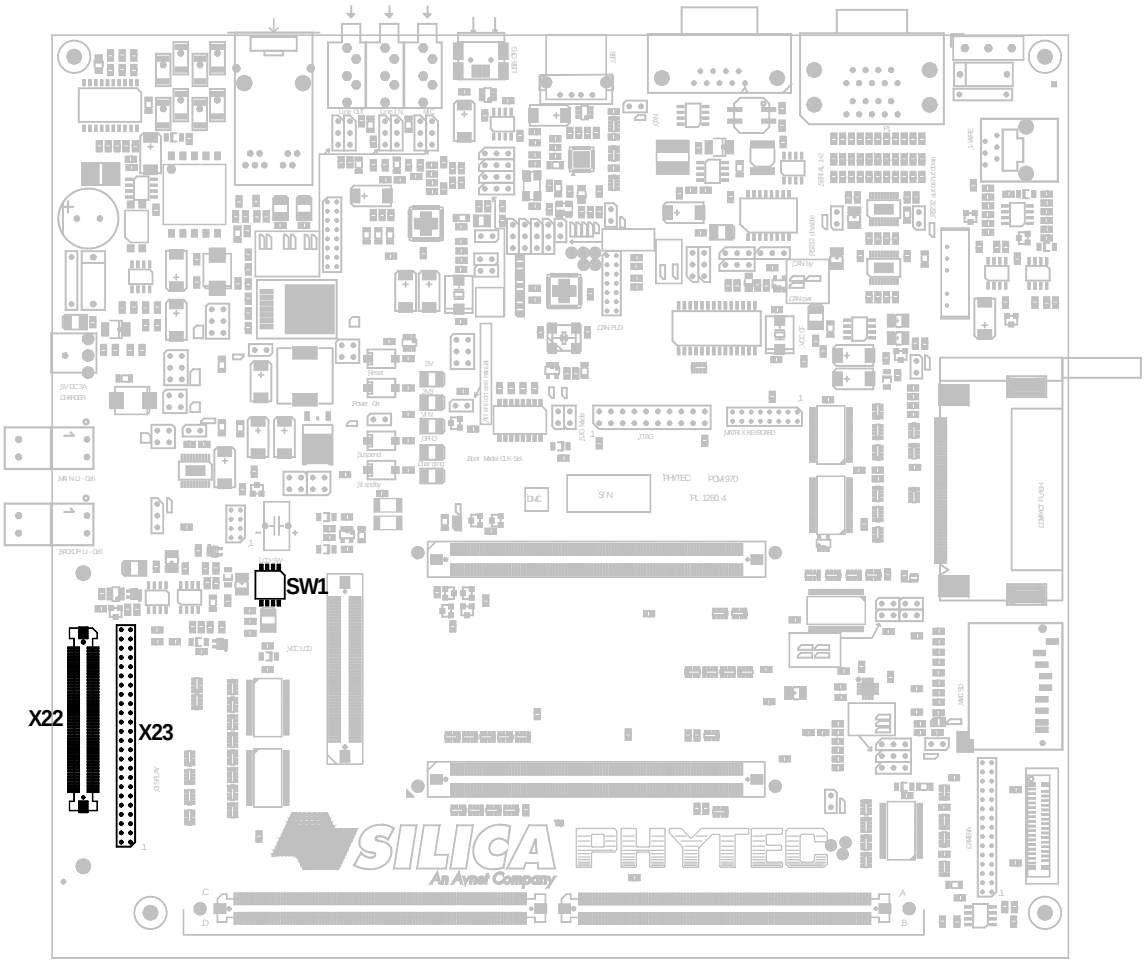

Figure 25: phyCORE-i.MX Carrier Board LCD Interfaces

The phyCORE-i.MX31 module comes with a 18-bit LCD interface. This 18-bit LCD interface is fully connected to the molex connectors X1 of the i.MX31 module and can be used in the customers application.

14.3.8.1 Serial LCD

Note:
Serial LCD is not supported by the phyCORE-i.MX31 module, because the i.MX31 microcontroller does not provide Serial LCD.

14.3.9 Camera Interface

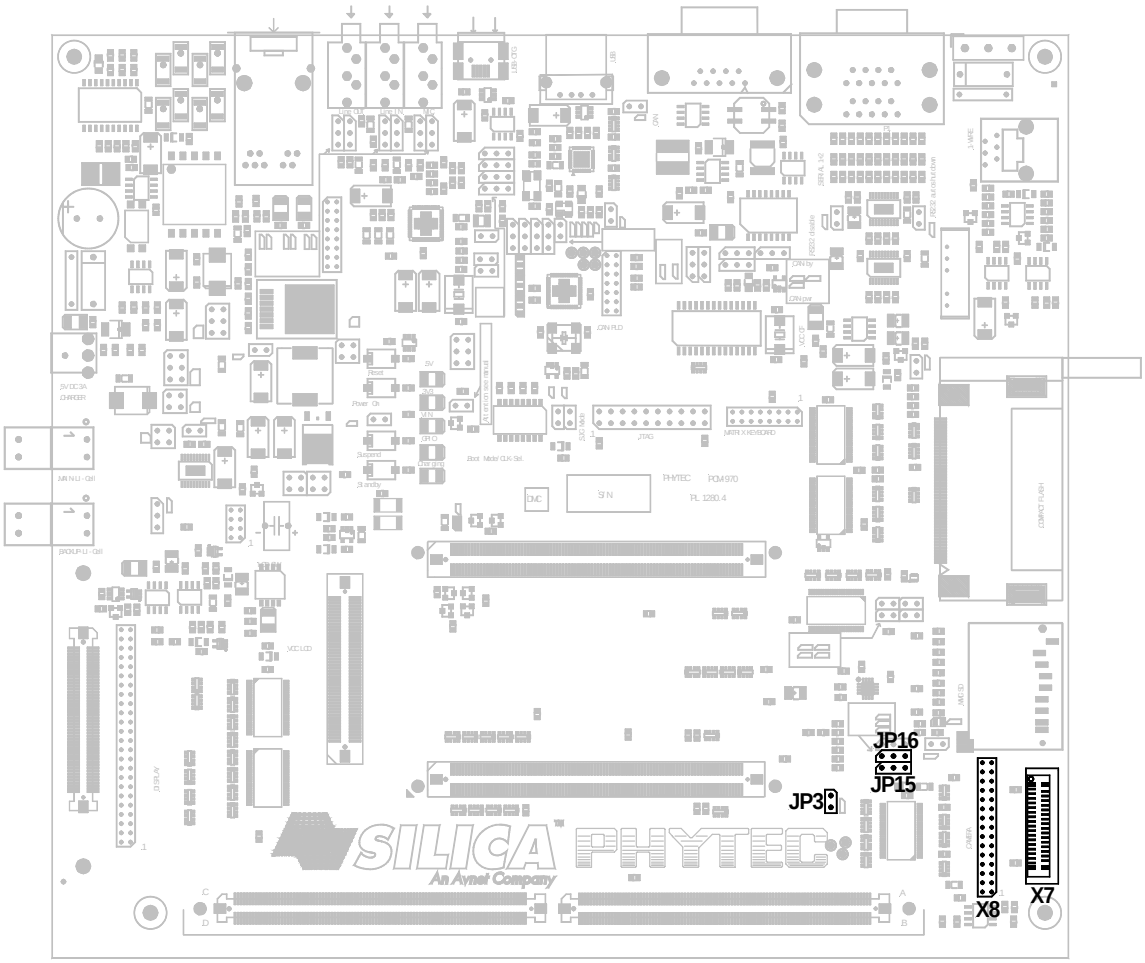

Figure 26: phyCORE-i.MX Carrier Board Camera Interface

The camera enable signal x_CSI_ENABLE of the i.MX Carrier Board is connected to one of three GPIO signals of the i.MX31 controller. These three GPIOs are x_MCU2_0, x_MCU2_3 and x_CSI_D5 (MCU3_5). Which of these GPIOs is used can be set by jumper J5 on the phyMAP-i.MX31 mapper. In standard configuration GPIO signal x_CSI_D5 (MCU3_5) is used.

Table 31: Camera Interface Jumper Settings for i.MX31 Module[1]

JUMPER	SETTING	DESCRIPTION
JP3	closed **open**	Outputs of level shifter U12 are enabled, CSI is active **Outputs of U12 are disabled or GPIO x_CSI_ENABLE can be used to control U12**
JP16	**1 + 2** 2 + 3	Jumper settings to chance camera sensor specific I²C address. For more information refer to the manual of the used camera sensor.
JP15	**1 + 2** 2 + 3	**Use of Camera Connector X7 with VCC_CAM supply (3.3 V)** Use of Camera Connector X8 with external VCC_CAM_EXT supply

1 Default Settings for the phyCORE-i.MX31 Camera Interface are in **bold blue**

14.3.9.1 PHYTEC Camera Connector

Note:
The phyCORE-i.MX31 module uses a 10-bit camera interface (CSI_D6 to CSI_D15) at the Camera Connectors. The camera interface is multiplexed with the ATA interface of the i.MX31 controller.

14.3.10 JTAG Interface

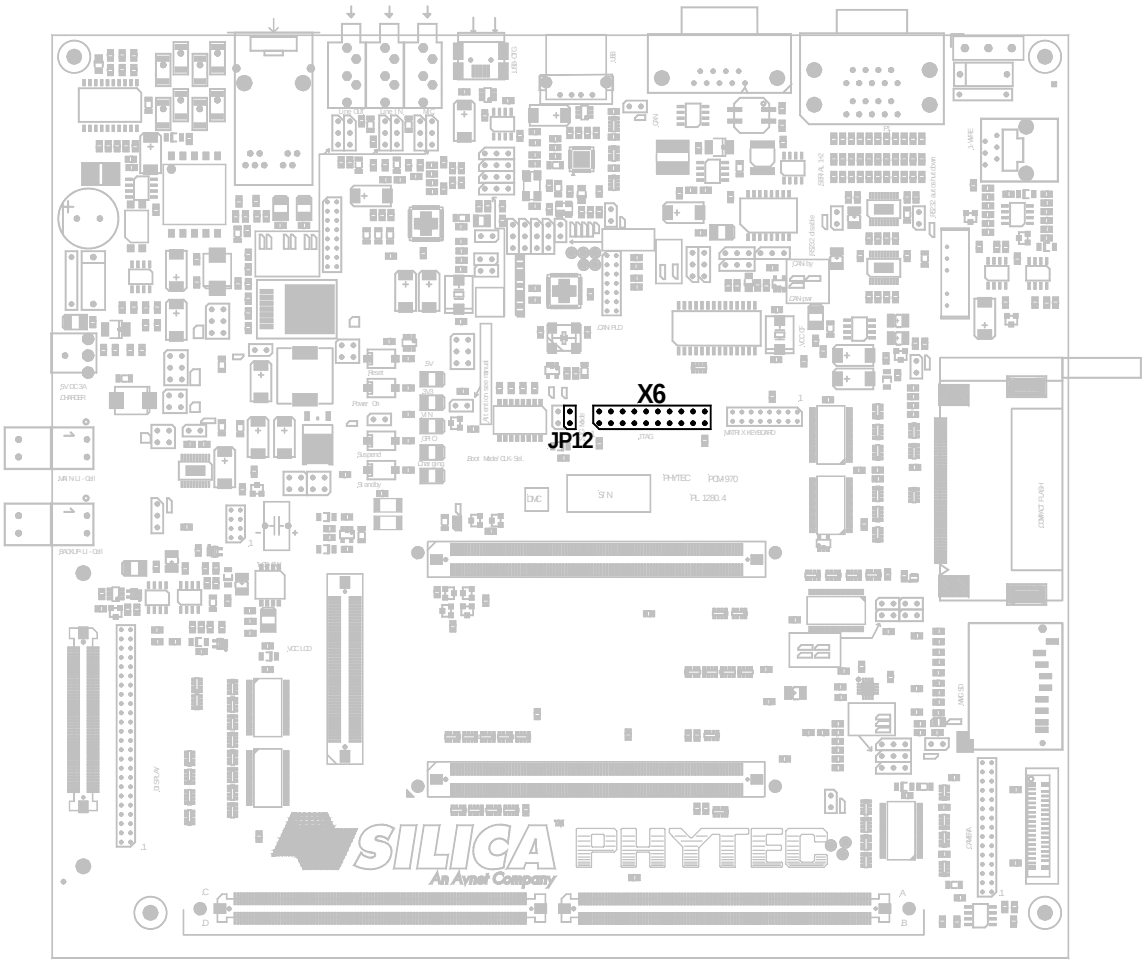

Figure 27: phyCORE-iMX Carrier Board JTAG Interface

Two JTAG modes are provided by the phyCORE-i.MX31 module dependent on the status of the SJC_MOD signal of the i.MX31 controller.
Jumper JP12 can be used to select the JTAG mode the controller should operate in.

Table 32: JTAG Jumper Settings for phyCORE-i.MX31 Module[1]

JUMPER	SETTING	NAME	DESCRIPTION
JP12	**closed**	**Daisy chain ALL**	**For common software debug, SDMA bypass is selected by default**
	open	SJC only	IEEE 1149.1 JTAG compatible mode

1 Default Settings for the phyCORE-i.MX31 JTAG Interface are in **bold blue**

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14.3.11 Complete Jumper Setting List for phyCORE-i.MX31 on the i.MX Carrier Board

The following table contains all jumper settings that can be set on the phyCORE-i.MX Carrier Board. Also it shows the default jumper settings for using the phyCORE-i.MX31 module with the i.MX Carrier Board. These default jumper settings are normally done prior to delivery.

Table 33: Jumper settings for i.MX31 module on i.MX Carrier Board[1]

JUMPER	SETTING	DESCRIPTION
JP1	**open**	**RS-232 transceivers are enabled**
	closed	RS-232 transceivers are disabled
JP2	**open**	**RS-232 auto shutdown is disabled**
	closed	RS-232 auto shutdown is enabled
JP3	**open**	**Camera interface is managed by x_CSI_ENABLE**
	closed	Camera interface is always enabled
JP4	open	Compact Flash is in overwrite mode
	closed	**Compact Flash is usable**
JP5	open	Compact-Flash is Slave
	closed	**Compact-Flash is Master**
JP6	**open**	**USBH2 transceiver Reset is not controllable**
	closed	USBH2 transceiver Reset is controllable via GPIO
JP7	**1+2**	**CAN is managed on the Carrier Board**
	2+3	CAN is managed on the module
JP8	1+2	CAN signals is are on the level VCC_CAN (from mapper)
	2+3	**CAN signals is are on the level VCC_5V**
JP9	**1+2**	**CAN is supplied via on Board 5V Power-Supply**
	2+3	CAN is supplied via an external Power-Supply
JP10	**1+2**	**CAN is managed on the Carrier Board**
	2+3	CAN is managed on the module
JP11	**1+2**	**CAN is supplied via on Board Power-Supply**
	2+3	CAN is supplied via an external Power-Supply
JP12	open	Only the System JTAG Controller
	closed	**All core's TAPS in a single daisy chain**
JP13	open	USB Host transceiver is disabled
	closed	**USB Host transceiver is enabled**
JP14	**open**	**VCC_FUSE = 2,775V (no FUSE programming)**
	closed	VCC_FUSE = 3,3V (use only for FUSE programming)
JP15	**1+2**	**Camera interface supplied via on-board 3.3V supply**
	2+3	Camera interface is supplied via external supply
JP16	**1+2**	**CMOS-Sensor I²C address is 0x55**
	2+3	CMOS-Sensor I²C Address is 0x33

1 Default settings are in **bold blue**

JP17	**open**	**Compact Flash expansion connector is enabled**
	closed	Compact Flash expansion connector is disabled
JP18	1+2	MMC driver is disabled
	2+3	**MMC driver is enabled**
JP19	1+2	Stereo output is managed on the baseboard
	2+3	**Stereo output is managed on the module**
JP20	1+2	Stereo output is managed on the baseboard
	2+3	**Stereo output is managed on the module**
JP21	1+2	Stereo MIC is managed on the baseboard
	2+3	**Stereo MIC is managed on the module**
JP22	1+2	Stereo MIC is managed on the baseboard
	2+3	**Stereo MIC is managed on the module**
JP23	1+2	Stereo LINE IN is managed on the baseboard
	2+3	**Stereo LINE IN is managed on the module**
JP24	1+2	Stereo LINE IN is managed on the baseboard
	2+3	**Stereo LINE IN is managed on the module**
JP25	1+2	Touch screen is managed on the baseboard
	2+3	**Touch screen is managed on the module**
JP26	1+2	Touch screen is managed on the baseboard
	2+3	**Touch screen is managed on the module**
JP27	1+2	Touch screen is managed on the baseboard
	2+3	**Touch screen is managed on the module**
JP28	1+2	Touch screen is managed on the baseboard
	2+3	**Touch screen is managed on the module**
JP29	1+2	Backup voltage is supplied by ext. LICELL
	2+3	**Backup voltage is supplied by onboard Goldcap**
JP30	1+2	VCC_BOOT is deep-sleep test voltage
	3+4	VCC_CLK is deep-sleep test voltage
	5+6	VCC_JTAG is deep-sleep test voltage
JP31	1+3,2+4	Power source is Power Over Ethernet (POE)
	3+5,4+6	**Power source is 5V adapter**
JP32	1+3,2+4	No power switching, direct supply of VCC_3V3
	3+5,4+6	**Separate supply path**
JP33	1+2,3+4	No power switching, direct supply from VCC_3V3
	open,open	**Separate supply path**
JP34	1+2,3+4	No power switching, direct supply from VCC_3V3
	open,open	**Separate supply path**
JP35	**open**	**VCC_5V Power Supply is enabled**
	closed	VCC_5V Power Supply is disabled
JP36	open	VCC_3V3 Power Supply is disabled
	closed	**VCC_3V3 Power Supply is enabled**

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JP37	open **closed**	Chargemode is Single Path **Chargemode is Dual Path**
JP38	**1+2,3+4** open,open	**Power switching, supply from 5V adapter or POE** No power switching, direct supply from VCC_3V3
JP39	**1+2,3+4** open,open	**Power switching active, Battery charge path closed** No power switching, direct supply from VCC_3V3
JP40	open **closed**	No power switching active, minimum circuit **Power switching active**
JP42	**1+2** 2+3	**USB VBUS power enable managed on baseboard** USB VBUS power enable managed on module
JP43	**1+2** 2+3	**USB VBUS overcurrent managed on the baseboard** USB VBUS overcurrent managed on the module
JP44	open **closed**	USB Host is managed on the module **USB Host is managed on the baseboard**
JP45	**1+2** 2+3	**USB Host is managed on the baseboard** USB Host is managed on the module
JP46	**1+2** 2+3	**USB Host is managed on the baseboard** USB Host is managed on the module
JP47	**open** closed	**Reset of audio/touch device is not controllable** Reset of audio/touch device is controllable via GPIO
JP48	**open** closed	**IRQ of audio/touch device is not controllable** IRQ of audio/touch device is controllable via GPIO
JP49	**open** closed	**PENDOWN of audio/touch device is not controllable** PENDOWN of audio/touch device is controllable via GPIO
JP50	open **closed**	SD card write protect is not connected to the module **SD card write protect is connected to the module**
JP602	**open** closed	**PC_RW inverted** PC_RW non-inverted
JP604	open **closed**	CF power is manged by x_EXP007 **Force enabling VCC_CFL**

15 Revision History

Date	Version numbers	Changes in this manual
16-July-2007	Manual L-700e_0 PCM-037 PCB# 1262.2 PCM-970 PCB# 1281.1	First draft, Preliminary documentation. Describes the phyCORE-i.MX31 with i.MX Baseboard.
August-2008	Manual L-700e_1 PCM-037 PCB# 1262.2 PCM-970 PCB# 1281.1	Second draft, Preliminary documentation. Describes the phyCORE-i.MX31 with i.MX Baseboard.
14-July-2009	Manual L-700e_2 PCM-037 PCB# 1262.2 PMA-001 PCB# 1283.1 PCM-970 PCB# 1281.4	Describes the phyCORE-i.MX31 with the phyMAP-i.MX31 and the i.MX Baseboard.

16 Component Placement Diagram

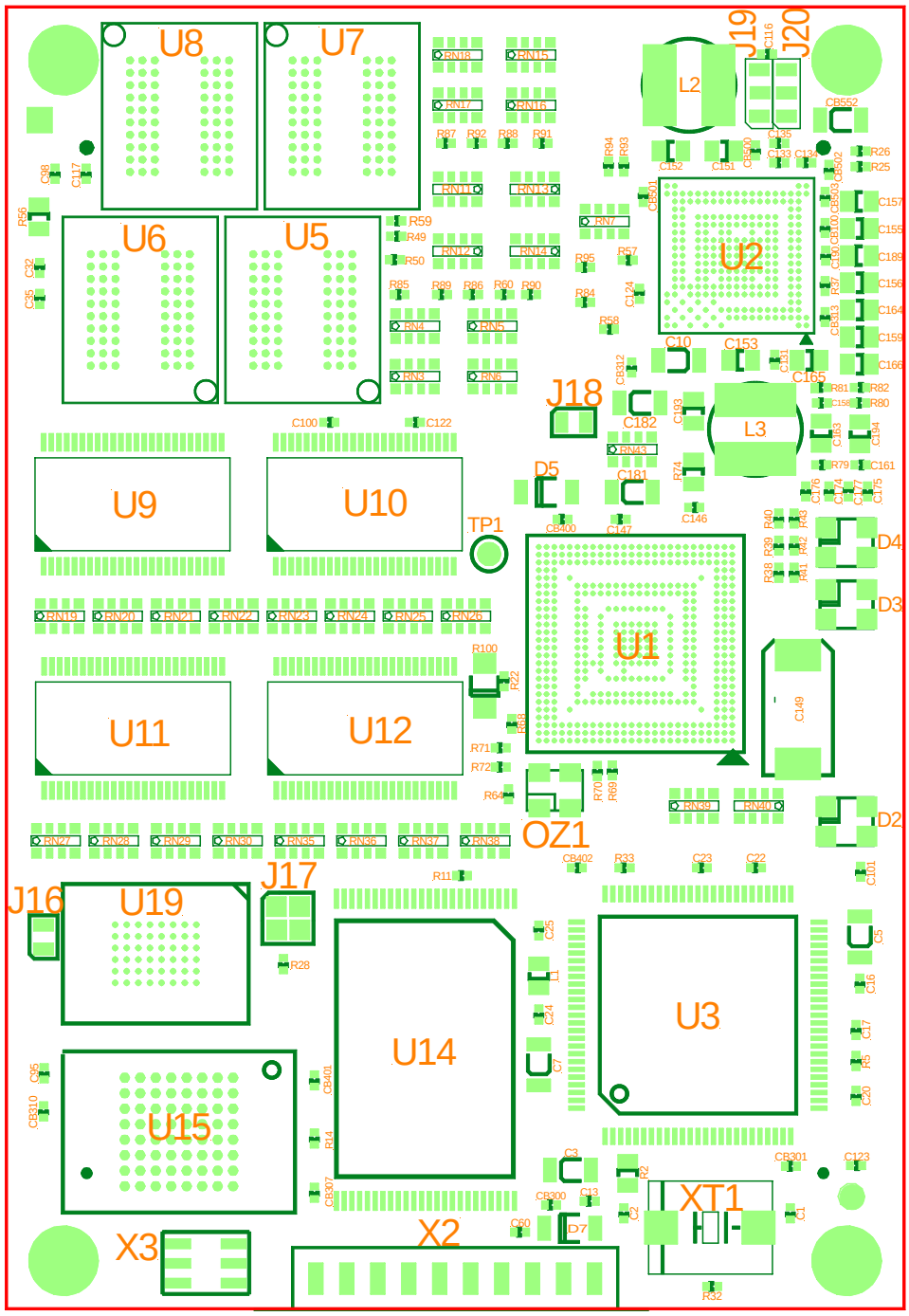

Figure 28: phyCORE-i.MX31 Component Placement (Top View)

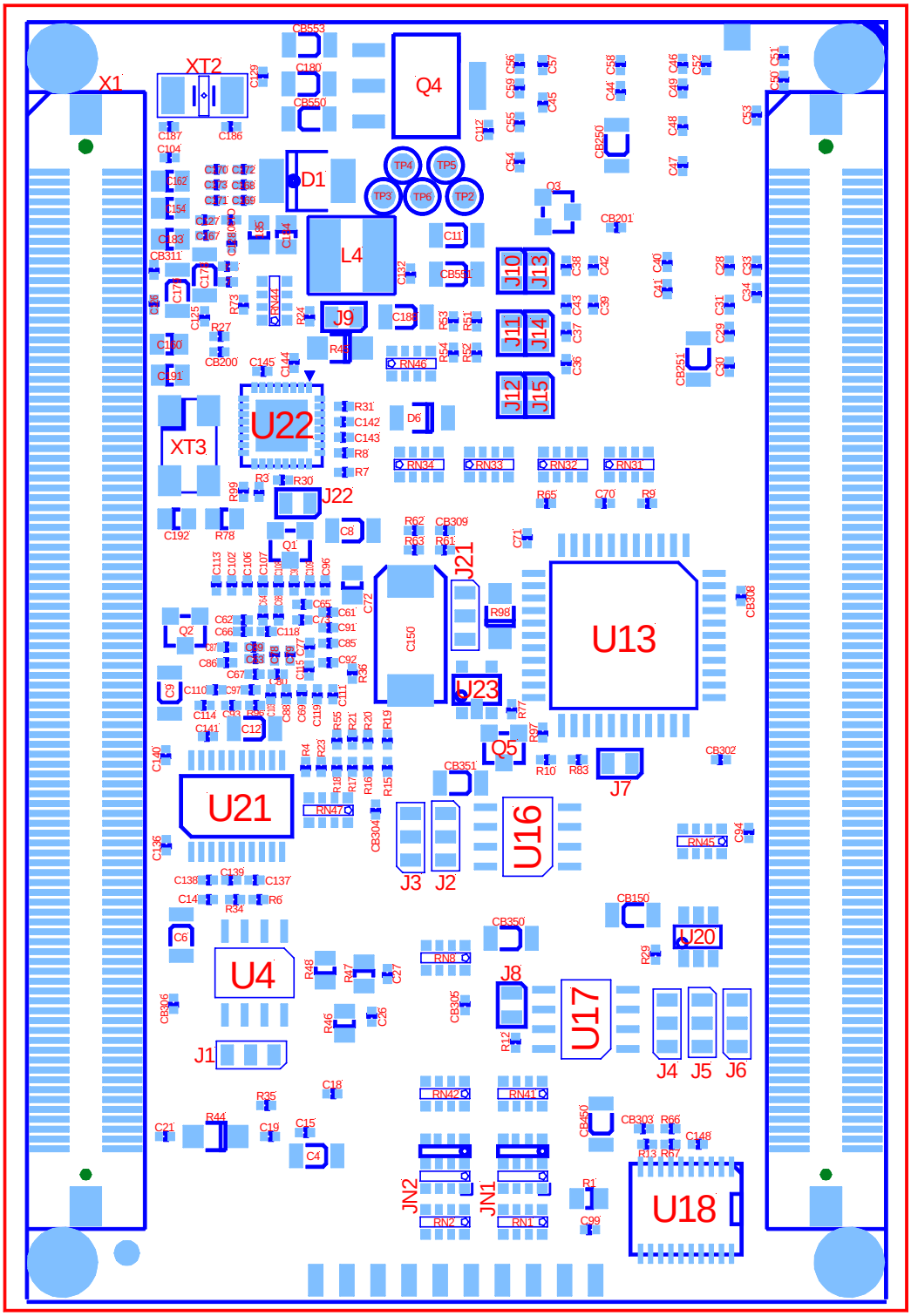

Figure 29: phyCORE-i.MX31 Component Placement (Bottom View)

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