PHYTEC

phyCORE-i.MX27

HARDWARE MANUAL

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	EUROPE	NORTH AMERICA
Address:	PHYTEC Technologie Holding AG Robert-Koch-Str. 39 D-55129 Mainz GERMANY	PHYTEC America LLC 203 Parfitt Way SW, Suite G100 Bainbridge Island, WA 98110 USA
Ordering Information:	+49 (800) 0749832 order@phytec.de	1 (800) 278-9913 sales@phytec.com
Technical Support:	+49 (6131) 9221-31 support@phytec.de	1 (800) 278-9913 support@phytec.com
Fax:	+49 (6131) 9221-33	1 (206) 780-9135
Web Site:	http://www.phytec.de	http://www.phytec.com

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1 Preface

This hardware manual describes the phyCORE-i.MX27 Single Board Computer's design and function. Precise specifications for the Freescale i.MX27 microcontrollers can be found in the enclosed microcontroller Data Sheet/User's Manual.

In this hardware manual and in the attached schematics, active low signals are denoted by a "/" or "#" preceding the signal name (e.g.: /RD or #RD). A "0" indicates a logic zero or low-level signal, while a "1" represents a logic one or high-level signal.

Declaration of Electro Magnetic Conformity of the PHYTEC phyCORE-I.MX27

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution!
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-i.MX27 is one of a series of PHYTEC Single Board Computers that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports a variety of 8-/16- and 32-bit controllers in two ways:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform

(2) as insert-ready, fully functional phyCORE OEM modules, which can be embedded directly into the user's peripheral hardware design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market. For more information go to:

http://www.phytec.com/services/phytec-advantage.html

1.1 Introduction

The phyCORE-i.MX27 belongs to PHYTEC's phyCORE Single Board Computer module family. The phyCORE SBCs represent the continuous development of PHYTEC Single Board Computer technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments the phyCORE board design features an increased pin package. The increased pin package allows dedication of approximately 20 % of all pin header connectors on the phyCORE boards to ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD components and laser-drilled microvias are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCORE-i.MX27 is a subminiature (84 x 60 mm) insert-ready Single Board Computer populated with the Freescale i.MX27 microcontroller. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to high-density pitch (0.635 mm) connectors aligning two sides of the board, allowing it to be plugged like a "big chip" into a target application.

Precise specifications for the controller populating the board can be found in the applicable controller User's Manual or datasheet. The descriptions in this manual are based on the Freescale i.MX27. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCORE-i.MX27.

The phyCORE-I.MX27 offers the following features:

- Subminiature Single Board Computer (84 x 60 mm) achieved through modern SMD technology
- Populated with the Freescale i.MX27 microcontroller (BGA404 packaging)
- Improved interference safety achieved through multi-layer PCB technology and dedicated ground pins
- Controller signals and ports extend to two 200-pin high-density (0.635 mm) Molex connectors aligning two sides of the board, enabling it to be plugged like a "big chip" into target application
- Max. 400 MHz core clock frequency
- Boot from NOR or NAND Flash
- 32 MByte (up to 64MByte) Intel Strata NOR Flash
- 64 MByte (up to 1 GByte) on-board NAND Flash[1]
- 128 MByte (up to 256 MByte) Mobile DDR SDRAM on-board
- RS-232 transceiver supporting one UART at data rates of up to 460kbps
- Full featured UART Interfaces without transceiver
- 32 KB I^2C EEPROM
- Separate I^2C RTC with backup function
- 512 Kbyte (up to 2MByte SRAM) with backup function
- Battery buffered controller based RTC with automatic battery switchover
- High-Speed USB OTG transceiver
- Auto FDX/MDX 100 MBit Ethernet Controller
- All controller required supplies generated on board by PMIC
- Synchronous 18Bit LCD-Interface
- PCMCIA/CF card Interface
- ATA-Interface DMA-Mode 3 (up to DMA-mode 5 without level-shifter) / CMOS Camera Interface
- Support of standard 20 pin debug interface through JTAG connector
- Keyboard support for up to 64 keys in a 8 * 8 matrix
- Two I^2C interfaces
- SD/MMC card interface with DMA
- Special Power-Management IC which includes:
  - Stereo line-in
  - Stereo line-out / pre-amplified mono-out
  - Stereo mic-in
  - 4-Wire touch interface
  - RTC
  - LCD-Backlight control
  - Battery charger
  - 6 AD-Inputs

1 *Please contact PHYTEC for more information about additional module configurations*.

1.2 Block Diagram

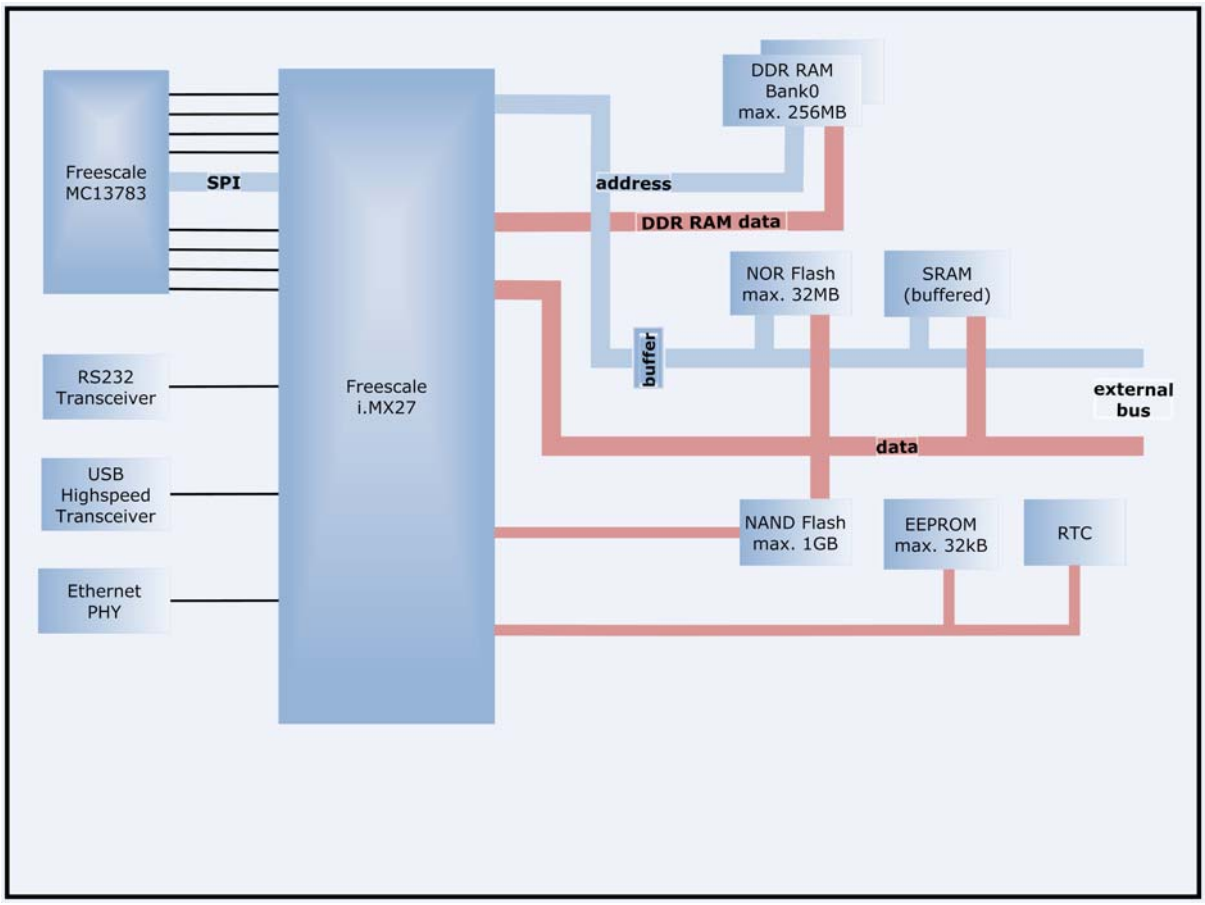

Figure 1: Block Diagram of the phyCore-i.MX27

1.3 View of the phyCORE-i.MX27

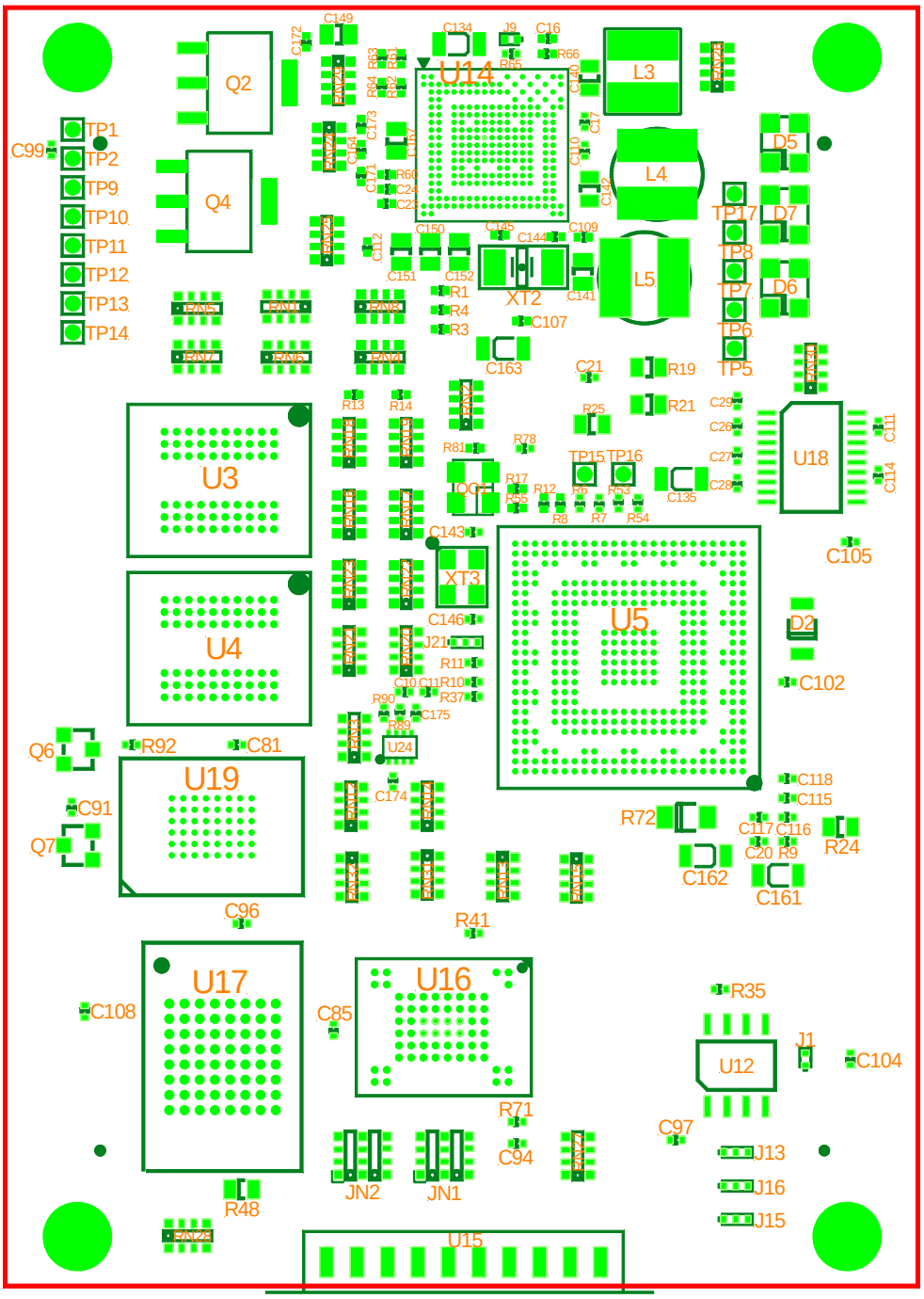

Figure 2: Top view of the phyCORE-i.MX27 (controller side)

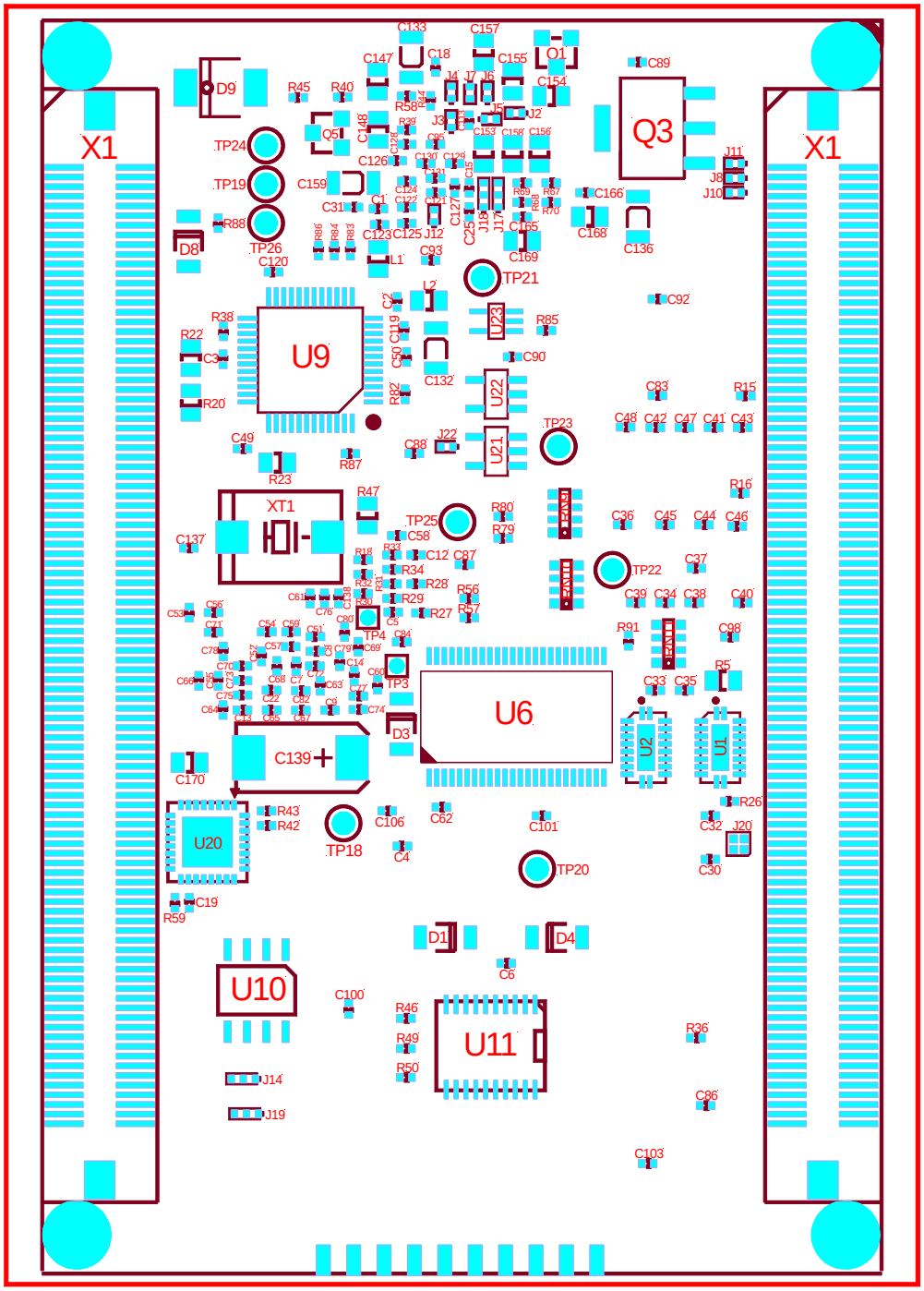

Figure 3: Bottom view of the phyCORE-i.MX27 (connector side)

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 4* indicates, all controller signals extend to surface mount technology (SMT) connectors (0.635 mm) lining two sides of the module (referred to as phyCORE-connector). This allows the phyCORE-i.MX27 to be plugged into any target application like a "big chip".

A new numbering scheme for the pins on the phyCORE-connector has been introduced with the phyCORE specifications. This enables quick and easy identification of desired pins and minimizes errors when matching pins on the phyCORE-module with the phyCORE-connector on the appropriate PHYTEC Development Board or in user target circuitry.

The numbering scheme for the phyCORE-connector is based on a two dimensional matrix in which column positions are identified by a letter and row position by a number. Pin 1A, for example, is always located in the upper left hand corner of the matrix. The pin numbering values increase moving down on the board. Lettering of the pin connector rows progresses alphabetically from left to right (*refer to Figure 4*).

The numbered matrix can be aligned with the phyCORE-i.MX27 (viewed from above; phyCORE-connector pointing down) or with the socket of the corresponding phyCORE Development Board/user target circuitry. The upper left-hand corner of the numbered matrix (pin 1A) is thus covered with the corner of the phyCORE-i.MX27 marked with a triangle. The numbering scheme is always in relation to the PCB as viewed from above, even if all connector contacts extend to the bottom of the module.

The numbering scheme is thus consistent for both the module’s phyCORE-connector as well as mating connectors on the phyCORE Development Board or target hardware, thereby considerably reducing the risk of pin identification errors.

Since the pins are exactly defined according to the numbered matrix previously described, the phyCORE-connector is usually assigned a single designator for its position (X1 for example). In this manner the phyCORE-connector comprises a single, logical unit regardless of the fact that it could consist of more than one physical socketed connector. The location of row 1 on the board is marked by a triangle on the PCB to allow easy identification.

The following figure (*Figure 4*) illustrates the numbered matrix system. It shows a phyCORE-i.MX27 with SMT phyCORE-connectors on its underside (defined as dotted lines) mounted on a Development Board. In order to facilitate understanding of the pin assignment scheme, the diagram presents a cross-view of the phyCORE-module showing these phyCORE-connectors mounted on the underside of the module’s PCB.

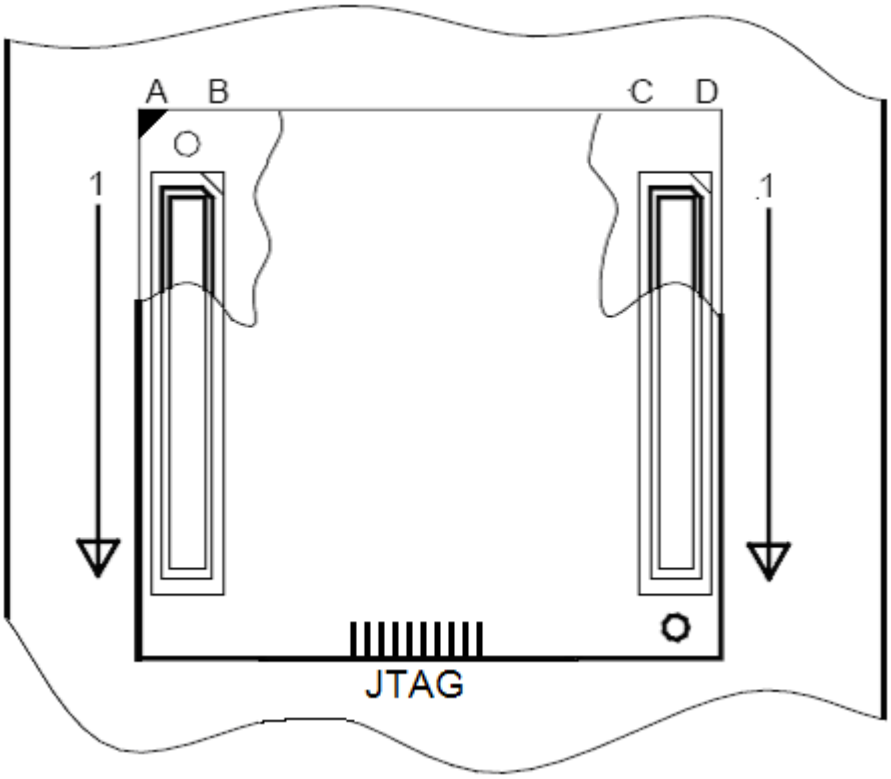

Figure 4: Pin-out of the phyCORE-Connector (top view, with cross section insert)

Table 1 provides an overview of the pin-out of the phyCORE-connector, as well as descriptions of possible alternative functions. *Table 1* also provides the appropriate signal level interface voltages listed in the SL (**S**ignal **L**evel) column. The Freescale i.MX27 is a multi-voltage operated microcontroller and as such special attention should be paid to the interface voltage levels to avoid unintentional damage to the microcontroller and other on-board components. *Please refer to the Freescale i.MX27 User's Manual/Data Sheet for details on the functions and features of controller signals and port pins*.

Note:
SL is short for Signal Level (V) and is the applicable logic level to interface a given pin.
Those pins marked as “N/A” have a range of applicable values that constitute proper operation.

Table 1: Pin-out of the phyCORE-Connector X1

PIN ROW X1A				
PIN #	SIGNAL	I/O	SL	DESCRIPTION
1A	NVDD7_12_14	O	NVDD7_12_14	LCD reference voltage (1.75 V - 2.8 V)
2A	GND	-	0	Ground 0 V
3A	not connected	-	-	Pin left unconnected
4A	not connected	-	-	Pin left unconnected
5A	X_VSYNC	I/O	NVDD7_12_14	Display vertical synchronization pulse
6A	X_OE_ACD	O	NVDD7_12_14	Alternate crystal direction/output enable
7A	GND	-	0	Ground 0 V
8A	X_REV	O	NVDD7_12_14	REV signal for display
9A	X_SPL_SPR	O	NVDD7_12_14	SPL/SPR signal for display
10A	X_PS	O	NVDD7_12_14	Control signal output for source driver
11A	Not connected	-	-	Pin left unconnected
12A	GND	-	0	Ground 0 V
13A	X_LD0	I/O	NVDD7_12_14	Input/Output data to display
14A	X_LD2	I/O	NVDD7_12_14	Input/Output data to display
15A	X_LD3	I/O	NVDD7_12_14	Input/Output data to display
16A	X_LD5	I/O	NVDD7_12_14	Input/Output data to display
17A	GND	-	0	Ground 0V
18A	X_LD8	I/O	NVDD7_12_14	Input/Output data to display
19A	X_LD10	I/O	NVDD7_12_14	Input/Output data to display
20A	X_LD11	I/O	NVDD7_12_14	Input/Output data to display
21A	X_LD13	I/O	NVDD7_12_14	Input/Output data to display
22A	GND	-	0	Ground 0 V
23A	X_LD17	I/O	NVDD7_12_14	Input/Output data to display
24A	X_#CS0	O	NVDD1_2_3_4_5	Chip Select 0 output
25A	X_#CS1	O	NVDD1_2_3_4_5	Chip Select 1 output
26A	X_#CS4	O	NVDD1_2_3_4_5	Chip Select 4 output
27A	GND	-	0	Ground 0 V
28A	X_#PC_IORD/#EB1	O	NVDD1_2_3_4_5	Active low external enable byte signal that controls D [7:0]
29A	X_#PC_IOWR/#OE	O	NVDD1_2_3_4_5	Memory Output Enable
30A	X_#LBA	O	NVDD1_2_3_4_5	Load Burst Address
31A	X_BCLK	O	NVDD1_2_3_4_5	Burst Clock
32A	GND	-	0	Ground 0 V
33A	X_A2	O	NVDD1_2_3_4_5	Address-Line A2

34A	X_A4	O	NVDD1_2_3_4_5	Address-Line A4
35A	X_A5	O	NVDD1_2_3_4_5	Address-Line A5
36A	X_A7	O	NVDD1_2_3_4_5	Address-Line A7
37A	GND	-	0	Ground 0 V
38A	X_A10	O	NVDD1_2_3_4_5	Address-Line A10
39A	X_A12	O	NVDD1_2_3_4_5	Address-Line A12
40A	X_A13	O	NVDD1_2_3_4_5	Address-Line A13
41A	X_A15	O	NVDD1_2_3_4_5	Address-Line A15
42A	GND	-	0	Ground 0 V
43A	X_A18	O	NVDD1_2_3_4_5	Address-Line A18
44A	X_A20	O	NVDD1_2_3_4_5	Address-Line A20
45A	X_A21	O	NVDD1_2_3_4_5	Address-Line A21
46A	X_A23	O	NVDD1_2_3_4_5	Address-Line A23
47A	GND	-	0	Ground 0 V
48A	X_D0	I/O	NVDD1_2_3_4_5	Data_Bus D0
49A	X_D2	I/O	NVDD1_2_3_4_5	Data_Bus D2
50A	X_D3	I/O	NVDD1_2_3_4_5	Data_Bus D3
51A	X_D5	I/O	NVDD1_2_3_4_5	Data_Bus D5
52A	GND	-	0	Ground 0 V
53A	X_D8	I/O	NVDD1_2_3_4_5	Data_Bus D8
54A	X_D10	I/O	NVDD1_2_3_4_5	Data_Bus D10
55A	X_D11	I/O	NVDD1_2_3_4_5	Data_Bus D11
56A	X_D13	I/O	NVDD1_2_3_4_5	Data_Bus D13
57A	GND	-	0	Ground 0 V
58A	X_PC_BVD1	I	NVDD1_2_3_4_5	PCMCIA Battery Voltage Detect Input 1
59A	X_PC_BVD2	I	NVDD1_2_3_4_5	PCMCIA Battery Voltage Detect Input 2
60A	X_#PC_CD1	I	NVDD1_2_3_4_5	PCMCIA Card Detect Input 1
61A	X_PC_PWRON	I	NVDD1_2_3_4_5	PCMCIA Power is ON Signal
62A	GND	-	0	Ground 0 V
63A	X_#PC_RW	O	NVDD1_2_3_4_5	PCMCIA External Transceiver Direction Signal
64A	X_PC_VS1	I	NVDD1_2_3_4_5	PCMCIA Voltage sense Input 1
65A	X_PC_VS2	I	NVDD1_2_3_4_5	PCMCIA Voltage sense Input 2
66A	X_CE0	O	NVDD1_2_3_4_5	PCMCIA Card Enable 0 Signal
67A	GND	-	0	Ground 0 V
68A	X_IOIS16	I	NVDD1_2_3_4_5	PCMCIA I/O port is 16-bits
69A	X_FEC_TXD3	O	NVDD6_8_9_10	Fast Ethernet Transmit Data 3
70A	X_FEC_RX_ER	I	NVDD6_8_9_10	Fast Ethernet Receive Data Error
71A	X_FEC_RXD2	I	NVDD6_8_9_10	Fast Ethernet Receive Data 2
72A	GND	-	0	Ground 0 V
73A	X_FEC_MDC	O	NVDD6_8_9_10	Fast Ethernet Management Data Clock
74A	X_FEC_TX_CLK	O	NVDD6_8_9_10	Fast Ethernet Transmit Clock signal

75A	X_FEC_RXD0	I	NVDD6_8_9_10	Fast Ethernet Receive Data 0
76A	X_FEC_RX_CLK	I	NVDD6_8_9_10	Fast Ethernet Receive Clock signal
77A	GND	-	0	Ground 0 V
78A	X_CSI_D0	I	NVDD11	Camera Sensor D0
79A	X_CSI_D2	I	NVDD11	Camera Sensor D2
80A	X_CSI_D3	I	NVDD11	Camera Sensor D3
81A	X_CSI_D5	I	NVDD11	Camera Sensor D5
82A	GND	-	0	Ground 0 V
83A	NVDD11	O	NVDD11	Camera reference voltage (2.8 V)
84A	X_CSI_MCLK	O	NVDD11	Camera Sensor Master Clock
85A	X_CSI_VSYNC	I	NVDD11	Camera Sensor vertical sync
86A	X_CSI_PIXCLK	I	NVDD11	Camera Sensor data latch clock
87A	GND	-	0	Ground 0 V
88A	X_KP_COL0	I/O	NVDD6_8_9_10	Keypad Port Column 0
89A	X_KP_COL1	I/O	NVDD6_8_9_10	Keypad Port Column 1
90A	X_KP_COL2	I/O	NVDD6_8_9_10	Keypad Port Column 2
91A	X_KP_ROW0	I/O	NVDD6_8_9_10	Keypad Port Row 0
92A	GND	-	0	Ground 0 V
93A	X_KP_ROW3	I/O	NVDD6_8_9_10	Keypad Port Row 3
94A	X_KP_ROW5	I/O	NVDD6_8_9_10	Keypad Port Row 5
95A	X_PC28	I/O	NVDD6_8_9_10	GPIO PC28
96A	not connected	-	-	Pin left unconnected
97A	GND	-	0	Ground 0 V
98A	X_PC29	I/O	NVDD6_8_9_10	GPIO PC29
99A	X_PC30	I/O	NVDD6_8_9_10	GPIO PC30
100A	X_PC31	I/O	NVDD6_8_9_10	GPIO PC31

PIN ROW X1B				
PIN #	SIGNAL	I/O	SL	DESCRIPTION
1B	X_WDI	I	LV	Watchdog input has to be kept high by the processor to keep MC13783 active
2B	X_VSTBY	I	LV	Signal from primary processor to put MC13783 in a low power mode
3B	X_PWGT1EN	I	LV	Power gate driver 1 enable
4B	GND	-	0	Ground 0 V
5B	X_HSYNC	I/O	NVDD7_12_14	Display horizontal synchronization pulse
6B	not connected	-	-	Pin left unconnected
7B	X_CONTRAST	O	NVDD7_12_14	Contrast control for display
8B	X_CLS	O	NVDD7_12_14	CLS signal for display
9B	GND	-	0	Ground 0 V
10B	X_LSCLK	O	NVDD7_12_14	Display Shift Clock
11B	not connected	-	-	Pin left unconnected
12B	not connected	-	-	Pin left unconnected
13B	X_LD1	I/O	NVDD7_12_14	Input/Output data to display
14B	GND	-	0	Ground 0 V
15B	X_LD4	I/O	NVDD7_12_14	Input/Output data to display
16B	X_LD6	I/O	NVDD7_12_14	Input/Output data to display
17B	X_LD7	I/O	NVDD7_12_14	Input/Output data to display
18B	X_LD9	I/O	NVDD7_12_14	Input/Output data to display
19B	GND	-	0	Ground 0 V
20B	X_LD12	I/O	NVDD7_12_14	Input/Output data to display
21B	X_LD14	I/O	NVDD7_12_14	Input/Output data to display
22B	X_LD15	I/O	NVDD7_12_14	Input/Output data to display
23B	X_LD16	I/O	NVDD7_12_14	Input/Output data to display
24B	GND	-	0	Ground 0 V
25B	X_#CSD1	O	NVDD1_2_3_4_5	Chip Select Output 1 for SDRAM
26B	X_#CS5	O	NVDD1_2_3_4_5	Chip Select Output 5
27B	X_#PC_REG/#EB0	O	NVDD1_2_3_4_5	Active low external enable byte signal that controls D [15:8]
28B	X_#PC_WE/#RW	O	NVDD1_2_3_4_5	#RW signal—Indicates whether external access is a read (high) or write (low) cycle
29B	GND	-	0	Ground 0 V
30B	X_#ECB	I	NVDD1_2_3_4_5	Active low signal sent by flash device
31B	X_A0	O	NVDD1_2_3_4_5	Address-Line A0
32B	X_A1	O	NVDD1_2_3_4_5	Address-Line A1
33B	X_A3	O	NVDD1_2_3_4_5	Address-Line A3
34B	GND	-	0	Ground 0 V
35B	X_A6	O	NVDD1_2_3_4_5	Address-Line A6

36B	X_A8	O	NVDD1_2_3_4_5	Address-Line A8
37B	X_A9	O	NVDD1_2_3_4_5	Address-Line A9
38B	X_A11	O	NVDD1_2_3_4_5	Address-Line A11
39B	GND	-	0	Ground 0 V
40B	X_A14	O	NVDD1_2_3_4_5	Address-Line A14
41B	X_A16	O	NVDD1_2_3_4_5	Address-Line A16
42B	X_A17	O	NVDD1_2_3_4_5	Address-Line A17
43B	X_A19	O	NVDD1_2_3_4_5	Address-Line A19
44B	GND	-	0	Ground 0 V
45B	X_A22	O	NVDD1_2_3_4_5	Address-Line A22
46B	X_A24	O	NVDD1_2_3_4_5	Address-Line A24
47B	X_A25	O	NVDD1_2_3_4_5	Address-Line A25
48B	X_D1	I/O	NVDD1_2_3_4_5	Data_Bus D1
49B	GND	-	0	Ground 0 V
50B	X_D4	I/O	NVDD1_2_3_4_5	Data_Bus D4
51B	X_D6	I/O	NVDD1_2_3_4_5	Data_Bus D6
52B	X_D7	I/O	NVDD1_2_3_4_5	Data_Bus D7
53B	X_D9	I/O	NVDD1_2_3_4_5	Data_Bus D9
54B	GND	-	0	Ground 0 V
55B	X_D12	I/O	NVDD1_2_3_4_5	Data_Bus D12
56B	X_D14	I/O	NVDD1_2_3_4_5	Data_Bus D14
57B	X_D15	I/O	NVDD1_2_3_4_5	Data_Bus D15
58B	X_#FL_WP	I		Flash Protection Signal
59B	GND	-	0	Ground 0 V
60B	X_#PC_CD2	I	NVDD1_2_3_4_5	PCMCIA Card Detect Input 2
61B	X_PC_POE	O	NVDD1_2_3_4_5	PCMCIA buffers output enable
62B	X_PC_READY	I	NVDD1_2_3_4_5	PCMCIA Ready
63B	X_PC_RST	O	NVDD1_2_3_4_5	PCMCIA Card Reset
64B	GND	-	0	Ground 0 V
65B	X_#PC_WAIT	I	NVDD1_2_3_4_5	PCMCIA Extend bus cycle Input
66B	X_CE1	O	NVDD1_2_3_4_5	PCMCIA Card Enable 1 Signal
67B	NVDD1_2_3_4_5	O	NVDD1_2_3_4_5	
68B	X_FEC_TXD2	O	NVDD6_8_9_10	Fast Ethernet Transmit Data 2
69B	GND	-	0	Ground 0 V
70B	X_FEC_RXD1	I	NVDD6_8_9_10	Fast Ethernet Receive Data 1
71B	X_FEC_RXD3	I	NVDD6_8_9_10	Fast Ethernet Receive Data 3
72B	X_FEC_MDIO	I/O	NVDD6_8_9_10	Fast Ethernet Management Data Input/Output
73B	X_FEC_CRS	I	NVDD6_8_9_10	Fast Ethernet Carrier Sense enable
74B	GND	-	0	Ground 0 V
75B	X_FEC_RX_DV	I	NVDD6_8_9_10	Fast Ethernet Receive data Valid signal
76B	X_FEC_COL	I	NVDD6_8_9_10	Fast Ethernet Collision signal

77B	X_FEC_TX_ER	O	NVDD6_8_9_10	Fast Ethernet Transmit Data Error
78B	X_CSI_D1	I	NVDD11	Camera Sensor D1
79B	GND	-	0	Ground 0 V
80B	X_CSI_D4	I	NVDD11	Camera Sensor D4
81B	X_CSI_D6	I	NVDD11	Camera Sensor D6
82B	X_CSI_D7	I	NVDD11	Camera Sensor D7
83B	X_FEC_TX_EN	O	NVDD6_8_9_10	Fast Ethernet Transmit enable signal
84B	GND	-	0	Ground 0 V
85B	X_CSI_HSYNC	I	NVDD11	Camera Sensor horizontal sync
86B	X_FEC_TXD0	O	NVDD6_8_9_10	Fast Ethernet Transmit Data 0
87B	X_FEC_TXD1	O	NVDD6_8_9_10	Fast Ethernet Transmit Data 1
88B	NVDD6_8_9_10	O	NVDD6_8_9_10	Keypad reference voltage (2.775 V)
89B	GND	-	0	Ground 0 V
90B	X_KP_COL3	I/O	NVDD6_8_9_10	Keypad Port Column 3
91B	X_KP_ROW1	I/O	NVDD6_8_9_10	Keypad Port Row 1
92B	X_KP_ROW2	I/O	NVDD6_8_9_10	Keypad Port Row 2
93B	X_KP_ROW4	I/O	NVDD6_8_9_10	Keypad Port Row 4
94B	GND	-	0	Ground 0V
95B	X_KP_COL4	I/O	NVDD6_8_9_10	Keypad Port Column 4
96B	X_KP_COL5	I/O	NVDD6_8_9_10	Keypad Port Column 5
97B	not connected	-	-	Pin left unconnected
98B	not connected	-	-	Pin left unconnected
99B	GND	-	0	Ground 0 V
100B	X_CLKO	O	NVDD1_2_3_4_5	Clock out signal selected from internal clock signals

PIN ROW X1C				
PIN #	SIGNAL	I/O	SL	DESCRIPTION
1C	VIN	-	Power	Main Power Input (3:3 V – 4.5 V)
2C	VIN	-	Power	Main Power Input (3.3 V – 4.65 V)
3C	GND	-	0	Ground 0 V
4C	VIN	-	Power	Main Power Input (3.3 V – 4.65 V)
5C	VIN	-	Power	Main Power Input (3.3 V – 4.65 V)
6C	Not connected	-	-	Pin left unconnected
7C	GND	-	0	Ground 0 V
8C	VCC_3V3	-	Power	Power for 3.3 V devices
9C	VCC_3V3	-	Power	Power for 3.3 V devices
10C	VCC_3V3	-	Power	Power for 3.3 V devices
11C	VCC_3V3	-	Power	Power for 3.3 V devices
12C	GND	-	0	Ground 0 V
13C	X_POWER_BATT	I	VATLAS (2.50 V - 2.86 V)	1. Battery positive terminal 2. Battery current sensing point 2 3. Battery supply voltage sense
14C	X_BATTISNS	I	VATLAS	Battery current sensing point 1
15C	X_BATTFET	O	VATLAS	Driver output for battery path FET
16C	X_CHRGISNSP	I	VATLAS	Charge current sensing point 1
17C	GND	-	0	Ground 0 V
18C	X_BKUP_SUPPLY	I	MV	1. Coincell supply input 2. Coincell charger output
19C	X_CHRGLED	O	EHV	Trickle LED driver output
20C	X_CHRGMOD0	I	VATLAS	Selection of the mode of charging
21C	X_CHRGMOD1	I	VATLAS	Selection of the mode of charging
22C	GND	-	0	Ground 0 V
23C	X_RXOUTL_LSPP	O	VAUDIO	J18=1+2 Loudspeaker positive terminal J18=2+3 Low power receive output for accessories left channel
24C	X_RXOUTR_LSPM	O	VAUDIO	J17=1+2 Loudspeaker minus terminal J17=2+3 Low power receive output for accessories right channel
25C	X_RXINL	I	VAUDIO	Receive input left channel
26C	X_RXINR	I	VAUDIO	Receive input right channel
27C	GND	-	0	Ground 0 V
28C	X_MC1RIN	I	VAUDIO	Right microphone amplifier input
29C	X_MC1LIN	Ì	VAUDIO	Left microphone amplifier input
30C	X_#ON1	I	LV	Power on/off button connection 1

31C	X_#ON2	I	LV	Power on/off button connection 2
32C	GND	-	0	Ground 0 V
33C	X_ETH_LINK	O	3.3V	Ethernet Link & Activity Indicator (Open Drain)
34C	X_ETH_SPEED	O	3.3V	Ethernet Speed Indicator (Open Drain)
35C	X_ETH_RX-	I/O	3.3V	Receive negative input (normal) Transmit negative output (reversed)
36C	X_ETH_TX-	I/O	3.3V	Transmit negative output (normal) Receive negative input (reversed)
37C	GND	-	0	Ground 0 V
38C	X_ETH_#PD	I	3.3V	Ethernet Chip power down input
39C	X_ETH_#INT	O	3.3V	Management Interface (MII) Interrupt Out
40C	NVDD6_8_9_10	O	NVDD6_8_9_10	JTAG reference voltage (2.775 V)
41C	X_#TRST	I	NVDD6_8_9_10	JTAG reset
42C	GND	-	0	Ground 0 V
43C	X_#BATTDET	O	LV	Battery thermistor presence detect output
44C	X_ADIN5	I	LV	Analog Input Channel 5
45C	X_ADIN6	I	LV	Analog Input Channel 6
46C	X_ADIN7	I	LV	Analog Input Channel 7
47C	GND	-	0	Ground 0 V
48C	X_ADOUT	O	LV	ADC trigger output
49C	X_ADTRIG	I	LV	ADC trigger input
50C	X_#LOWBAT	O	LV	Low battery detection signal
51C	X_USEROFF	I	LV	Signal from processor to confirm user off mode after a power fail
52C	GND	-	0	Ground 0 V
53C	X_VBUS	I/O	5V (SW3)	USB VBUS Voltage
54C	X_UDM	I/O	3.3V	USB transceiver cable interface, D-
55C	X_UDP	I/O	3.3V	USB transceiver cable interface, D+
56C	X_UID	I/O	3.3V	USB on the go transceiver cable ID resistor connection
57C	GND	-	0	Ground 0 V
58C	X_PB24	I/O	NVDD7_12_14	GPIO PB 24
59C	X_PB23	I/O	NVDD7_12_14	GPIO PB 23
60C	X_USBH2_CLK	I	NVDD7_12_14	USB Host transceiver ULPI clock signal
61C	X_USBH2_DIR	I	NVDD7_12_14	USB Host transceiver ULPI clock signal
62C	GND	-	0	Ground 0 V
63C	X_USBH2_DATA2	I/O	NVDD7_12_14	USB Host transceiver ULPI data signal D2
64C	X_USBH2_DATA4	I/O	NVDD7_12_14	USB Host transceiver ULPI data signal D4
65C	X_USBH2_DATA6	I/O	NVDD7_12_14	USB Host transceiver ULPI data signal D6
66C	NVDD7_12_14	O	NVDD7_12_14	USB Host reference voltage (2.775 V)
67C	GND	-	0	Ground 0 V

68C	X_SD2_D0	I/O	NVDD15	SD/MMC Data line both in 1-bit and 4-bit mode
69C	X_SD2_D1	I/O	NVDD15	SD/MMC Data line or interrupt in 4-bit mode Interrupt in 1-bit mode
70C	X_SD2_D2	I/O	NVDD15	SD/MMC Data line or interrupt in 4-bit mode Interrupt in 1-bit mode
71C	X_SD2_D3	I/O	NVDD15	SD/MMC Card detect in power up, Data line in 4-bit mode, not used in 1-bit mode
72C	GND	-	0	Ground 0 V
73C	X_UART2_RTS	I	NVDD6_8_9_10	Request to send UART 2
74C	X_UART2_CTS	O	NVDD6_8_9_10	Clear to send UART 2
75C	not connected	-	-	Pin left unconnected
76C	not connected	-	-	Pin left unconnected
77C	GND	-	0	Ground 0 V
78C	X_UART3_TXD	O	NVDD6_8_9_10	Serial transmit signal UART 3
79C	X_UART3_CTS	O	NVDD6_8_9_10	Clear to send UART 3
80C	not connected	-	-	Pin left unconnected
81C	not connected	-	-	Pin left unconnected
82C	GND	-	0	Ground 0 V
83C	X_I2C2_SCL	I/O	NVDD7_12_14	I²C 2 Serial Clock
84C	X_I2C2_SDA	I/O	NVDD7_12_14	I²C 2 Serial Data
85C	X_I2C_DATA	I/O	NVDD7_12_14	I²C 1 Serial Data
86C	X_CSPI1_SCLK	I/O	NVDD6_8_9_10	SPI 1 clock
87C	GND	-	0	Ground 0 V
88C	X_CSPI1_SS1	I/O	NVDD6_8_9_10	SPI 1 Chip select 1
89C	X_CSPI3_MOSI	I/O	NVDD6_8_9_10	SPI 3 Master data out; slave data in Used as GPIO PE22
90C	X_#CSPI1_RDY	I/O	NVDD6_8_9_10	SPI 1 SPI data ready in Master mode
91C	X_PE19	I/O	NVDD6_8_9_10	GPIO PE19
92C	GND	-	0	Ground 0 V
93C	X_GPT5_TOUT	O	NVDD6_8_9_10	General purpose timer 5 output
94C	X_GPT5_TIN	I	NVDD6_8_9_10	General purpose timer 5 input
95C	X_GPT4_TOUT	O	NVDD6_8_9_10	General purpose timer 4 output
96C	X_GPT4_TIN	I	NVDD6_8_9_10	General purpose timer 4 input
97C	GND	-	0	Ground 0 V
98C	X_BOOT1	I/O	AVDD	Boot-Mode 1
99C	X_BOOT0	I/O	AVDD	Boot-Mode 0
100C	AVDD	O	AVDD	BOOT (0-3) reference voltage (1.8 V)

PIN ROW X1D				
PIN #	SIGNAL	I/O	SL	DESCRIPTION
1D	VIN	-	Power	Main Power Input (3.3 V – 4.65 V)
2D	VIN	-	Power	Main Power Input (3.3 V – 4.65 V)
3D	GND	-	0	Ground 0 V
4D	X_#RESET_OUT	O	NVDD1_2_3_4_5	Reset Output from the i.MX27
5D	X_#RESET	O	NVDD1_2_3_4_5	Reset Input/Output
6D	X_#RESET	O	NVDD1_2_3_4_5	Reset Input/Output
7D	X_IMX27_FUSE	I	3.0 V	Fusebox write (program) Supply Voltage (3.0 V)
8D	X_TOUT	O	3.3 V	Open-Drain Thermostat Output of U10 (DS75)
9D	GND	-	0	Ground 0 V
10D	X_CHARGER_INPUT_3-20V	I	EHV (max. 20 V)	Charger Input
11D	X_CHARGER_INPUT_3-20V	I	EHV	Charger Input
12D	X_CHARGER_INPUT_3-20V	I	EHV	Charger Input
13D	X_CHARGER_INPUT_3-20V	I	EHV	Charger Input
14D	GND	-	0	Ground 0 V
15D	X_CHRGISNSN	I	VATLAS	Charge current sensing point 2
16D	X_BFET	O	EHV	1. Driver output for dual path regulated BP FET 2. Driver output for separate USB charger path FET
17D	X_CHRGCTL	O	EHV	Driver output for charger path FET's
18D	X_PWRRDY	O	LV	Power ready signal after DVS and power gate transition
19D	GND	-	0	Ground 0 V
20D	X_GPO1	O	LV	General purpose output 1
21D	X_GPO2	O	LV	General purpose output 2
22D	X_UART_RXD_RS232	O	RS232/ NVDD6_8_9_10	Serial Data receive line UART X
23D	X_UART_TXD_RS232	O	RS232/ NVDD6_8_9_10	Serial Data transmit line UART X
24D	GND	-	0	Ground 0 V
25D	X_UART_RTS_RS232	O	RS232/ NVDD6_8_9_10	Request to send UART X
26D	X_UART_CTS_RS232	O	RS232/ NVDD6_8_9_10	Clear to send UART X
27D	X_GPO3	O	LV	General purpose output 3
28D	X_GPO4	O	LV	General purpose output 4

29D	GND	-	0	Ground 0 V
30D	X_TSX1	O	LV	ADC generic input channel 12 or touchscreen input X1, group 2
31D	X_TSX2	O	LV	ADC generic input channel 13 or touchscreen input X2, group 2
32D	X_TSY1	O	LV	ADC generic input channel 14 or touchscreen input Y1, group 2
33D	X_TSY2	O	LV	ADC generic input channel 15 or touchscreen input Y2, group 2
34D	GND	-	0	Ground 0 V
35D	X_ETH_RX+	I/O	3.3 V	Receive positive input (normal) Transmit positive output (reversed)
36D	X_ETH_TX+	I/O	3.3 V	Transmit positive output (normal) Receive positive input (reversed)
37D	X_#ON3	I	LV	Power on/off button connection 3
38D	X_TCK	I	NVDD6_8_9_10	JTAG clock
39D	GND	-	0	Ground 0 V
40D	X_TDI	I	NVDD6_8_9_10	JTAG Data In
41D	X_TDO	O	NVDD6_8_9_10	JTAG Data Out
42D	X_TMS	I	NVDD6_8_9_10	JTAG Mode select
43D	X_JTAG_CTRL	I	NVDD1_2_3_4_5	JTAG Mode
44D	GND	-	0	Ground 0 V
45D	X_ADIN8	I	LV	Analog Input Channel 8
46D	X_ADIN9	I	LV	Analog Input Channel 9
47D	X_ADIN10	I	LV	Analog Input Channel 10
48D	X_ADIN11	I	LV	Analog Input Channel 11
49D	GND	-	0	Ground 0 V
50D	X_USBH1_RXDM	I	NVDD7_12_14	USB Host1 Receive Data Minus signal
51D	X_USBH1_RXDP	I	NVDD7_12_14	USB Host1 Receive Data Plus signal
52D	X_USBH1_TXDM	O	NVDD7_12_14	USB Host1 Transmit Data Minus signal
53D	X_USBH1_TXDP	O	NVDD7_12_14	USB Host1 Transmit Data Plus signal
54D	GND	-	0	Ground 0 V
55D	X_USBH1_RCV	O	NVDD7_12_14	USB Host1 RCV signal
56D	X_USB_HS_/PSW	O	5 V	USB-OTG Power switch output open drain
57D	X_USB_HS_FAULT	I	5 V	USB-OTG over current input signal
58D	X_USBH1_SUSP	I	NVDD7_12_14	USB Host1 Suspend signal
59D	GND	-	0	Ground 0 V
60D	X_USBH2_STP	O	NVDD7_12_14	USB Host transceiver ULPI stop signal
61D	X_USBH2_NXT	I	NVDD7_12_14	USB Host transceiver ULPI next signal
62D	X_USBH2_DATA0	I/O	NVDD7_12_14	USB Host transceiver ULPI data signal D0
63D	X_USBH2_DATA1	I/O	NVDD7_12_14	USB Host transceiver ULPI data signal D1
64D	GND	-	0	Ground 0 V
65D	X_USBH2_DATA3	I/O	NVDD7_12_14	USB Host transceiver ULPI data signal D3

66D	X_USBH2_DATA5	I/O	NVDD7_12_14	USB Host transceiver ULPI data signal D5
67D	X_USBH2_DATA7	I/O	NVDD7_12_14	USB Host transceiver ULPI data signal D7
68D	X_SD2_CMD	I/O	NVDD15	SD/MMC line connect to card
69D	GND	-	0	Ground 0 V
70D	X_SD2_CLK	O	NVDD15	SD/MMC Clock for MMC/SD/SDIO
71D	NVDD15	O	NVDD15	SD2 reference voltage (2.775 V)
72D	X_UART2_TXD	O	NVDD6_8_9_10	Serial data transmit signal UART 2
73D	X_UART2_RXD	I	NVDD6_8_9_10	Serial data receive signal UART 2
74D	GND	-	0	Ground 0 V
75D	X_#USBH1_OE	O	NVDD7_12_14	USB Host1 Output Enable signal
76D	X_USBH1_FS	O	NVDD7_12_14	USB Host1 Full Speed output signal
77D	X_UART3_RXD	I	NVDD6_8_9_10	Serial data receive signal UART 3
78D	X_UART3_RTS	I	NVDD6_8_9_10	Request to send UART 3
79D	GND	-	0	Ground 0 V
80D	not connected	-	-	Pin left unconnected
81D	X_PRIINT	O	NVDD6_8_9_10	Primary Interrupt output of PMIC U14
82D	X_#IRQRTC	O	NVDD6_8_9_10	Interrupt Output from RTC U11 (RTC-8564JE)
83D	NVDD6_8_9_10	O	NVDD6_8_9_10	I2C reference voltage (2.775 V)
84D	GND	-	0	Ground 0 V
85D	X_I2C_CLK	I/O	NVDD6_8_9_10	I²C 1 Serial Clock
86D	X_CSPI1_MOSI	I/O	NVDD6_8_9_10	SPI 1 Master data out; slave data in
87D	X_CSPI1_MISO	I/O	NVDD6_8_9_10	SPI 1 Master data in; slave data out
88D	X_CSPI3_SCLK		NVDD6_8_9_10	SPI 3 clock Used as GPIO PE23
89D	GND	-	0	Ground 0 V
90D	X_CSPI3_MISO		NVDD6_8_9_10	SPI 3 Master data in; slave data out Used as GPIO PE18
91D	X_OWIRE	I/O	NVDD6_8_9_10	1-Wire bus
92D	NVDD6_8_9_10	O	NVDD6_8_9_10	1-Wire reference voltage (2.775 V)
93D	X_PE20	I/O	NVDD6_8_9_10	GPIO PE20
94D	GND	-	0	Ground 0 V
95D	X_CSPI3_SS		NVDD6_8_9_10	SPI 3 Chip select Used as GPIO PE21
96D	X_TIN	I	NVDD6_8_9_10	Timer Input Clock-The signal on this input is applied to GPT 1–3 simultaneously
97D	X_TOUT1	O	NVDD6_8_9_10	Timer Output signal from General Purpose Timer1 (GPT1)
98D	X_BOOT2	I/O	AVDD	Boot-Mode 2
99D	GND	-	0	Ground 0 V
100D	X_PWMO	O	NVDD6_8_9_10	Pulse Width Modulator Output

3 Jumpers

For configuration purposes, the phyCORE-i.MX27 has 24 solder jumpers, some of which have been installed prior to delivery. *Figure 5* illustrates the numbering of the solder jumper pads, while *Figure 6* and *Figure 7* indicate the location of the solder jumpers on the board. 8 solder jumpers are located on the top side of the module (opposite side of connectors) and 16 solder jumpers are located on the bottom side of the module (connector side). *Table 2* below provides a functional summary of the solder jumpers, their default positions, and possible alternative positions and functions. A detailed description of each solder jumper can be found in the applicable section listed in the table.

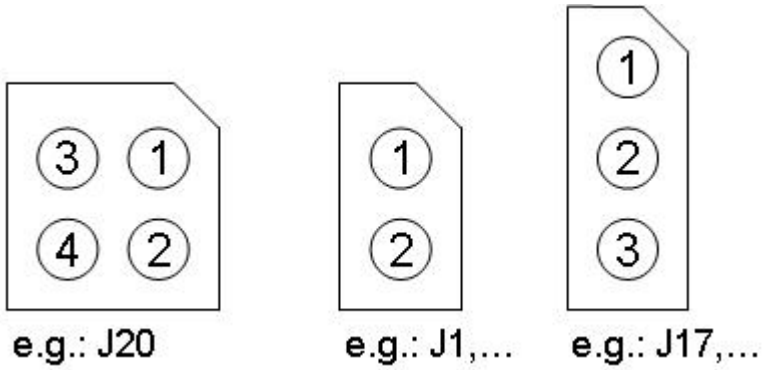

Figure 5: Typical jumper pad numbering scheme

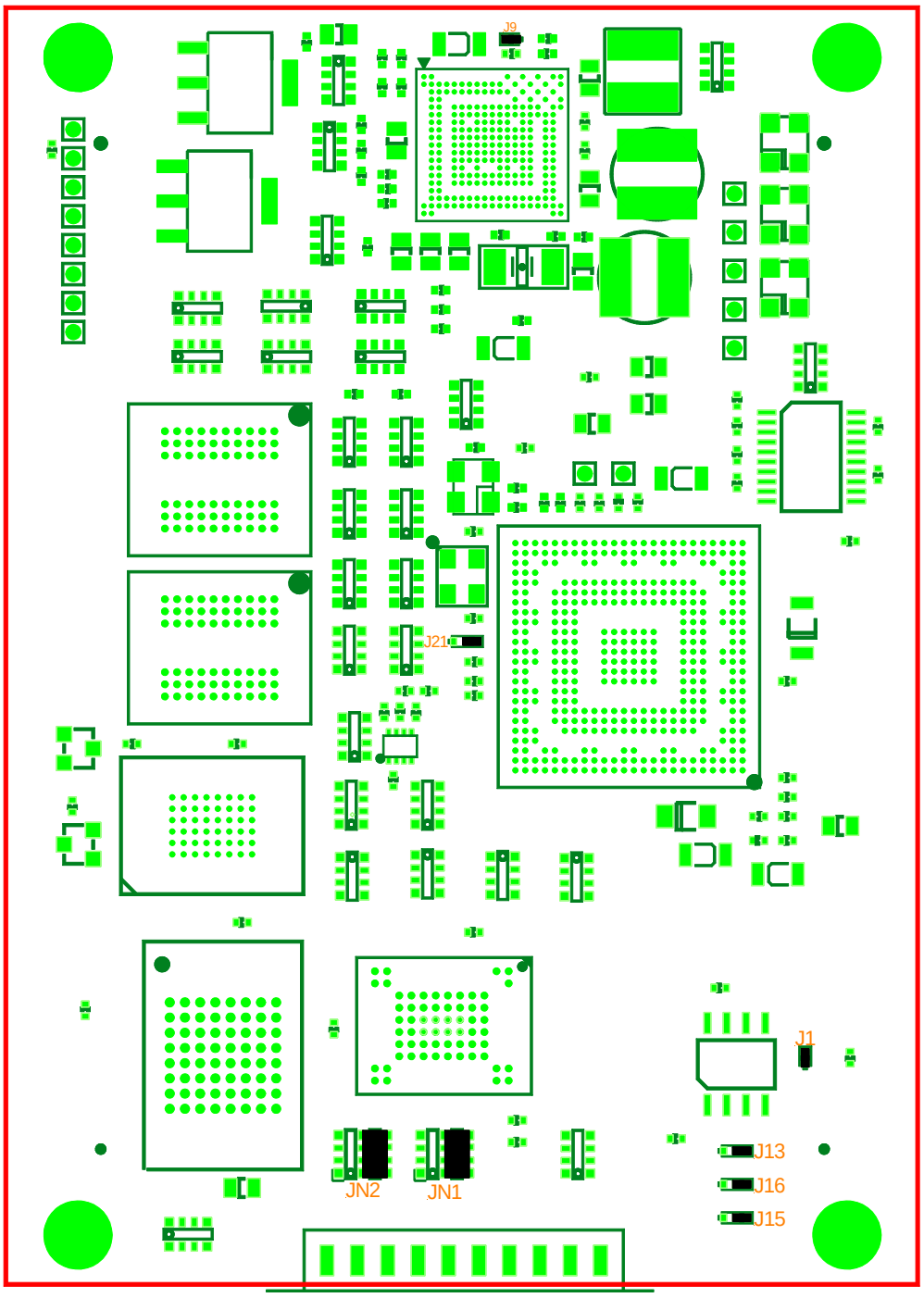

Figure 6: Jumper locations (top view)

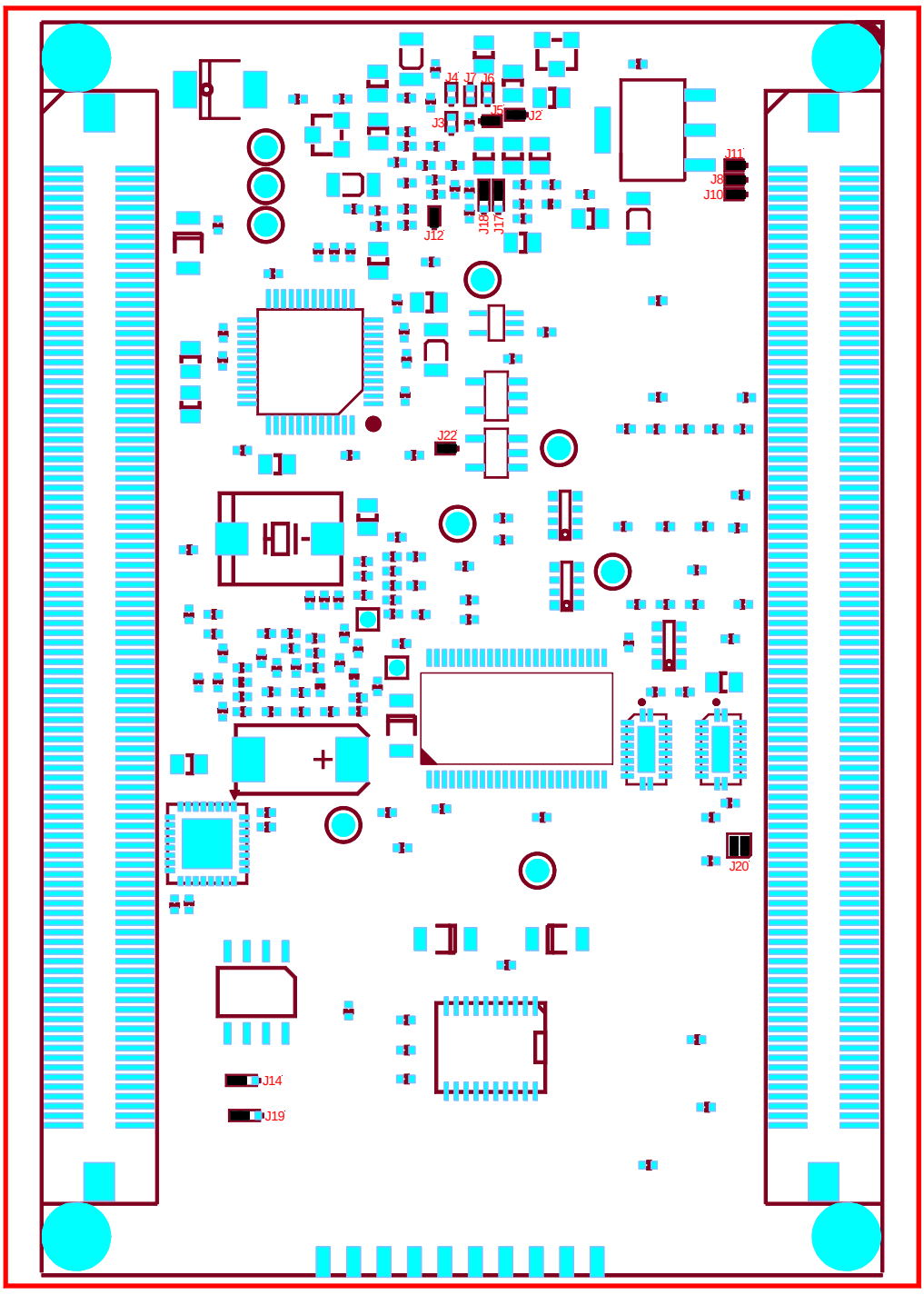

Figure 7: Jumper locations (bottom view)

The jumpers (J = solder jumper) have the following functions:

Table 2: Jumper settings

	DEFAULT SETTING		ALTERNATIVE SETTING		SEE SECTION
J1	closed	EEPROM U12 is not write protected	open	EEPROM U12 is write protected	7.5.2
J2	closed	Power up Mode select (PUMS1) is connected to GND (low)	open	Power up Mode select (PUMS1) is floating	**Fehler! Verweisquelle konnte nicht gefunden werden.**
J3	open	Power up Mode select (PUMS1) is floating	closed	Power up Mode select (PUMS1) is connected to VATLAS (high)	
J4	open	Power up Mode select (PUMS1) is floating	closed	Power up Mode select (PUMS2) is connected to VATLAS (high)	
J5	closed	Power up Mode select (PUMS2) is connected to GND (low)	open	Power up Mode select (PUMS2) is floating	
J6	open	Power up Mode select (PUMS3) is floating	closed	Power up Mode select (PUMS3) is connected to VATLAS (high)	
J7	open	Power up Mode select (PUMS3) is floating	closed	Power up Mode select (PUMS3) is connected to GND (low)	
J9	closed	CHRGMOD1 is connected to VATLAS (high)	open	CHRGMOD1 is floating (high-z)	

J10	closed	Signal X_PWGT1EN is connected to the Molex-Connector (X1 – Pin 3B)	open	Signal X_PWGT1EN is not connected to the Molex-Connector (X1 – Pin 3B)	
J12	closed	Signal X_PRIINT is connected to X_PB23 (GPIO)	open	Signal X_PRIINT is not connected to X_PB23 (GPIO)	
J13	2 + 3	EEPROM A1 is connected to NVDD7_12_14 (high)	1 + 2	EEPROM A1 is connected to GND (low)	7.5
J14	2 + 3	DS75 A1 is connected to NVDD7_12_14 (high)	1 + 2	DS75 A1 is connected to GND (low)	
J15	2 + 3	EEPROM A2 is connected to GND (low)	1 + 2	EEPROM A2 is connected to NVDD7_12_14 (high)	7.5
J16	2 + 3	EEPROM A0 is connected to GND (low)	1 + 2	EEPROM A0 is connected to NVDD7_12_14 (high)	7.5
J17	2 + 3	RXOUTR is connected to X_RXOUTR_LSPM (X1 – Pin 24C)	1 + 2	LSPM is connected to X_RXOUTR_LSPM (X1 – Pin 24C)	
J18	2 + 3	RXOUTL is connected to X_RXOUTL_LSPP (X1 – Pin 23C)	1 + 2	LSPP is connected to X_RXOUTL_LSPP (X1 – Pin 23C)	
J19	2 + 3	DS75 A2 is connected to GND (low)	1 + 2	DS75 A2 is connected to NVDD7_12_14 (high)	
J20	1 + 3 2 + 4	#SRAM_BHE is connected to X_#PC_IORD/#EB1 X_#PC_REG/#EB0 is connected to #SRAM_BLE	1 + 2 3 + 4	#SRAM_BHE is connected to X_#PC_REG/#EB0 X_#PC_IORD/#EB1 is connected to #SRAM_BLE	
J21	2 + 3	If main clock is generated by crystal	1 + 2	If main clock is generated by oscillator	
J22	closed	If Sofware-Reset (GPIO) is used to reset ETH_PHY	open	If no Sofware-Reset (GPIO) is used to reset ETH_PHY	
JN1	2 + 3	If 8-bit mode is used for NAND-Flash	1 + 2	If 16-bit mode is used for NAND-Flash	7.4.1
JN2	2 + 3	If 8-bit mode is used for NAND-Flash	1 + 2	If 16-bit mode is used for NAND-Flash	7.4.1

4 Power Requirements

The phyCORE-i.MX27 normally operates off two different voltage supplies denoted as **VIN** and **VCC_3V3**. The MC13783 primary on-board voltage regulator operates off VIN and generates all on-board supply voltages except 3.3 V. The VCC_3V3 input supplies this required voltage.

Because of its wide input voltage range VIN is ideally suited for a battery. VCC_3V3, however, has a very narrow input voltage range and must not be connected to a battery. A well regulated supply should be used for VCC_3V3.

The phyCORE-i.MX Carrier Board generates VCC_3V3 from VIN with a 3.3 V voltage regulator on the Carrier Board. VIN is sourced from either the wall socket input, or a battery. The Carrier Board also controls charging the battery when the wall socket is used. *You should refer to this example circuitry when designing your own Carrier Board.*

If your system does not require a battery then you can connect VIN and VCC_3V3 together and supply both inputs with a 3.3 V input voltage. This will simplify the design and reduce the component count. In this case make sure that the X_CHARGER_INPUT_3-20V is connected to a power supply >4.4V. You also have to design a 0.02R resistor between X_POWER_BATT and X_BATTISNS and a 22µF capacitor at X_POWER_BATT. Put both components as close as possible to the module connector. (*see Figure 8 and Table 3*)

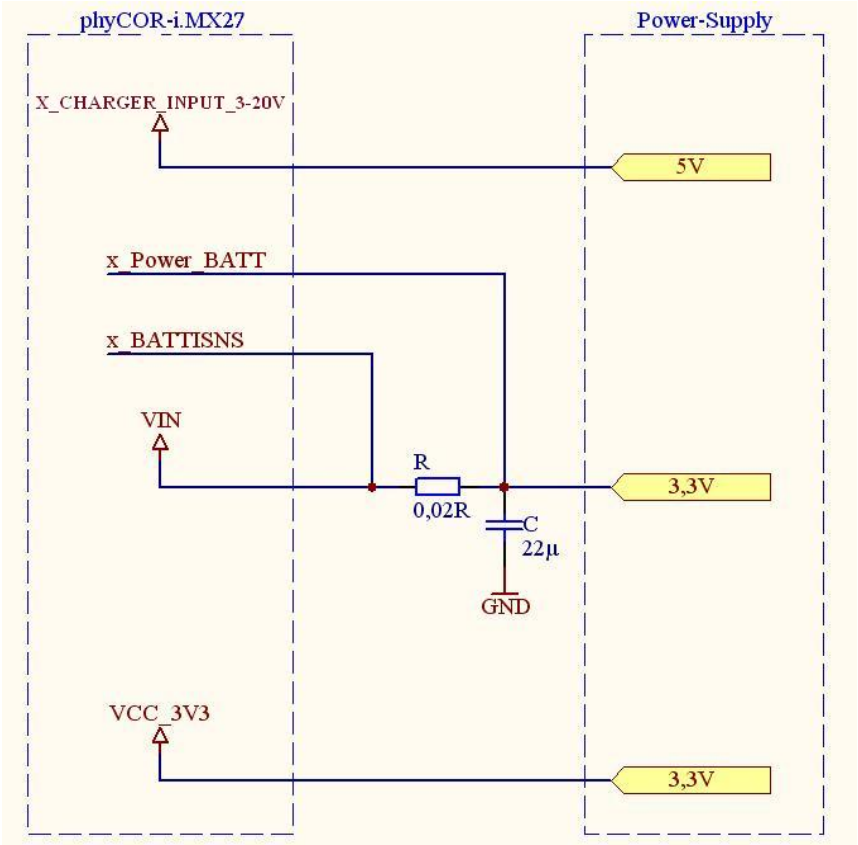

Figure 8: minimum circuit

Table 3: Power supply for the minimum circuit

power supply	min.	typ.	max.
5 V (x_Charger_Input)	4.4 V	5 V	20 V
3.3 V (VIN)	3.25 V	3.3 V	4.5 V
3.3 V (VCC_3V3)	3.15 V	3.3 V	3.45 V

The input voltage range of VIN is from 3.1 V.. 4.65 V, with a nominal current allowance of at least 3 A. VCC_3V3 should be in a range of 3.3 V ± 0.15 V (±0.05 V if VCC_3V3 is connected to VIN) with a nominal current allowance of at least 1.5 A.

See *Table 1* from *section 2* above for applicable VIN / VCC_3V3 power pins on the phyCORE-connector.

Caution!
Connect all VIN and VCC_3V3 input pins to your power supplies.

As a general design rule we recommend connecting all GND pins which are neighboring signals being used in the application circuitry.

The i.MX27 CPU is supplied by a lot of different power domains. Some of them are connected together. The startup voltage levels are selected by the Power up Mode selection inputs (PUMS1..3) of the PMIC device MC13783. With the default settings of the input pins PUMS1..3 the voltages are the following:

Table 4: i.MX27 default power input voltages

MC13783 Power Output	Power-Domain	Startup Voltage-Level
SW1	QVDD	1.2 V
SW2	NVDD1_2_3_4_5	1.8 V
SW3	SW3	5 V
VAUDIO	internally used by MC13783	2.775 V
VIOLO	AVDD	1.8 V
VIOHI	OSC26VDD	2.775 V
VGEN	PLL_VDD	1.5 V
VCAM	NVDD11	2.8 V
VRF1	NVDD7_12_14	2.775 V
VRF2	NVDD6_8_9_10	2.775 V
VMMC1	NVDD15	2.775 V

In general you should not need to adjust the Power up Mode settings. The configuration has been optimized for the phyCORE-i.MX27 together with the phyCORE-i.MX Carrier Board.

5 Real Time Clock U11 / SRAM U19 Backup-Voltage

In case of a power fail or a user off event the backup-voltage AVDD_BKUP provides power to the I²C Real Time Clock U11 (RTC8564JE) and the low power SRAM U19. In this cases a backup coincell will supply the memory and the RTC via AVDD_BKUP (VBKUP2 of MC13783).
To set the output voltage and the different modes of VBKUP2, U14 (MC13783) must be programmed over SPI.

Table 5: VBKUP2 Voltage Settings

VBKUP2[1:0]	00	output = 1.0 V
	01	output = 1.2 V
	10	output = 1.5 V
	11	output = 1.8 V

There are three bits which must be set to low/high for the different modes of VBKUP2:

VBKUP2EN: Enables VBKUP2 in startup modes, on and user off wait modes
VBKUP2AUTOMH: Enables VBKUP2 in memory hold modes
VBKUP2AUTOUO: Enables VBKUP2 in user off modes

For further information refer to the MC13783 manual chapter 5.2. Operating Modes.

6 System Configuration

Although most features of the Freescale phyCORE-i.MX27 microcontroller are configured and/or programmed during the initialization routine, other features, which impact program execution, must be configured prior to initialization via pin termination.

6.1 System Startup Configuration

During the reset cycle the i.MX27 processor reads the state of selected controller signals to determine the basic system configuration. The configuration circuitries (pull-up or pull-down resistors) are located on the phyCORE module. They are already set, so no further settings are necessary.

6.1.1 Power-Up-Mode-Select (PUMS)

The Power-Management-IC (M13783) has three Power-Up-Mode-Selecets. PUMS1 and PUMS2 determine the initial setup for the voltage level of the switchers and regulators and if they get enabled or not. With PUMS3 three different power up sequences are selectable.

The three states of the PUMS settings are:

- Pull-up (connected to VATLAS)
- Pull-down (connected to GND)
- Open (no jumper populated/left open)

For detailed information about PUMS and the power up sequence, refer to the MC13783 IC User's Guide, chapter 5.3 Power up.

The i.MX27 module (PCM-038) comes with a standard Power-Up-Mode-Select (*see table below*).

Table 6: Default PUMS for i.MX27 module

PUMS1	**GND**
PUMS2	**GND**
PUMS3	**Open**

Note:
The i.MX27 controller has a defined power up sequence*. Refer to the i.MX27 Data Sheet, chapter 3.3 Power-Up sequence.*

6.1.2 Boot Mode Select

The i.MX27 controller has different boot modes, which can be selected. The system boot mode of the processor is determined by the configuration of the four external input pins, BOOT[3:0].

Table 7: Boot Modes of i.MX27 module

Boot Mode Selection	Boot Mode/Device
0000	Bootstrap from UART/USB
0001	Reserved
0010	8-bit NAND Flash (2 Kbyte per page)
0011	16-bit Nand Flash (2 Kbyte per page)
0100	16-bit Nand Flash (512 bytes per page)
0101	16-bit CS0 (NOR-Flash)
0110	32-bit CS0
0111	8-bit Nand Flash (512 bytes per page)
1xxx	Reserved

The phyCORE-i.MX27 module comes with a standard boot configuration of **‘0101’**, so the system will boot from the 16-bit NOR-Flash at CS0.

7 System Memory

The phyCORE-i.MX27 provides different types of on-board memory:

- LP-DDR-SDRAM: 128 MByte (up to 256 MByte)
- SRAM: 512KByte (up to 2 MByte)
- NAND Flash: 64 MByte (up to 1 GByte)
- NOR Flash: 32MByte (up to 64 MByte)
- I²C-EEPROM: 32 KB (up to 32 KByte)

It should be noted that the LP-DDR-SDRAM has a dedicated memory bus to the i.MX27 microcontroller. The LP-DDR-SDRAM bus is therefore not made available at the phyCORE-connector X1.

7.1 Memory Model

The i.MX27 memory map is summarized in *Table 8* below. *For a detailed view of the memory map please consult the Freescale i.MX27 User's Manual*.

Table 8: i.MX27 memory map

ADDRESS	CHIP-SELECT	FUNCTION
0xA000 0000 – 0xAFFF FFFF	/CSD0 (/CS2)	LP-DDR-SDRAM Bank 0 (U3, U4)
0xB000 0000 – 0xBFFF FFFF	/CSD1 (/CS3)	not used on phyCORE-i.MX27
0xC000 0000 – 0xC7FF FFFF	/CS0	NOR-Flash (U17)
0xC800 0000 – 0xCFFF FFFF	/CS1	SRAM (U19)
0xD400 0000 – 0xD5FF FFFF	/CS4	not used on phyCORE-i.MX27
0xD600 00000 – 0xD7FF FFFF	/CS5	not used on phyCORE-i.MX27 (SJA1000 on Carrier Board)

7.2 LP-DDR-SDRAM (U3-U4)

The phyCORE-i.MX27 has one bank of LP-DDR-SDRAMs on the i.MX27.

The RAM bank is comprised of two 16-bit wide DDR-SDRAM chips, configured for 32-bit access, and operating at 133 MHz. In lower density configurations, U3 and U4 populate the module and are accessed via SDRAM memory bank 0 using chip select signal /CSD0 starting at 0xA000 0000.
Actually the RAM bank 1 is not populated and the /CSD1 chip select line is freed and can be used as /CS3.

Typically the LP-DDR-SDRAM initialization is performed by a boot loader or operating system following a power-on reset and must not be changed at a later point by any application code. When writing custom code independent of an operating system or boot loader, SDRAM must be initialized by accessing the appropriate SDRAM configuration registers on the i.MX27 controller. *Refer to the i.MX27 User Manual for accessing and configuring these registers.*

7.3 NOR-Flash (U17)

The phyCORE-i.MX27 can be populated with an Intel Strata Flash at U17. This NOR-Flash is connected to /CS0 which is located at memory address 0xC000 0000. The entire Flash can be write protected by pulling the x_/FL_WP signal, located at the phyCORE-connector X1 on pin 58B, low.

The following NOR-Flash devices can be used on the phyCORE-i.MX27:

Table 9: Compatible NOR Flash devices

MANUFACTURER	NOR FLASH P/N	DENSITY (MBYTE)
Intel	PC28F640P30	8
Intel	PC28F128P30	16
Intel	PC28F256P30	32

7.4 NAND Flash Memory (U16)

Use of Flash as non-volatile memory on the phyCORE-i.MX27 provides an easily reprogrammable means of code storage. The following Flash devices can be used on the phyCORE-i.MX27:

Table 10: Compatible NAND Flash devices

MANUFACTURER	NAND FLASH P/N	DENSITY (MBYTE)
ST Microelectronics	NAND256R3A2BZA6	32
ST Microelectronics	NAND512R3A2BZA6	64

Additionally, any parts that are footprint (VFBGA) and functionally compatible with the NAND Flash devices listed above may also be used with the phyCORE-i.MX27.

These Flash devices are programmable with 1.8 V. No dedicated programming voltage is required.

As of the printing of this manual these NAND Flash devices generally have a life expectancy of at least 100,000 erase/program cycles and a data retention rate of 10 years.

7.4.1 8/16-Bit NAND Flash Usage (JN1,JN2,RN31,RN32)

The i.MX27 is capable of using 8-Bit and 16-Bit NAND Flash devices. To select between 8- and 16-bit NAND Flash, the jumpers/resistor networks must be populated as follows:

Table 11: JN1/2,RN31/32 NAND Flash bit width selection[1]

NAND-FLASH BIT WIDTH	JN1/2	RN31/32
8-bit	**2-3/5-6/8-9/11-12**	**not populated**
16-bit	1-2/4-5/7-8/10-11	populated

7.5 I²C EEPROM (U12)

The phyCORE-i.MX27 is populated with a ST 24W32C[2] non-volatile 32 KByte EEPROM (U12) with an I²C interface to store configuration data or other general purpose data. This device is accessed through I²C port 2 on the i.MX27. The serial clock signal and serial data signal for I²C port 2 are made available at the phyCORE-connector as x_I2C2_SDA on X1 pin 84C and x_I2C2_SCL on X1 pin 83C.

Three solder jumpers are provided to set the lower address bits: J13, J15, and J16. *Refer to section 7.5.1 for details on setting these jumpers.*

Write protection to the device is accomplished via jumper J1. By default this jumper is closed, allowing write access to the EEPROM. Removing this jumper will cause the EEPROM to enter write protect mode, thereby disabling write access to the device. *Refer to section 7.5.2 for further details on setting this jumper.*

1 Default settings are in **bold blue** text

2: *See the manufacturer's data sheet for interfacing and operation.*

7.5.1 Setting the EEPROM Lower Address Bits (J13, J15, J16)

The 32 KB I²C EEPROM populating U12 on the phyCORE-module has the capability of configuring the lower address bits A0, A1, and A2. The four upper address bits of the device are fixed at '1010' (*see ST 24W32C data sheet).* The remaining three lower address bits of the seven bit I²C device address are configurable using jumpers J13, J15 and J16. J16 sets address bit A0, J13 address bit A1, and J15 address bit A2.

Table 12 below shows the resulting seven bit I²C device address for the eight possible jumper configurations.

Table 12: U12 EEPROM I²C address via J13, J15, and J16[1]

U12 I²C Device Address	J15	J13	J16
1010 010	**2 + 3**	**2 + 3**	**2 + 3**
1010 011	2 + 3	2 + 3	1 + 2
1010 000	2 + 3	1 + 2	2 + 3
1010 001	2 + 3	1 + 2	1 + 2
1010 110	1 + 2	2 + 3	2 + 3
1010 111	1 + 2	2 + 3	1 + 2
1010 100	1 + 2	1 + 2	2 + 3
1010 101	1 + 2	1 + 2	1 + 2

7.5.2 EEPROM Write Protection Control (J1)

Jumper J1 controls write access to the EEPROM (U12) device. Closing this jumper allows write access to the device, while opening this jumper enables write protection.

The following configurations are possible:

Table 13: EEPROM write protection states via J1[1]

EEPROM Write Protection State	J1
Write access allowed	**closed**
Write protected	open

1 Defaults are in **bold blue** text

8 Serial Interface

8.1 RS-232 Transceiver (U18)

One high-speed RS-232 transceiver supporting 460kbps data rates populates the phyCORE-i.MX27 at U18. This device converts the signal levels for:

- RXD1/TXD1/RTS1/CTS1 (UART1)

The RS-232 interface enables connection of the module to a COM port on a host-PC. In this instance the RxD line of the transceiver is connected to the TxD line of the COM port; while the TxD line of the transceiver is connected to the RxD line of the COM port. The ground potential of the phyCORE-i.MX27 circuitry needs to be connected to the applicable ground pin on the COM port as well.

The phyCORE-i.MX27 does not convert the remaining two available UARTs (UART2, UART3) provided by the i.MX27 MCU to RS-232 levels. The TTL level signals are made available at the phyCORE-connector X1 (*see Table 1*). External RS-232 transceivers must be supplied by the user if additional UART's require RS-232 levels.

The maximum baud rate of UART1 is limited to 460,800 bps when used with the on-board MAX3380 RS-232 transceiver.

8.1.1 UART1 Routing (RN30)

RN30 is used to route the signals of UART1 serial interface through the RS-232 transceiver or around the RS-232 transceiver when populated. When RN30 is not populated UART1_RXD, UART1_TXD, UART1_RTS and UART1_CTS are routed through the RS-232 transceiver U18 and come out as X_UART1_RXD_RS232, X_UART1_TXD_RS232, x_UART1_RTS_RS232 and x_UART1_CTS_RS232 at the phyCORE-connector pins X1 pin 22D, X1 pin 23D, X1 pin 25D, X1 pin 26D. If U18 does not populate the module, RN30 is populated to route the TTL level signals to these same pins.

The standard phyCORE-i.MX27 module will have U18 populated, thereby routing the RS-232 level signals to the phyCORE-connector. Be sure the phyCORE-i.MX27 configuration you are working with before interfacing these signals outside of the module as incorrect voltage levels will likely cause damage to on-board and off-board components.

The following configurations are possible:

Table 14: RN30 UART1 signal routing[1]

SIGNAL CONFIGURATION	RN30
X_UART1_RXD_RS232, X_UART1_TXD_RS232, X_UART1_ RTS_RS232, X_ UART1_CTS_RS232 as RS-232 level signals at X1 pin 22D, X1 pin 23D, X1 pin 25D and X1 pin 26D	**not populated**
X_UART1_RXD_RS232, X_UART1_TXD_RS232, X_UART1_ RTS_RS232, X_ UART1_CTS_RS232 as TTL level signals at X1 pin 22D, X1 pin 23D, X1 pin 25D and X1 pin 26D	populated

1 Defaults are in **bold blue** text

9 USB-OTG Transceiver (U20)

The phyCORE-i.MX27 comes populated with a NXP ISP1504 USB On-The-Go High-Speed transceiver (U20) supporting high speed, full speed, and low speed data rates. The ISP1504 functions as the transceiver between the i.MX27 Host Controller, Device Controller, and On-The-Go Controller. An external USB Standard-A (for USB host), USB Standard-B (for USB device), or USB mini-AB (for USB OTG) connector is all that is needed to interface the phyCORE-i.MX27 USB OTG functionality. The applicable interface signals (D+/D-/VBUS/ID) can be found in the phyCORE-connector pin-out *Table 1.*

10 Ethernet Controller / Ethernet-Phy (U9)

Connection of the phyCORE-i.MX27 to the world wide web (WWW) or a local area network (LAN) is possible with the internal 10/100 Mbps Fast Ethernet controller. With this Ethernet controller an external transceiver interface and transceiver function are required to complete the interface to the media. Therefor the i.MX27 uses an Ethernet-Phy (U9).

The Ethernet-Phy provides MII/RMII/SMII interfaces to transmit and receive data. In addition the PHY also supports HP Auto-MDIX technology, eliminating the need for the consideration of a direct connect LAN cable, or a cross-over patch cable. It detects the TX and RX pins of the connected device and automatically configures the PHY TX and RX pins accordingly. The Ethernet-Phy also features LinkMD cable diagnostics, which allows detection of common cabling plant problems such as open and short circuits.

The physical memory area for the Fast Ethernet controller is defined in *Table 15.*

Table 15: Fast Ethernet controller memory map

ADDRESS	FUNCTION
0x1002_B + 0x000-1FF	Control/Status Registers
0x1002_B + 0x200-3FF	MIB Block Counters

Connection to an external Ethernet transformer should be done using very short signal traces. The TPI+/TPI- and TPO+/TPO- signals should be routed as 100 Ohm differential pairs. The same applies for the signal lines after the transformer circuit. The carrier board layout should avoid any other signal lines crossing the Ethernet signals.

Caution!
Please note the datasheet of the Ethernet-Phy when creating the Ethernet transformer circuitry.

11 JTAG Interface (U15)

The phyCORE-i.MX27 is equipped with a JTAG interface for downloading program code into the external flash, internal controller RAM or for debugging programs currently executing. The JTAG interface extends out to a 2.0 mm pitch pin header at U15 on the edge of the module PCB. *Figure 9* and *Figure 10* show the position of the debug interface (JTAG connector U15) on the phyCORE-module.

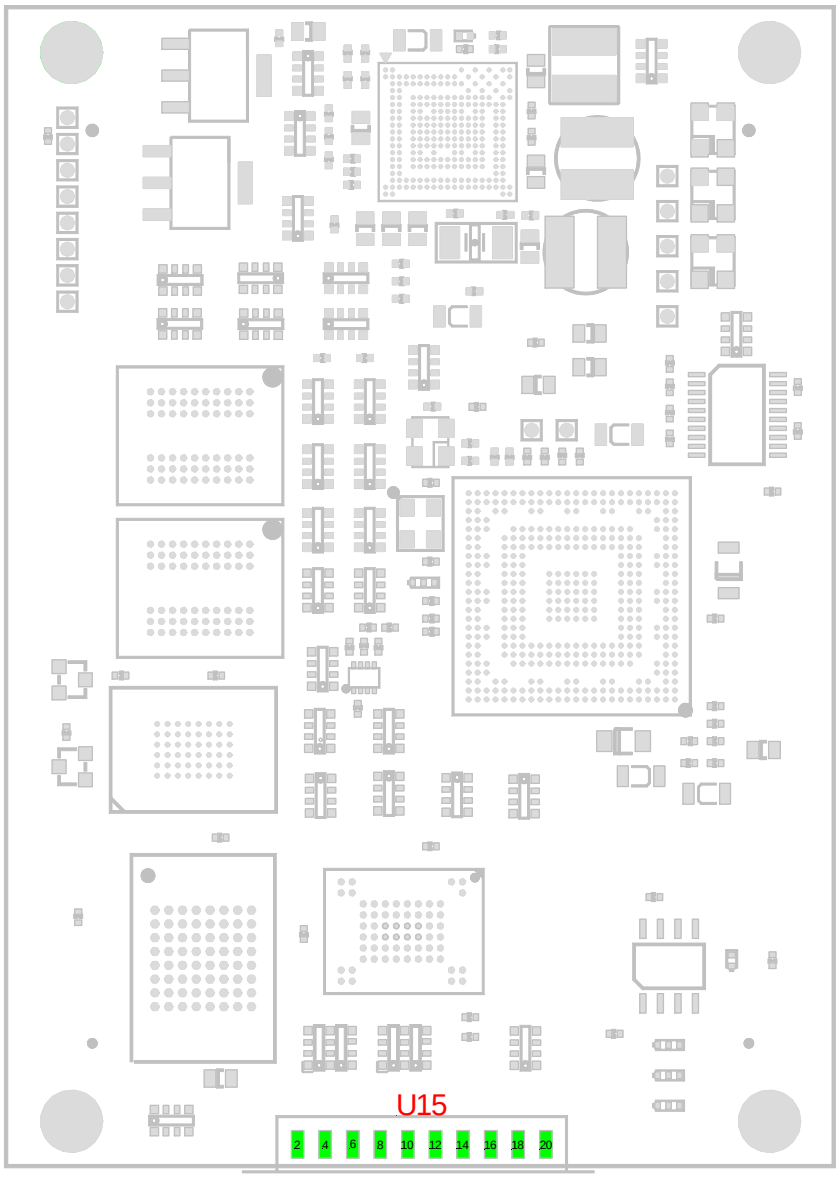

Figure 9: JTAG interface at U15 (top view)

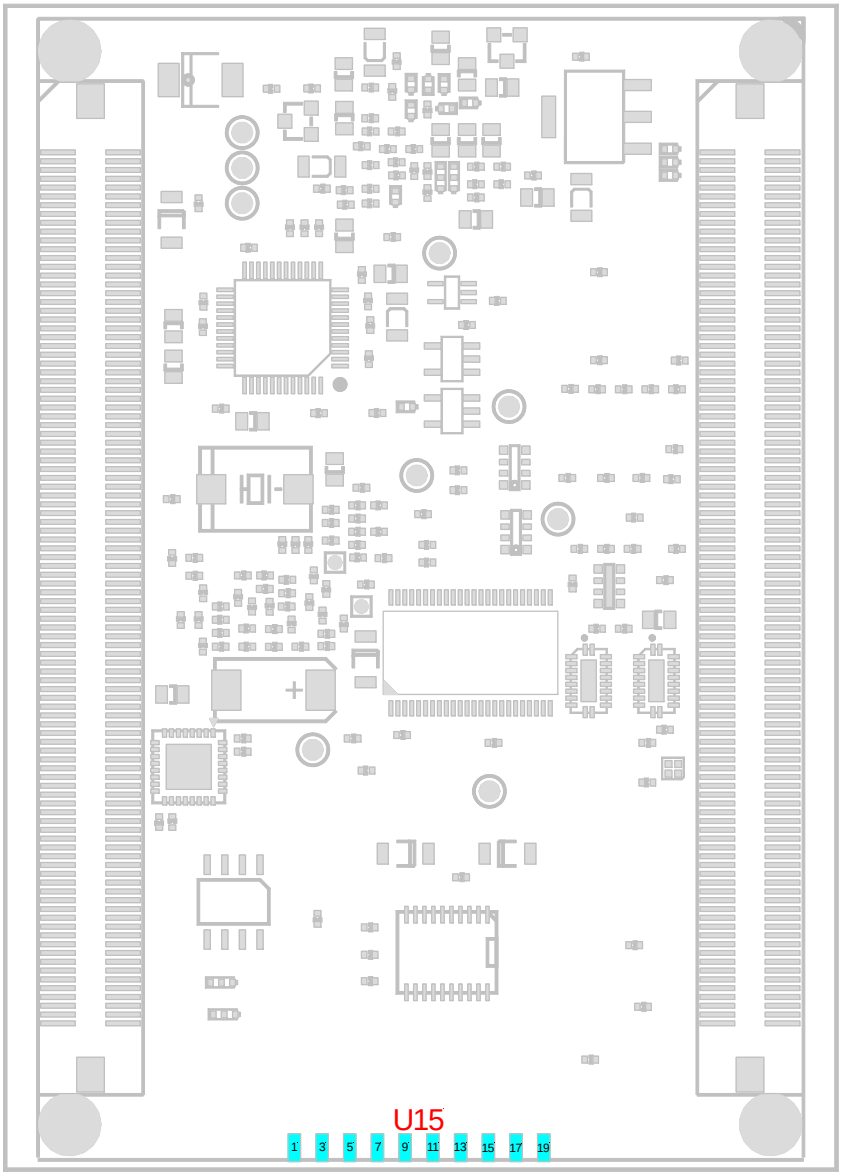

Figure 10: JTAG interface at U15 (bottom view)

Pin 1 of the JTAG connector U15 is on the connector side of the module. Pin 2 of the JTAG connector is on the controller side of the module.

Note:
The JTAG connector U15 only populates phyCORE-i.MX27 modules with order code PCM-038-D. JTAG connector U15 is not populated on phyCORE modules with order code PCM-038. However, all JTAG signals are also accessible at the phyCORE-connector X1 (Molex connectors). We recommend integration of a standard (2.54 mm pitch) pin header connector in the user target circuitry to allow easy program updates via the JTAG interface. See *Table 16 for details on the JTAG signal pin assignment.*

Table 16: JTAG connector U15 signal assignment

SIGNAL	PIN ROW*		SIGNAL
	A	B	
VCC(NVDD6_8_9_10)	2	1	VTref (NVDD6_8_9_10 via 100 Ohm)
GND	4	3	X_#TRST
GND	6	5	X_TDI
GND	8	7	X_TMS
GND	10	9	X_TCK
GND	12	11	RTCK (10k Ohm pulldown)
GND	14	13	X_TDO
GND	16	15	X_#RESET
GND	18	17	Not connected
GND	20	19	J_DBGACK (10k Ohm pulldown)

*Note:
Row A is on the controller side of the module and row B is connector side of the module

PHYTEC offers a JTAG-Emulator adapter (order code JA-002) for connecting the phyCORE-i.MX27 to a standard emulator. The JTAG-Emulator adapter extends the signals of the module's JTAG connector to a standard ARM connector with 2.54 mm pin pitch. The JA-002 therefor functions as an adapter for connecting the module's non-ARM-compatible JTAG connector U15 to standard Emulator connectors.

12 Technical Specifications

The physical dimensions of the phyCORE-i.MX27 are represented in *Figure 11.* The module's profile is approximately ***8.5 mm*** thick, with a maximum component height of ***4.0 mm*** on the bottom (connector) side of the PCB and approximately ***3.1 mm*** on the top (microcontroller) side. The board itself is approximately ***1.4 mm*** thick.

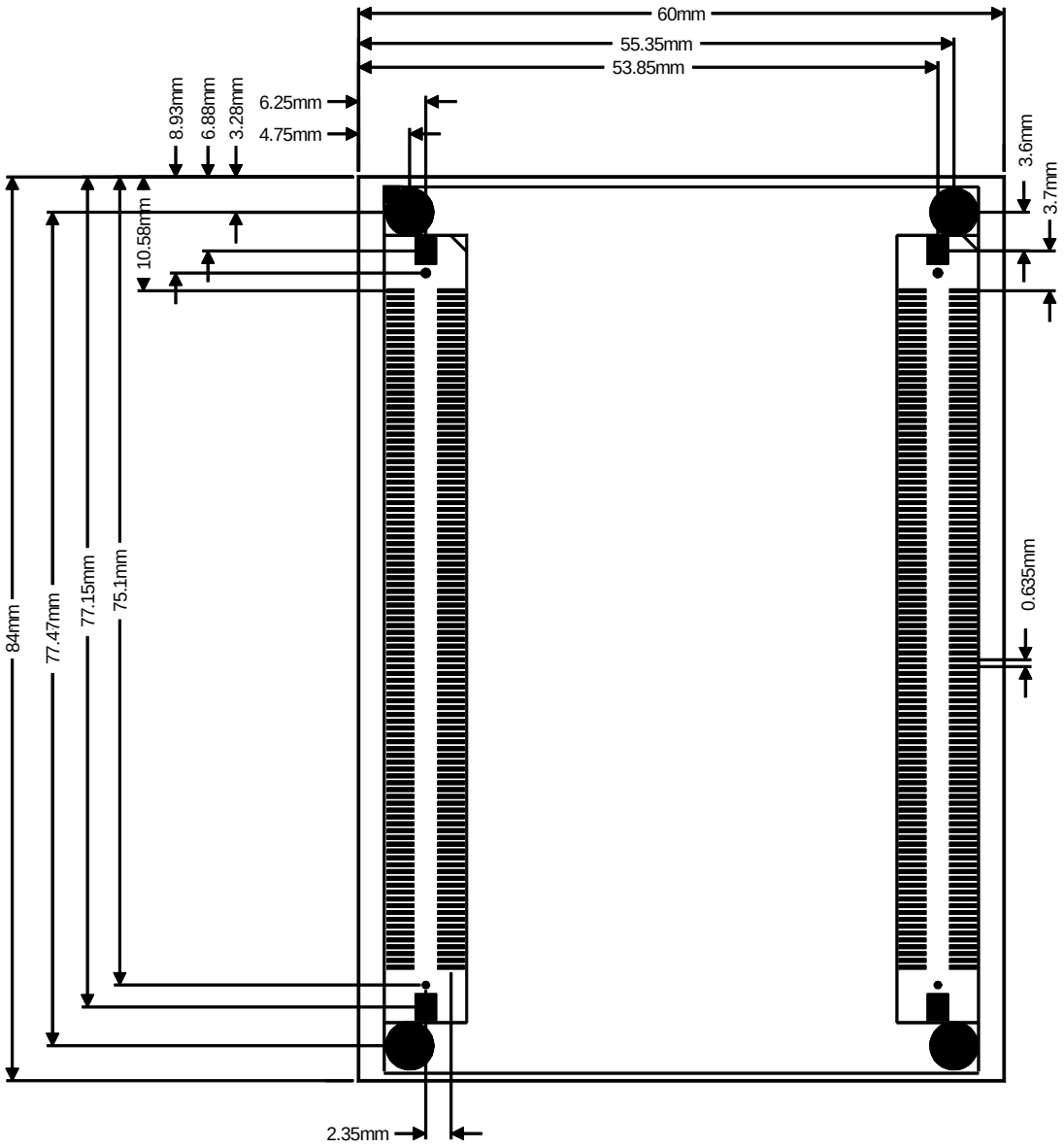

Figure 11: Physical dimensions

Additional specifications:

• *Dimensions:*	*60 mm x 84 mm*
• *Weight:*	*approximately 35 g with all optional components mounted on the circuit board*
• *Storage temperature:*	*-20°C to +125°C*
• *Operating temperature:*	*0°C to +70°C (standard)* *-20°C to +85°C (optional)*
• *Humidity:*	*95 % r.F. not condensed*
• *Operating voltage:*	*VIN 3.1 V to 4.6 V*
• *Power consumption:* *VCC_3V3 / 43 mA typical* *VIN / 100 mA typical*	*Conditions:* ***VCC_3V3 = 3.3 V, VIN = 4.25 V*** *256 kByte SRAM, 32 MByte Flash, 128 MB LP-DDR-RAM, 64 MB NAND-Flash, Ethernet, 400 MHz CPU frequency at 20°C*

These specifications describe the standard configuration of the phyCORE-i.MX27 as of the printing of this manual.

13 Hints for Handling the phyCORE-i.MX27

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

14 The phyCORE i.MX27 on the i.MX Carrier Board

In this chapter you will find the information about using the phyCORE-i.MX27 module with the phyCORE i.MX Carrier Board.
You will get an overview of how the phyCORE-i.MX27 module works with the phyCORE-i.MX Carrier Board, how both boards are connected together over the phyMAPPER and you will also find all settings that have to be done for a speedy and secure start-up of your i.MX27 module.

In this chapter you will only find specialized information of how the phyCORE-i.MX27 module works with the phyCORE-i.MX Carrier Board. *For further information about the Carrier Board please refer to the i.MX Carrier Board Hardware Manual.*

14.1 Concept of the phyCORE-i.MX Development Kits

Phytec decided to use one i.MX Carrier Board for different i.MX modules. Because every i.MX module has different features and therefore a different pinning it is necessary to map the signals of the modules to the right place on the Carrier Board.
For this every i.MX module comes with a phyMAPPER that is mapping the signals of the i.MX module to the i.MX Carrier Board.
An example of the concept is shown in *Figure 12* below. *For further information about the concept of the i.MX Carrier Board refer to the i.MX Carrier Board Hardware Manual*.

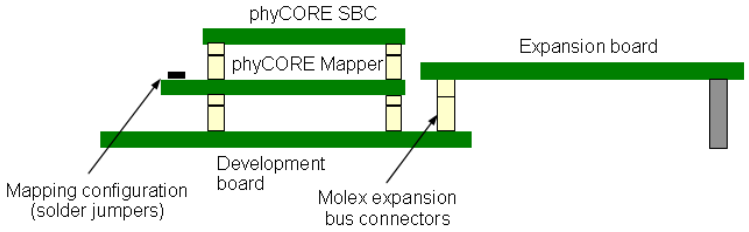

Figure 12: phyCORE-i.MX27 Carrier Board connection using the phyMAP-i.MX27

Figure 13 below illustrates the modular development platform concept:

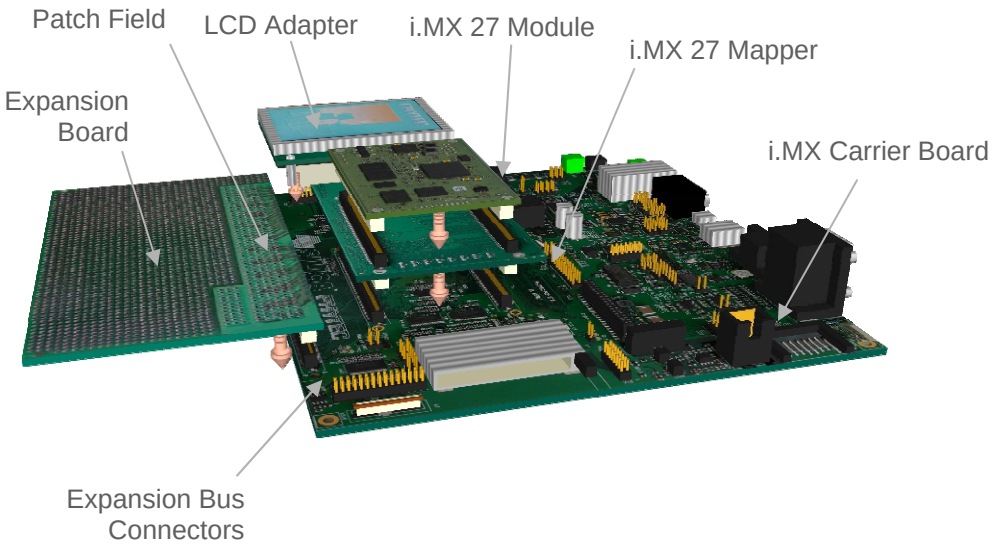

Figure 13: Modular development and Expansion Board concept with phyCORE-i.MX27

14.2 phyMAP-i.MX27

The phyMAP-i.MX27 is responsible for mapping the signals from the various phyCORE-i.MX modules to the phyCORE-i.MX Carrier Board. Signal differences at the connectors on the phyCORE-i.MX modules, along with signal differences between the phyCORE-i.MX module connectors and i.MX Carrier Board connector do not allow for direct connection of the phyCORE-i.MX modules into a single, standardized Carrier Board. To allow for the use of a single Carrier Board, despite the signal differences, the phyMAP-i.MX27 board serves as the gateway to properly map signals from the i.MX Carrier Board Molex connectors to the various phyCORE-i.MX module connectors.

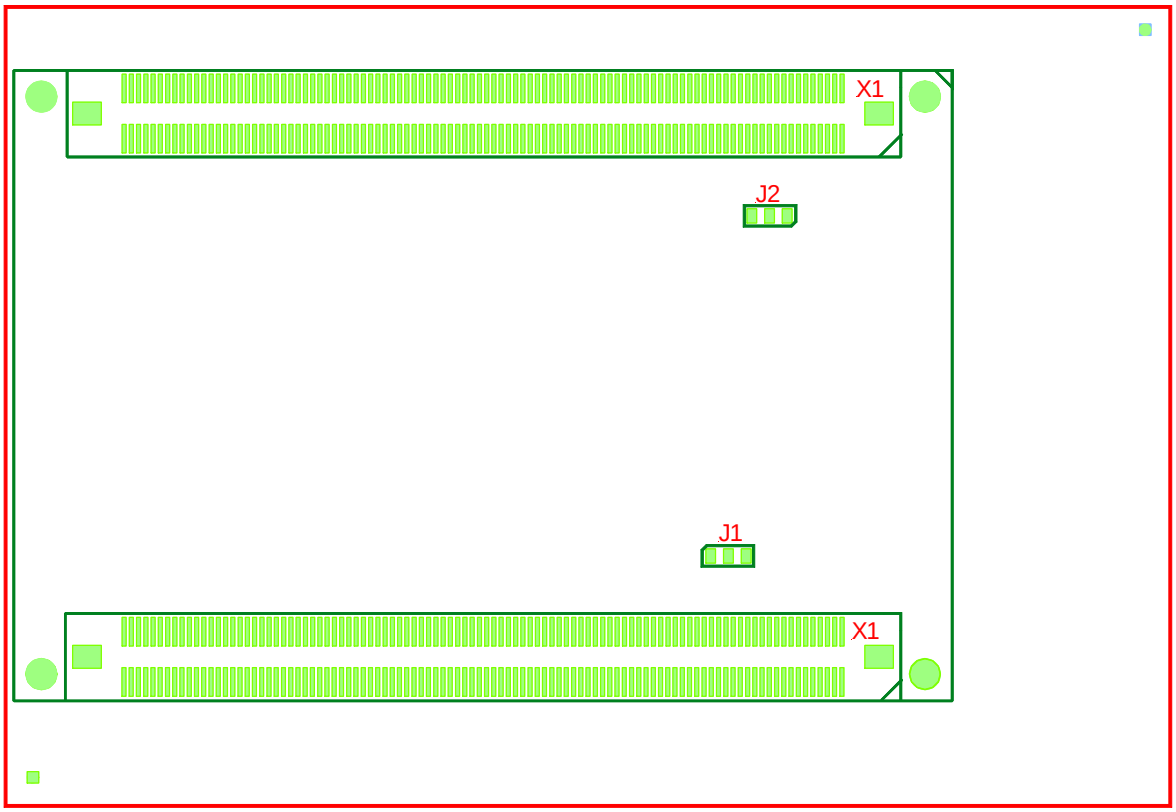

Figure 14: phyMAP-i.MX27 top view

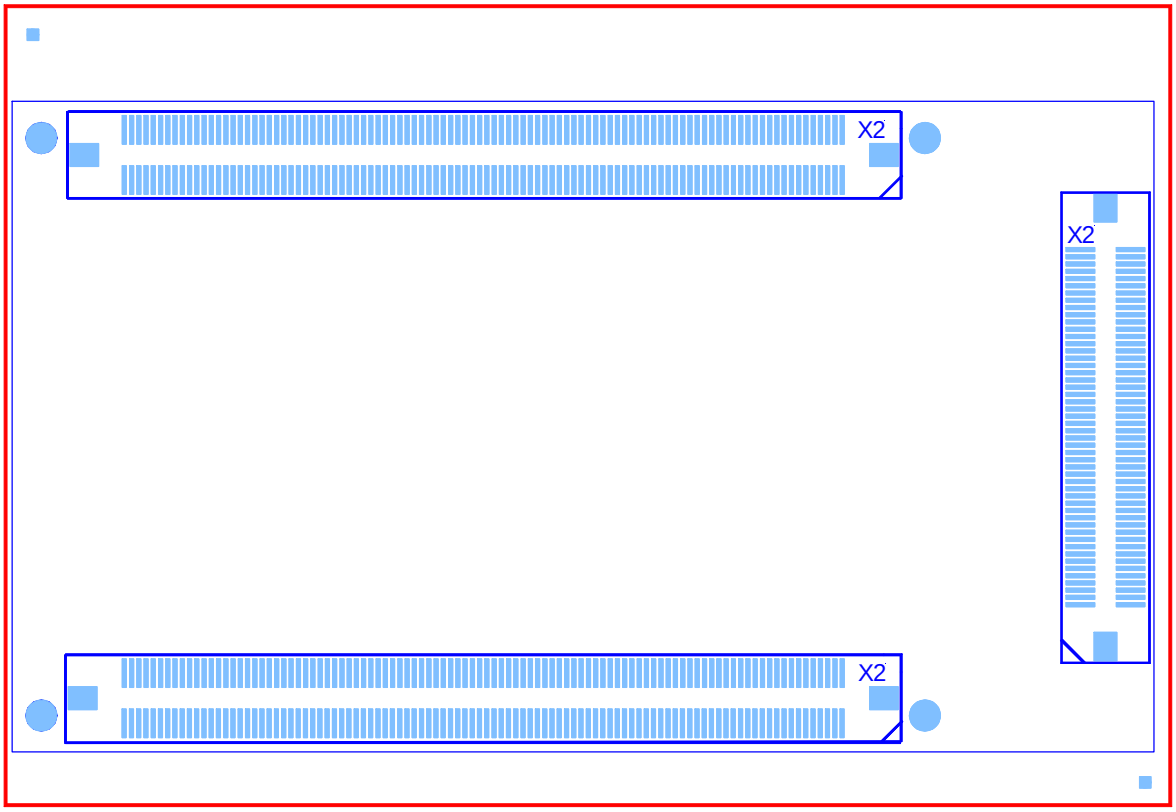

Figure 15: phyMAP-i.MX27 bottom view

14.2.1 phyMAP-i.MX27 Jumper Settings

Figure 16: Jumper location on PMA-005

There are 2 solder jumpers (0805) available on the phyMAP-i.MX27 Mapper. They are used to set different functions partially in relation with the i.MX Carrier Board.
An individual description of the jumpers and a list of all jumper settings you will find subsequent.

J1 With this jumper you can select the backup power supply of the module. If it is set to 1+2 the backup power supply device is the goldcap C161 of the Carrier Board. If J1 is set to 2+3 the backup power is provided by a Li-Cell at connector X20 of the Carrier Board.

J2 Whether the Phytec provided Sharp-Display or the Hitachi-Display is used with the i.MX27 Development Kit this jumper has to be set to the right position. In position 1+2 the X_OE_ACD signal for the Hitachi Display is connected to the display. When J2 is set to 2+3 the X_PS signal for the Sharp-Display is connected to the display.

Table 17: Jumper settings of PMA-002

JUMPER	SETTING	DESCRIPTION
J1	1+2 2+3	x_BKUP_SUPPLY supplied by X_LICELL x_BKUP_SUPPLY supplied by X_VBAT
J2	1+2 2+3	Hitachi display is used Sharp display is used

14.2.2 phyMAP-i.MX27 Signal Mapping

In the following table you will find all signals of the phyCORE-i.MX27 module (PCM-038) connected through the phyMAP-i.MX27 mapper (PMA-002) to the phyCORE-i.MX Carrier Board (PCM-970).
Take care that there are some signals connected to jumpers on the phyMAP-i.MX27 mapper. With this signals it depends on the individual jumper setting where this signals are connected to. This signals are in **bold** text.

Table 18: PMA-002 mapping list

Signal Name on PMA-002 Mapper	X1 Pin #	mapped to	X2 Pin #	Signal Name on i.MX Carrier Board
X_#BATTDET	43C	<->	25E	x_EXP038
X_#CSD1	25B	<->	2F	x_EXP002
X_#CSPI1_RDY	90C	<->	41F	x_EXP065
X_#CS0	24A	<->	1E	x_EXP000
X_#CS1	25A	<->	1F	x_EXP001
X_#CS4	26A	<->	58A, 3E	x_/CS_CAN, x_EXP003
X_#CS5	26B	<->	3F	x_EXP004
X_#ECB	30B	<->	4E	x_EXP005
X_#FL_WP	58B	<->	49E	x_EXP077
X_#IRQRTC	82D	<->	45E	x_EXP070
X_#LBA	30A	<->	54A	x_LBA
X_#LOWBAT	50C	<->	31E	x_EXP048
X_#ON1	30C	<->	55D	x_/ON1
X_#ON2	31C	<->	56C	x_/ON2
X_#ON3	37D	<->	56D	x_/ON3
X_#PC_CD1	60A	<->	66A	x_/PC_CD1
X_#PC_CD2	60B	<->	66B	x_/PC_CD2
X_#PC_IORD/#EB1	28A	<->	56B	x_/EB1
X_#PC_IOWR/#OE	29A	<->	53A	x_/OE
X_#PC_REG/#EB0	27B	<->	55B	x_/EB0
X_#PC_RW	63A	<->	64A	x_/PC_RW
X_#PC_WAIT	65B	<->	61B	x_/PC_WAIT
X_#PC_WE/#RW	28B	<->	55A	x_/WR
X_#RESET	5D	<->	68D	x_EXP081
X_#RESET_OUT	4D	<->	68C	x_EXP080
X_#RST_MCU	6D	<->	4D, 5D, 44C	x_/RESET_3V3, x_/Reset_Btn, x_JTAG_SRST
X_#TRST	41C	<->	43D	x_CPU_/TRST
X_#USBH1_OE	75D	<->	35F	x_EXP055
X_ADIN5	44C	<->	25F	x_EXP039

X_ADIN6	45C	<->	26E	x_EXP040
X_ADIN7	46C	<->	26F	x_EXP041
X_ADIN8	45D	<->	27F	x_EXP042
X_ADIN9	46D	<->	28E	x_EXP043
X_ADIN10	47D	<->	28F	x_EXP044
X_ADIN11	48D	<->	29E	x_EXP045
X_ADOUT	48C	<->	30E	x_EXP046
X_ADTRIG	49C	<->	30F	x_EXP047
X_A0	31B	<->	27B	x_A0
X_A1	32B	<->	28A	x_A1
X_A2	33A	<->	28B	x_A2
X_A3	33B	<->	29A	x_A3
X_A4	34A	<->	30A	x_A4
X_A5	35A	<->	30B	x_A5
X_A6	35B	<->	31A	x_A6
X_A7	36A	<->	31B	x_A7
X_A8	36B	<->	32B	x_A8
X_A9	37B	<->	33A	x_A9
X_A10	38A	<->	33B	x_A10
X_A11	38B	<->	34A	x_A11
X_A12	39A	<->	35A	x_A12
X_A13	40A	<->	35B	x_A13
X_A14	40B	<->	36A	x_A14
X_A15	41A	<->	36B	x_A15
X_A16	41B	<->	37B	x_A16
X_A17	42B	<->	38A	x_A17
X_A18	43A	<->	38B	x_A18
X_A19	43B	<->	39A	x_A19
X_A20	44A	<->	40A	x_A20
X_A21	45A	<->	40B	x_A21
X_A22	45B	<->	41A	x_A22
X_A23	46A	<->	41B	x_A23
X_A24	46B	<->	42B	x_A24
X_A25	47B	<->	43A	x_A25
X_BATTFET	15C	<->	15C	x_BATTFET
X_BATTISNS	14C	<->	14C	x_BATTISNS
X_BCLK	31A	<->	18E	x_EXP027
X_BFET	16D	<->	17D	x_BFET
X_BKUP_SUPPLY	18C	<->	18C, (6C)	x_LICELL, (x_VBAT)
X_BOOT0	99C	<->	100B	x_switch
X_BOOT1	98C	<->	53C	x_BOOT_MODE0

X_BOOT2	98D	<->	53D	x_BOOT_MODE1
X_CE0	66A	<->	58B	x_/CE2
X_CE1	66B	<->	57B	x_/CE1
X_CHARGER_INPUT_3-20V	10D, 11D, 12D, 13D	<->	10D, 11D, 12D, 13D	Charger_Input -> x_Charger_Input
X_CHRGCTL	17D	<->	18D	x_CHRGCTL
X_CHRGISNSN	15D	<->	16D	x_CHRGISNSN
X_CHRGISNSP	16C	<->	16C	x_CHRGISNSP
X_CHRGLED	19C	<->	19C	x_CHRGLED
X_CHRGMOD0	20C	<->	20C	x_CHRGMOD0
X_CLKO	100B	<->	20F	x_EXP031
X_CLS	8B	<->	8B	x_LC_D3_CLS
X_CONTRAST	7B	<->	7B	x_LC_CONTRAST
X_CSI_D0	78A	<->	75A	x_CSI_D2
X_CSI_D1	78B	<->	75B	x_CSI_D3
X_CSI_D2	79A	<->	76A	x_CSI_D4
X_CSI_D3	80A	<->	76B	x_CSI_D5
X_CSI_D4	80B	<->	77B	x_CSI_D6
X_CSI_D5	81A	<->	78A	x_CSI_D7
X_CSI_D6	81B	<->	78B	x_CSI_D8
X_CSI_D7	82B	<->	79A	x_CSI_D9
X_CSI_HSYNC	85B	<->	73B	x_CSI_HSYNC
X_CSI_MCLK	84A	<->	69A	x_CSI_MCLK
X_CSI_PIXCLK	86A	<->	71B	x_CSI_PCLK
X_CSI_VSYNC	85A	<->	72B	x_CSI_VSYNC
X_CSPI1_MISO	87D	<->	96B	x_MISO
X_CSPI1_MOSI	86D	<->	95B	x_MOSI
X_CSPI1_SCLK	86C	<->	97B	x_SPICLK
X_CSPI1_SS1	88C	<->	98B	X_CE
X_D0	48A	<->	43B	x_D0
X_D1	48B	<->	44A	x_D1
X_D2	49A	<->	45A	x_D2
X_D3	50A	<->	45B	x_D3
X_D4	50B	<->	46A	x_D4
X_D5	51A	<->	46B	x_D5
X_D6	51B	<->	47B	x_D6
X_D7	52B	<->	48A	x_D7
X_D8	53A	<->	48B	x_D8
X_D9	53B	<->	49A	x_D9
X_D10	54A	<->	50A	x_D10
X_D11	55A	<->	50B	x_D11

X_D12	55B	<->	51A	x_D12
X_D13	56A	<->	51B	x_D13
X_D14	56B	<->	52B	x_D14
X_D15	57B	<->	53B	x_D15
X_ETH_#PD	38C	<->	5E	x_EXP006
X_ETH_LINK	33C	<->	32D	x_ETH_/LED1
X_ETH_RX+	35D	<->	30C	x_ETH_TPI+
X_ETH_RX-	35C	<->	31C	x_ETH_TPI-
X_ETH_SPEED	34C	<->	33D	x_ETH_/LED2
X_ETH_TX+	36D	<->	30D	x_ETH_TPO+
X_ETH_TX-	36C	<->	31D	x_ETH_TPO-
X_FEC_COL	76B	<->	15E	x_EXP022
X_FEC_CRS	73B	<->	11F	x_EXP017
X_FEC_MDC	73A	<->	11E	x_EXP016
X_FEC_MDIO	72C	<->	10F	x_EXP015
X_FEC_RXD0	75A	<->	13E	x_EXP019
X_FEC_RXD1	70B	<->	8F	x_EXP012
X_FEC_RXD2	71A	<->	9E	x_EXP013
X_FEC_RXD3	71B	<->	10E	x_EXP014
X_FEC_RX_CLK	76A	<->	14E	x_EXP021
X_FEC_RX_DV	75B	<->	13F	x_EXP020
X_FEC_RX_ER	70A	<->	8E	x_EXP011
X_FEC_TXD0	86B	<->	16F	x_EXP025
X_FEC_TXD1	87B	<->	17F	x_EXP026
X_FEC_TXD2	68B	<->	6F	x_EXP009
X_FEC_TXD3	69A	<->	7F	x_EXP010
X_FEC_TX_CLK	74A	<->	12F	x_EXP018
X_FEC_TX_EN	83B	<->	16E	x_EXP024
X_FEC_TX_ER	77B	<->	15F	x_EXP023
X_GPO1	20D	<->	21F	x_EXP033
X_GPO2	21D	<->	22F	x_EXP034
X_GPO3	27D	<->	23E	x_EXP035
X_GPO4	28D	<->	23F	x_EXP036
X_GPT4_TIN	96C	<->	46E	x_EXP072
X_GPT4_TOUT	95C	<->	46F	x_EXP073
X_GPT5_TIN	94C	<->	47F	x_EXP074
X_GPT5_TOUT	93C	<->	48F	x_EXP076
X_HSYNC	5B	<->	11A	x_LC_FPLINE
X_IMX27_FUSE	7D	<->	6D	x_iMX_FUSE
X_IOIS16	68A	<->	65A	x_IOIS16
X_I2C_CLK	85D	<->	99A	x_I2C_SCL

X_I2C_DATA	85C	<->	100A	x_I2C_SDA
X_I2C2_SCL	83C	<->	39E	x_EXP061
X_I2C2_SDA	84C	<->	40E	x_EXP062
X_JTAG_CTRL	43D	<->	43C	x_CPU_SJC_MOD
X_KP_COL0	88A	<->	48D	x_KEY_COL0
X_KP_COL1	89A	<->	49C	x_KEY_COL1
X_KP_COL2	90A	<->	50C	x_KEY_COL2
X_KP_COL3	90B	<->	50D	x_KEY_COL3
X_KP_COL4	95B	<->	51C	x_KEY_COL4
X_KP_COL5	96B	<->	51D	x_KEY_COL5
X_KP_ROW0	91A	<->	45C	x_KEY_ROW0
X_KP_ROW1	91B	<->	45D	x_KEY_ROW1
X_KP_ROW2	92B	<->	46C	x_KEY_ROW2
X_KP_ROW3	93A	<->	46D	x_KEY_ROW3
X_KP_ROW4	93B	<->	47D	x_KEY_ROW4
X_KP_ROW5	94A	<->	48C	x_KEY_ROW5
X_LD0	13A	<->	13A	x_LC_D0
X_LD1	13B	<->	13B	x_LC_D1
X_LD2	14A	<->	14A	x_LC_D2
X_LD3	15A	<->	15A	x_LC_D3
X_LD4	15B	<->	15B	x_LC_D4
X_LD5	16A	<->	16A	x_LC_D5
X_LD6	16B	<->	16B	x_LC_D6
X_LD7	17B	<->	17B	x_LC_D7
X_LD8	18A	<->	18A	x_LC_D8
X_LD9	18B	<->	18B	x_LC_D9
X_LD10	19A	<->	19A	x_LC_D10
X_LD11	20A	<->	20A	x_LC_D11
X_LD12	20B	<->	20B	x_LC_D12
X_LD13	21A	<->	21A	x_LC_D13
X_LD14	21B	<->	21B	x_LC_D14
X_LD15	22B	<->	22B	x_LC_D15
X_LD16	23B	<->	23B	x_LC_D16
X_LD17	23A	<->	23A	x_LC_D17
X_LSCLK	10B	<->	10B	x_LC_BCLK
X_MC1LIN	29C	<->	29C	x_MC1LIN
X_MC1RIN	28C	<->	28C	x_MC1RIN
X_OE_ACD	6A	<->	10A, 24E	x_LC_DRDY0, x_EXP037
X_OWIRE	91D	<->	58D	x_1Wire
X_PB24	58C	<->	70B	x_CSI_ENABLE
X_PC_BVD1	58A	<->	60A	x_PC_BVD1

X_PC_BVD2	59A	<->	61A	x_PC_BVD2
X_PC_POE	61B	<->	62B	x_PCOE
X_PC_PWRON	61A	<->	63A	x_PC_PWRON
X_PC_READY	62B	<->	63B	x_PC_READY
X_PC_RST	63B	<->	65B	x_PC_RST
X_PC_VS1	64A	<->	67B	x_PC_VS1
X_PC_VS2	65A	<->	68B	x_PC_VS2
X_PC28	95A	<->	95A	x_SD_W
X_PC29	98A	<->	94A	x_SD_D
X_PC30	99A	<->	71A	x_SNAPSHOT
X_PC31	100A	<->	70A	x_TRIGGER
X_PE18	90D	<->	58C, 5F, 42F	x_LED, x_EXP007, x_EXP066
X_PE19	91C	<->	59A, 96A	x_CAN_INT, x_/IRQ
X_PE20	39C	<->	70D	x_EXP084
X_PE21	3B	<->	43E	x_EXP067
X_PE22	2B	<->	41E	x_EXP064
X_PE23	1B	<->	40F	x_EXP063
X_POWER_BATT	13C	<->	15D	x_Power_BATT
X_PRIINT	81D	<->	69C	x_EXP082
X_PS	10A	<->	10A	x_LC_DRDY0
X_PWMO	100D	<->	45F	x_EXP071
X_PWRRDY	18D	<->	6E	x_EXP008
X_REV	8A	<->	8A	x_LC_D3_REV
X_RXINL	25C	<->	25C	x_RXINL
X_RXINR	26C	<->	26C	x_RXINR
X_RXOUTL_LSPP	23C	<->	23C	x_RXOUTL
X_RXOUTR_LSPM	24C	<->	24C	x_RXOUTR
X_SD2_CLK	70D	<->	91A	x_SD1_CLK
X_SD2_CMD	68D	<->	90B	x_SD1_CMD
X_SD2_D0	68C	<->	91B	x_SD1_DATA0
X_SD2_D1	69C	<->	92B	x_SD1_DATA1
X_SD2_D2	70C	<->	93A	x_SD1_DATA2
X_SD2_D3	71C	<->	93B	x_SD1_DATA3
X_SPL_SPR	9A	<->	9A	x_LC_D3_SPL
X_TCK	38D	<->	40D	x_CPU_TCK
X_TDI	40D	<->	39C	x_CPU_TDI
X_TDO	41D	<->	40C	x_CPU_TDO
X_TIN	96D	<->	50F	x_EXP079
X_TMS	42D	<->	41C	x_CPU_TMS
X_TOUT	8D	<->	48E	x_EXP075

X_TOUT1	97D	<->	50E	x_EXP078
X_TSX1	30D	<->	25D	x_TSX1
X_TSX2	31D	<->	26D	x_TSX2
X_TSY1	32D	<->	27D	x_TSY1
X_TSY2	33D	<->	28D	x_TSY2
X_UART1_CTS_RS232	26D	<->	65C	x_CTS_RS232
X_UART1_RTS_RS232	25D	<->	66C	x_RTS_RS232
X_UART1_RXD_RS232	22D	<->	65D	x_RXD_RS232
X_UART1_TXD_RS232	23D	<->	66D	x_TXD_RS232
X_UART2_CTS	74C	<->	61D	x_CTS_DCE1_TTL
X_UART2_RTS	73C	<->	60D	x_RTS_DCE1_TTL
X_UART2_RXD	73D	<->	61C	x_RXD_DCE1_TTL
X_UART2_TXD	72D	<->	60C	x_TXD_DCE1_TTL
X_UART3_CTS	79C	<->	38E	x_EXP059
X_UART3_RTS	78D	<->	38F	x_EXP060
X_UART3_RXD	77D	<->	36F	x_EXP057
X_UART3_TXD	78C	<->	37F	x_EXP058
X_UDM	54C	<->	34C	x_UDM
X_UDP	55C	<->	35C	x_UDP
X_UID	56C	<->	36C	x_UID
X_USBH1_FS	76D	<->	36E	x_EXP056
X_USBH1_RCV	55D	<->	34E	x_EXP053
X_USBH1_RXDM	50D	<->	31F	x_EXP049
X_USBH1_RXDP	51D	<->	32F	x_EXP050
X_USBH1_SUSP	58D	<->	35E	x_EXP054
X_USBH1_TXDM	52D	<->	33E	x_EXP051
X_USBH1_TXDP	53D	<->	33F	x_EXP052
X_USBH2_CLK	60C	<->	83A	x_USBHOST2_CLK
X_USBH2_DATA0	62D	<->	85A	x_USBHOST2_DA0
X_USBH2_DATA1	63D	<->	85B	x_USBHOST2_DA1
X_USBH2_DATA2	63C	<->	86A	x_USBHOST2_DA2
X_USBH2_DATA3	65D	<->	86B	x_USBHOST2_DA3
X_USBH2_DATA4	64C	<->	87B	x_USBHOST2_DA4
X_USBH2_DATA5	66D	<->	88A	x_USBHOST2_DA5
X_USBH2_DATA6	65C	<->	88B	x_USBHOST2_DA6
X_USBH2_DATA7	67D	<->	89A	x_USBHOST2_DA7
X_USBH2_DIR	61C	<->	84A	x_USBHOST2_DIR
X_USBH2_NXT	61D	<->	83B	x_USBHOST2_NXT
X_USBH2_STP	60D	<->	82B	x_USBHOST2_STP
X_USB_HS_/PSW	56D	<->	35D	x_USB_HS_/PSW
X_USB_HS_FAULT	57D	<->	36D	x_USB_HS_FAULT

X_USEROFF	51C	<->	21E	x_EXP032
X_VBUS	53C	<->	33C	x_VBUS
X_VSYNC	5A	<->	5B	x_LC_FPFRAME

Note:
Signals in **bold** text are connected to jumpers. The mapping of this signals could differ from the mapping list. Please check the positions of the affected jumpers to find out how the signals are mapped.

14.2.3 phyMAP-i.MX27 Mapper Physical Dimensions

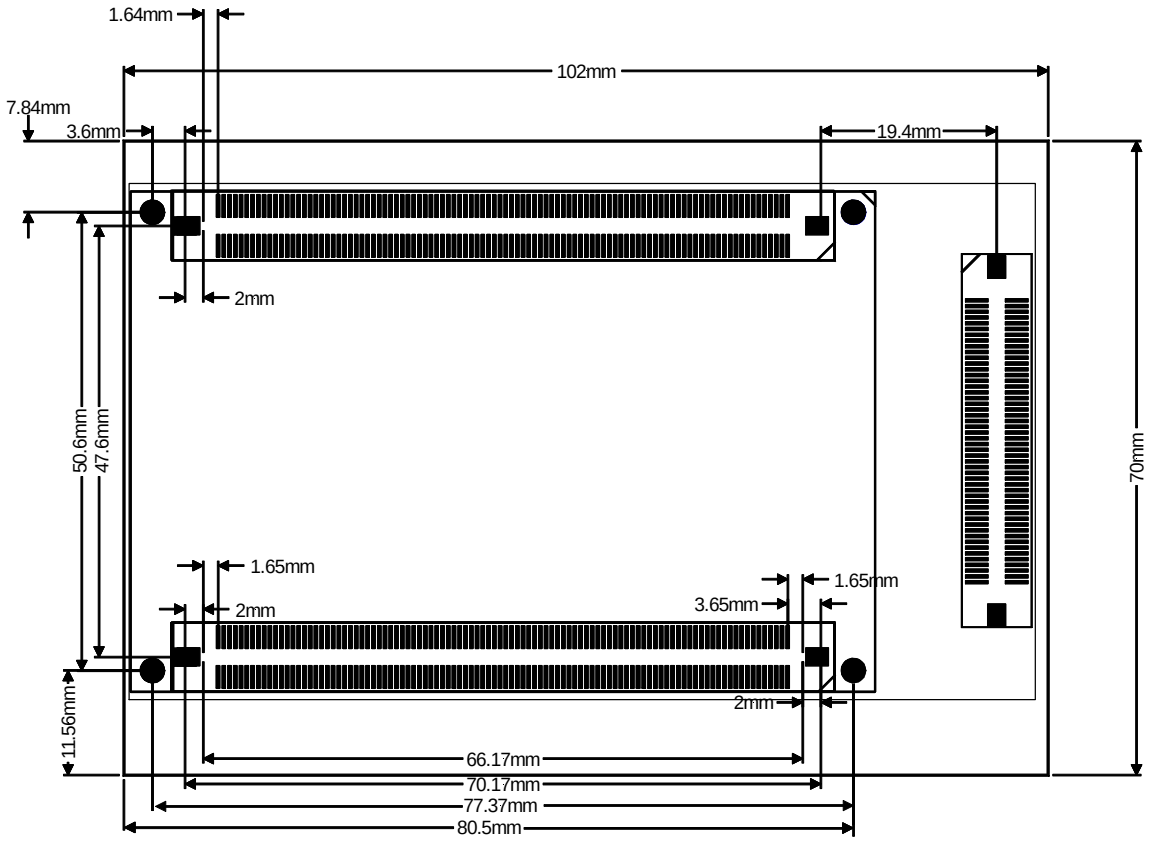

Figure 17: Physical dimensions of phyMAP-i.MX27 mapper

14.3 Cooperation of phyCORE-i.MX27 and phyCORE-i.MX Carrier Board

In this chapter you will find specific information and settings to adapt the i.MX Carrier Board to the i.MX27 module.
For information about the general functionality of the various interfaces of the phyCORE-i.MX Carrier Board, please refer to the phyCORE-i.MX Carrier Board Hardware Manual.

14.3.1 Power Supply

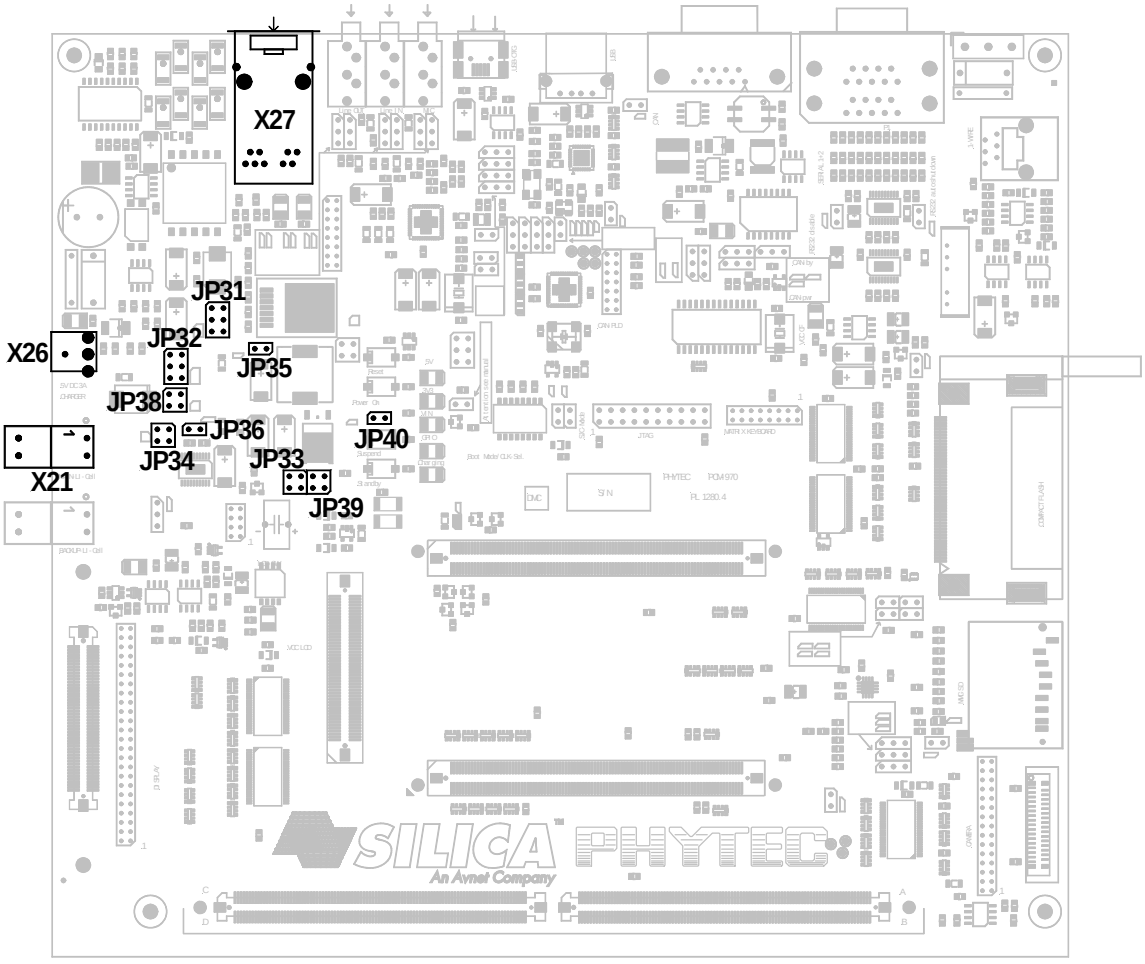

Figure 18: pyhCORE-i.MX Carrier Board and phyCORE-i.MX27 Power Supply

Subsequent you will find the different jumper settings for the three power supply modes described in the phyCORE-i.MX Carrier Board Hardware Manual.

Note:
With the phyCORE-i.MX27 module the Power Management IC MC13783 is provided so battery charging is also provided with the i.MX27 module.

14.3.1.1 Power Supply via Power Plug

Table 19 below shows the jumper settings to supply the phyCORE-i.MX27 module and the phyCORE-i.MX Carrier Board with a wall charger at X26 of the i.MX Carrier Board.

Table 19: Jumper settings for i.MX27 power supply via power plug[6]

JUMPER	SETTING	DESCRIPTION
JP31	1+3,2+4 **3+5,4+6**	Power source is Power Over Ethernet (POE) **Power source is 5 V adapter**
JP32	1+3,2+4 **3+5,4+6**	No power switching, direct supply of VCC_3V3 **Separate supply path**
JP33	1+2,3+4 **open,open**	No power switching, direct supply from VCC_3V3 **Separate supply path**
JP34	1+2,3+4 **open,open**	No power switching, direct supply from VCC_3V3 **Separate supply path**
JP35	**open** closed	**VCC_5V Power Supply is enabled** VCC_5V Power Supply is disabled
JP36	open **closed**	VCC_3V3 Power Supply is disabled **VCC_3V3 Power Supply is enabled**
JP38	**1+2,3+4** open,open	**Power switching, supply from 5 V adapter or POE** No power switching, direct supply from VCC_3V3
JP39	**1+2,3+4** open,open	**Power switching active, Battery charge path closed** No power switching, direct supply from VCC_3V3
JP40	open **closed**	No power switching active, minimum circuit **Power switching active**

6 Settings for the phyCORE-i.MX27 power supply via power plug are in **bold blue**

14.3.1.2 Power Supply via Power over Ethernet

Table 20 below shows the jumper settings to supply the phyCORE-i.MX27 module and the phyCORE-i.MX Carrier Board with Power over Ethernet at X27.

Table 20: Jumper settings for i.MX27 power supply via POE[7]

JUMPER	SETTING	DESCRIPTION
JP31	**1+3,2+4**	**Power source is Power Over Ethernet (POE)**
	3+5,4+6	Power source is 5V adapter
JP32	1+3,2+4	No power switching, direct supply of VCC_3V3
	3+5,4+6	**Separate supply path**
JP33	1+2,3+4	No power switching, direct supply from VCC_3V3
	open,open	**Separate supply path**
JP34	1+2,3+4	No power switching, direct supply from VCC_3V3
	open,open	**Separate supply path**
JP35	**open**	**VCC_5V Power Supply is enabled**
	closed	VCC_5V Power Supply is disabled
JP36	open	VCC_3V3 Power Supply is disabled
	closed	**VCC_3V3 Power Supply is enabled**
JP38	**1+2,3+4**	**Power switching, supply from 5 V adapter or POE**
	open,open	No power switching, direct supply from VCC_3V3
JP39	**1+2,3+4**	**Power switching active, Battery charge path closed**
	open,open	No power switching, direct supply from VCC_3V3
JP40	open	No power switching active, minimum circuit
	closed	**Power switching active**

7 Settings for the phyCORE-i.MX27 power supply via Power over Ethernet are in **bold blue**

14.3.1.3 Power Supply via Battery

Table 21 below shows the jumper settings to supply the phyCORE-i.MX27 module and the phyCORE-i.MX Carrier Board with a battery at X21 of the i.MX Carrier Board.

Table 21: Jumper settings for i.MX27 power supply via battery[8]

JUMPER	SETTING	DESCRIPTION
JP31	1+3,2+4	Power source for battery charging is Power Over Ethernet (POE)
	3+5,4+6	**Power source for battery charging is 5 V adapter**
JP32	1+3,2+4	No power switching, direct supply of VCC_3V3
	3+5,4+6	**Separate supply path**
JP33	1+2,3+4	No power switching, direct supply from VCC_3V3
	open,open	**Separate supply path**
JP34	1+2,3+4	No power switching, direct supply from VCC_3V3
	open,open	**Separate supply path**
JP35	**open**	**VCC_5V Power Supply is enabled**
	closed	VCC_5V Power Supply is disabled
JP36	open	VCC_3V3 Power Supply is disabled
	closed	**VCC_3V3 Power Supply is enabled**
JP38	**1+2,3+4**	**Power switching, supply from 5 V adapter or POE**
	open,open	No power switching, direct supply from VCC_3V3
JP39	**1+2,3+4**	**Power switching active, Battery charge path closed**
	open,open	No power switching, direct supply from VCC_3V3
JP40	open	No power switching active, minimum circuit
	closed	**Power switching active**

8 Settings for the phyCORE-i.MX27 power supply via battery are in **bold blue**

14.3.2 CAN Interface

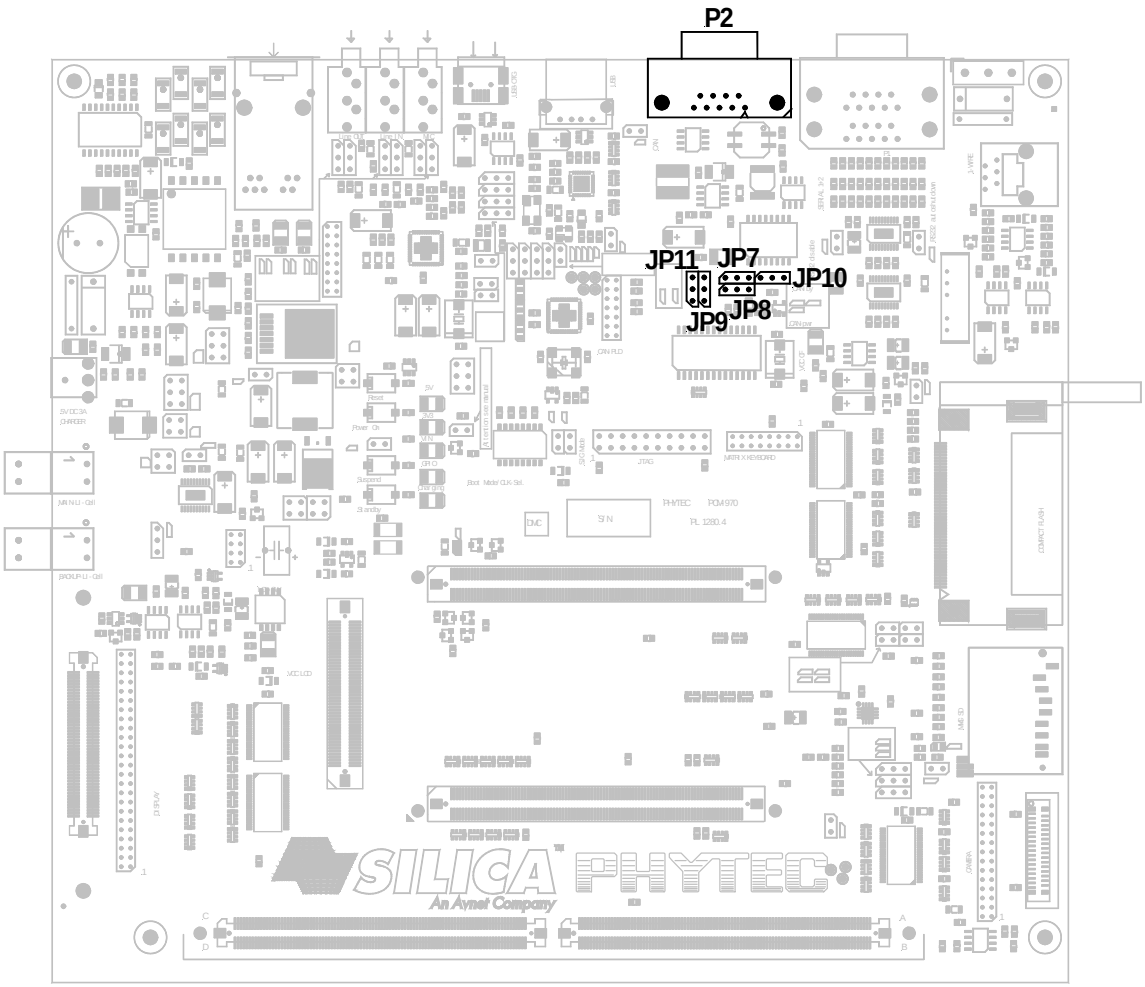

Figure 19: phyCORE-i.MX Carrier Board CAN Interface

The phyCORE-i.MX27 does not provide a CAN controller. For CAN support there is a CAN controller available on the Carrier Board that is connected to the data-/address bus of the phyCORE-i.MX27.
Please refer to Table 22 below for the jumper settings to use the CAN interface with the i.MX27 module.

Table 22: CAN interface jumper settings[9]

JUMPER	SETTING	DESCRIPTION
JP7	**1 + 2** 2 + 3	**CANTxD signal is routed to the CAN transceiver** x_CAN_TxD signal is routed to the CAN transceiver
JP8	1 + 2 **2 + 3**	Digital Isolator is supplied by VCC_CAN **Digital Isolator supply is VCC_5V**
JP9	**1 + 2** 2 + 3	**CANV- is connected to GND of i.MX Carrier Board** CANV- is not connected to GND of i.MX Carrier Board
JP10	**1 + 2** 2 + 3	**CANRxd signal is routed to the CAN transceiver** x_CAN_RxD signal is routed to the CAN transceiver
JP11	**1 + 2** 2 + 3	**CANV+ is connected to VCC_5V of i.MX Carrier Board** CANV+ is connected to CAN_OUT (external supply)

[9] Default settings for the phyCORE-i.MX27 CAN interface on the i.MX Carrier Board are in **bold blue**

14.3.3 Push Buttons and LEDs

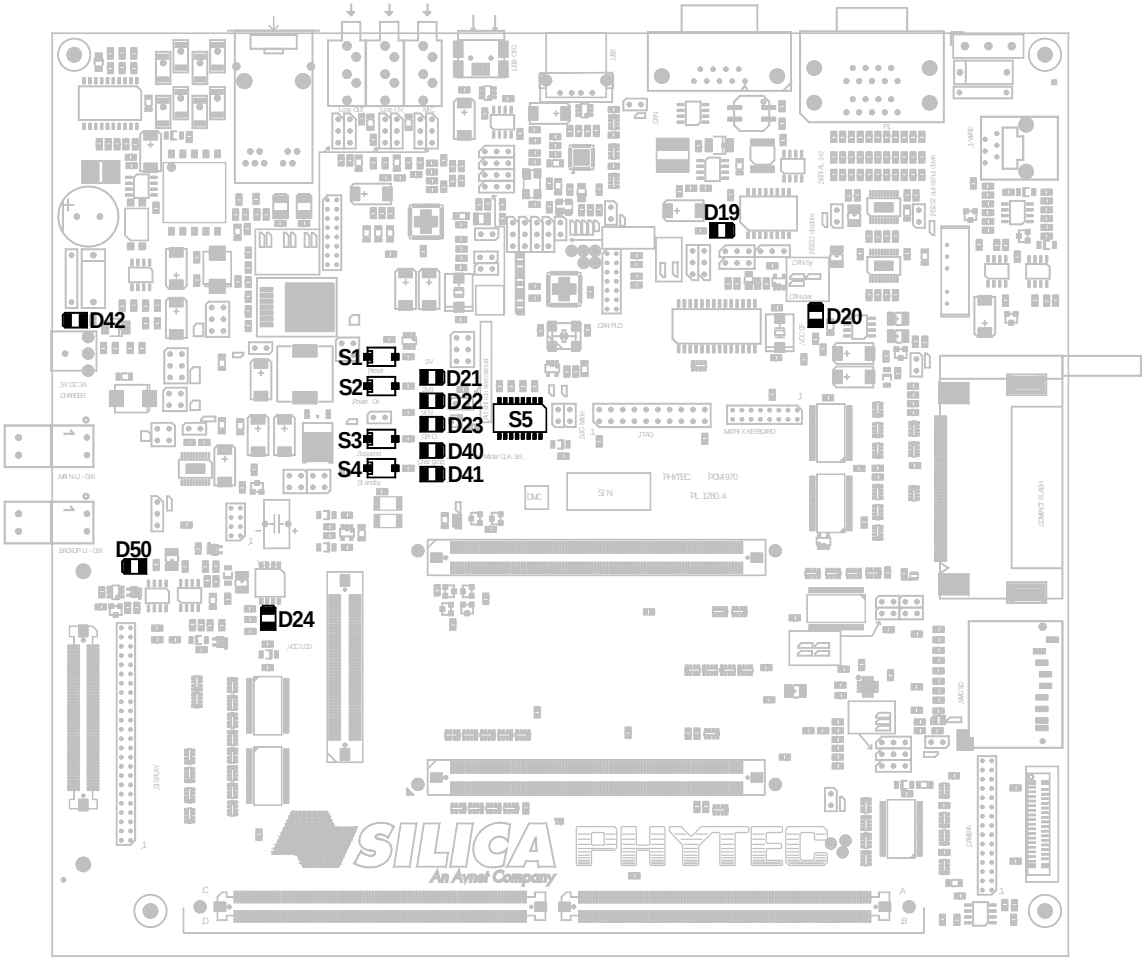

Figure 20: phyCORE-i.MX Carrier Board Buttons and LEDs

The GPIO signal to drive the User-LED D40 high or low is the X_PE18 signal of the i.MX27 module.

Caution!
GPIO PE18 can also be used to manage the power supply of the CF interface on the i.MX Carrier Board. If you only want to drive the User-LED D40 high or low make sure, that jumper JP604 is closed to force the CF interface active.

14.3.3.1 Boot-Mode and Clock Selection

Note:
Clock selection is not available with the i.MX27 module.

The i.MX27 controller is able to boot from different devices as described in *chapter 6.1.2*. To have a choice from which device the controller should boot the boot signals BOOT0 to BOOT2 are connected to the dip-switch S5 on the i.MX Carrier Board.

With S5 on the i.MX Carrier Board it is possible to select the status of BOOT0, BOOT1 and BOOT2. For detailed information see *Table 23*, *Table 24* and *Table 25* below.

Note:
A standard Boot Configuration is already set on the i.MX27 module. Here you can change the Boot Mode to an alternatively mode. For standard Boot Configuration all dip switches have to be in OFF position.

Table 23: x_BOOT_MODE0 selection

STATE OF SW NUMBER 3	STATE OF SW NUMBER 4	STATE OF X_BOOT1
ON	OFF	0
OFF	ON	1

Table 24: x_BOOT_MODE1 selection

STATE OF SW NUMBER 5	STATE OF SW NUMBER 6	STATE OF X_BOOT2
ON	OFF	0
OFF	ON	1

Table 25: x_switch

STATE OF SW NUMBER 7	STATE OF SW NUMBER 8	STATE OF X_BOOT0
ON	OFF	0
OFF	ON	1

14.3.4 Compact Flash Card

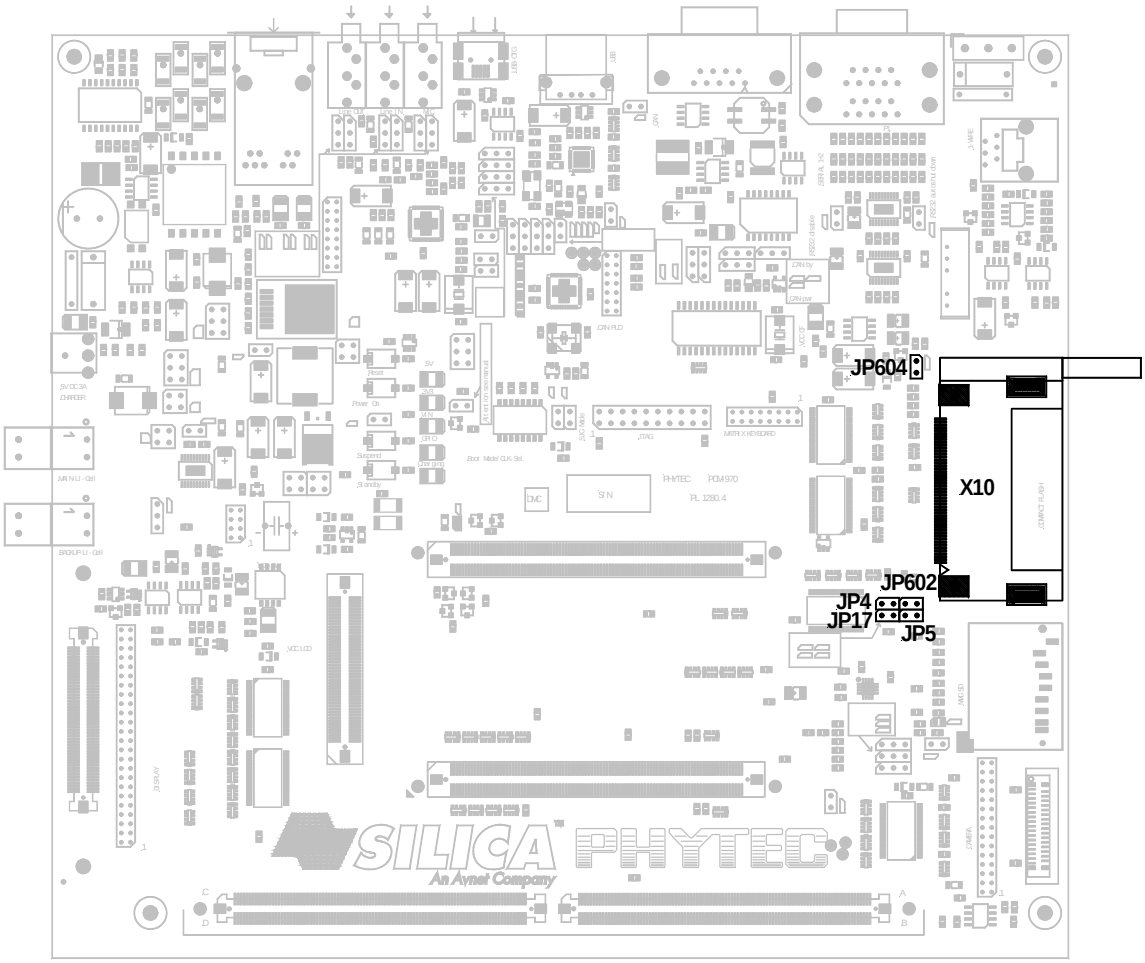

Figure 21: Compact Flash Card Interface

The GPIO signal of the i.MX27 module connected to signal x_EXP007 of the i.MX Carrier Board is X_PE18. With GPIO PE18 the power supply of the CF interface can be managed.

Caution!
GPIO PE18 is also used with the User-LED D40 on the i.MX Carrier Board.

Table 26: CF interface jumper settings[1]

JUMPER	SETTING	DESCRIPTION
JP4	**closed** open	**/PC_RW signal can manage the data direction of U13** Data direction of U13 is from controller to CF
JP5	**closed** open	**Compact Flash is Master** Compact Flash is Slave
JP17	**open** closed	**Output 2 of U15 is active** Output 2 of U15 is disabled
JP602	closed **open**	PC_RW non-inverted **PC_RW inverted**
JP604	**closed** open	**Power supply of CF is forced active** Power supply of CF can be managed by GPIO signal x_EXP007

1 Default settings for the phyCORE-i.MX27 CF interface on the i.MX Carrier Board are in **bold blue**

14.3.5 Security Digital Card/ MultiMedia Card

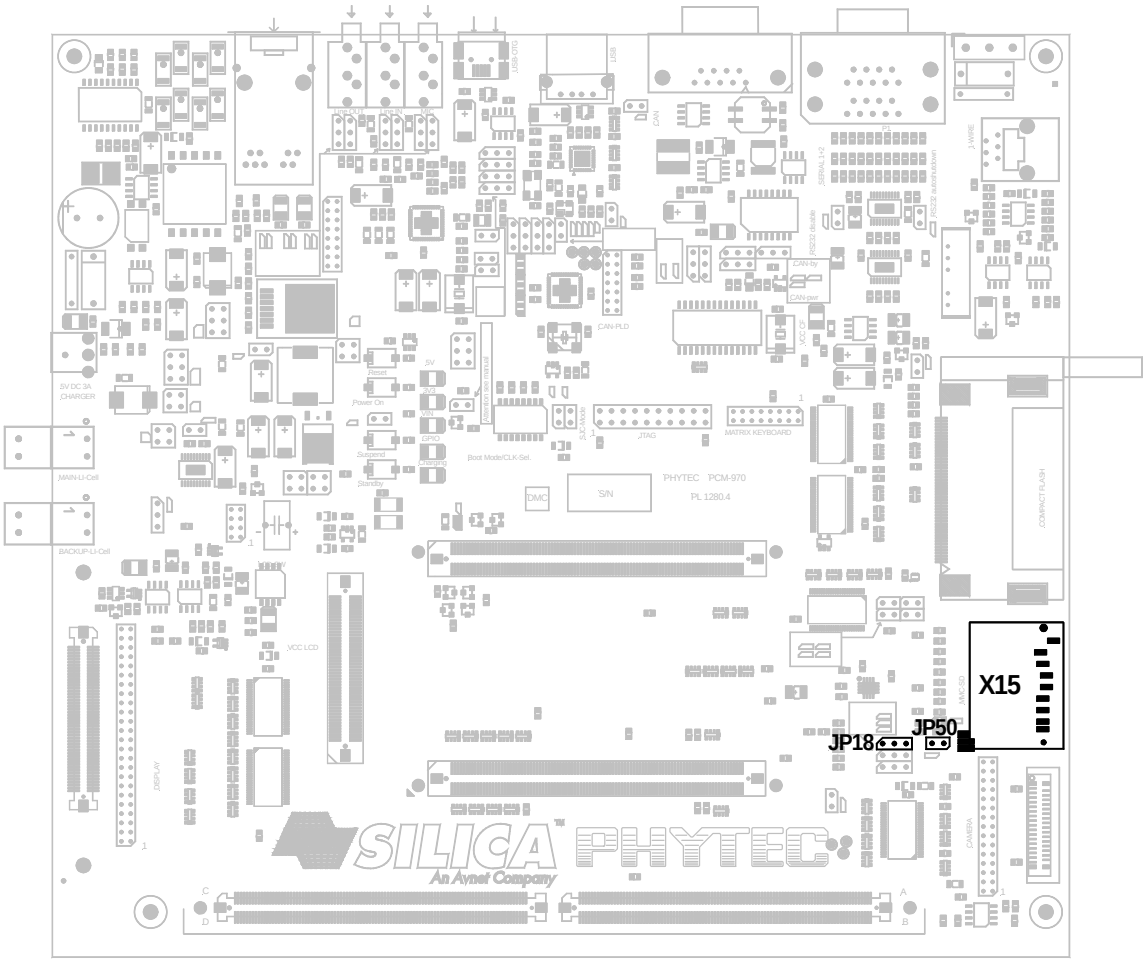

Figure 22: SD Card interface

The MMC_DETECT signal is connected to GPIO signal X_PC29 of the i.MX27 module. MMC_WP is connected to GPIO signal X_PC28.

Table 27: SD/MMC interface jumper settings for i.MX27 module[1]

JUMPER	SETTING	DESCRIPTION
JP50	**2 + 3** 1 + 2	**MMC_WP signal of SD/MMC Interface is connected to GPIO** MMC_WP signal of SD/MMC Interface is not connected to GPIO
JP18	**2 + 3** 1 + 2	**Level shifter U25 is enabled** Level shifter U25 is disabled

1 Default settings for the phyCORE-i.MX27 SD/MMC interface are in **bold blue**

14.3.6 Audio and Touchscreen

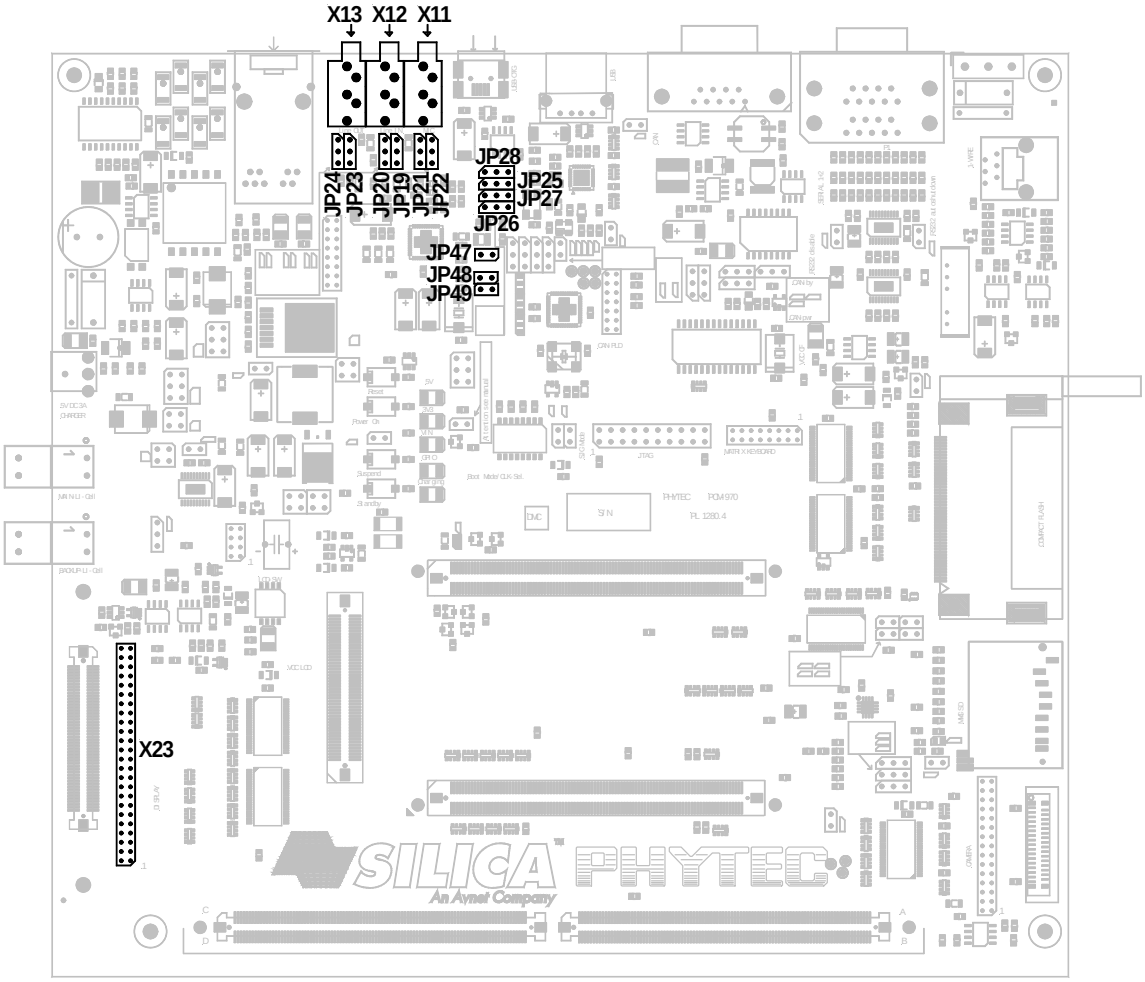

Figure 23: phyCORE-i.MX Carrier Board Audio/Touch Interface

With the phyCORE-i.MX27 module the MC13783 Power Management IC is used that has audio and touch functions integrated. So the i.MX27 module does not have to use the audio/touchscreen device (U24) on the i.MX Carrier Board.
To select that the PMIC audio and touch should be used, there are a variety of jumpers which have to be set.

A detailed list of all jumper settings you will find in *Table 28* below.

Table 28: Audio/Touchscreen interface jumper settings[1]

JUMPER	SETTING	DESCRIPTION
JP21	**2 + 3** 1 + 2	**x_MC1RIN is connected to X11** MIC1 is connected to X11
JP22	**2 + 3** 1 + 2	**x_MC1LIN is connected to X11** MIC2 is connected to X11
JP19	**2 + 3** 1 + 2	**x_RXOUTL is connected to X12** LINE_INR is connected to X12
JP20	**2 + 3** 1 + 2	**x_RXOUTR is connected to X12** LINE_INL is connected to X12
JP23	**2 + 3** 1 + 2	**x_RXINL is connected to X13** LINE_OUTR is connected to X13
JP24	**2 + 3** 1 + 2	**x_RXINR is connected to X13** LINE_OUTL is connected to X13
JP25	**2 + 3** 1 + 2	**x_TSY1 is connected to X23** TP_Y- is connected to X23
JP26	**2 + 3** 1 + 2	**x_TSX2 is connected to X23** TP_X+ is connected to X23
JP27	**2 + 3** 1 + 2	**x_TSY2 is connected to X23** TP_Y+ is connected to X23
JP28	**2 + 3** 1 + 2	**X_TSX1 is connected to X23** TP_X- is connected to X23
JP47	**open** closed	**Reset is held high, no asserting by GPIO of i.MX module** Reset can be asserted by GPIO of i.MX module
JP48	**open** closed	**No access to IRQ via GPIO of i.MX module** Access to IRQ via GPIO of i.MX module
JP49	**open** closed	**No access to PENDOWN via GPIO of i.MX module** Access to PENDOWN via GPIO of i.MX module

Caution!
Jumper JP47 to JP49 always have to be opened with the phyCORE-i.MX27. Functions behind this jumpers are not available for the i.MX27 module.

1 Settings for the phyCORE-i.MX27 audio/touchscreen interface are in **bold blue**

14.3.7 USB Host

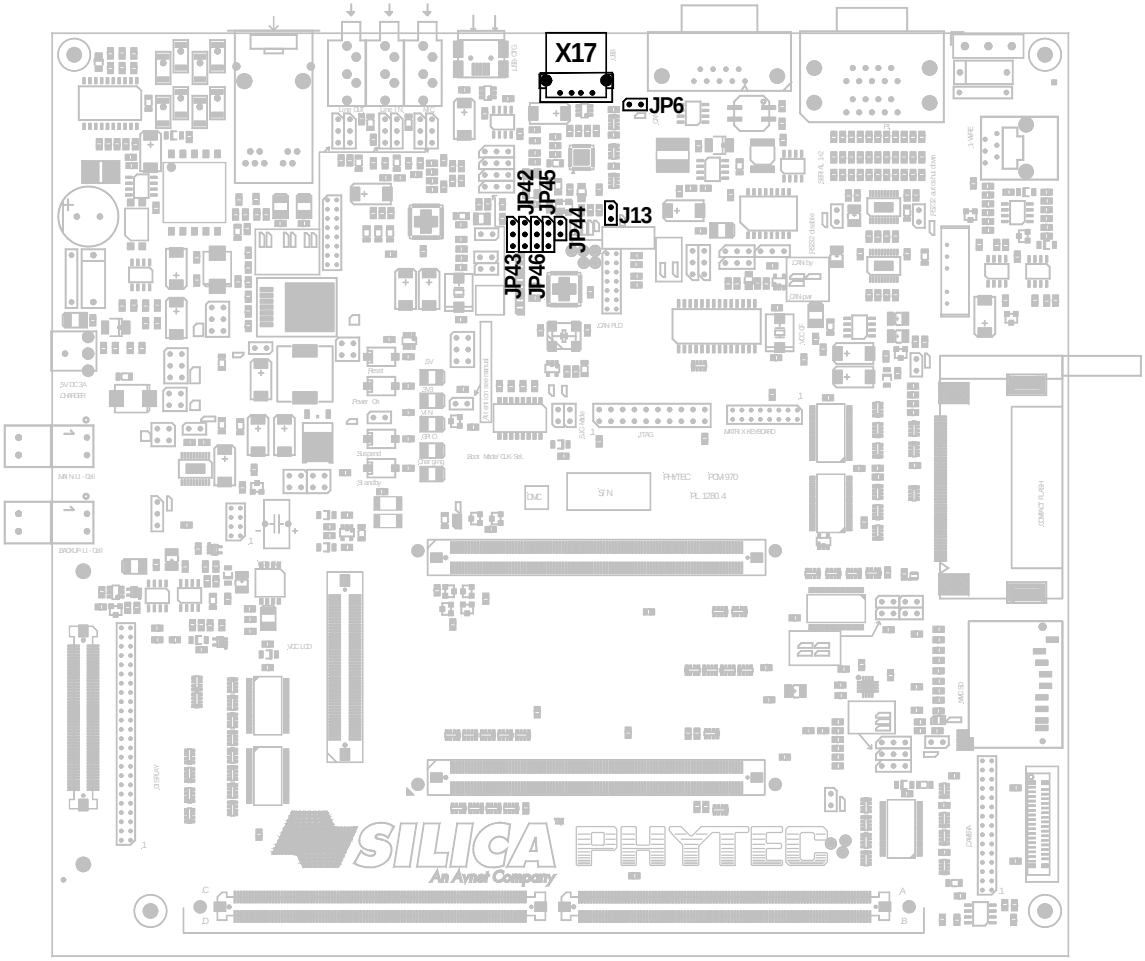

Figure 24: phyCORE-iMX Carrier Board USB-Host Interface

The i.MX27 controller supports control of input USB devices such as keyboard, mouse or USB key. To realize a USB Host interface the i.MX27 USB Host Controller (USBH2) uses the USB Host Transceiver (U26) of the i.MX Carrier Board.

For further details and jumper settings have a look at Table 29.

Table 29: UBS Host interface jumper settings for i.MX27 module[1]

JUMPER	SETTING	DESCRIPTION
JP13	open **closed**	USB Host transceiver U26 is disabled, USB Host is out of operation **USB Host transceiver U26 is active, USB Host is in operation**
JP6	**open** closed	**Reset pin is held HIGH, no Reset asserted** Reset pin is connected to GPIO, Reset can be asserted
JP42	**1+2** 2+3	**USB Host is managed on the i.MX baseboard** USB Host is managed on the i.MX module
JP43	**1+2** 2+3	**USB Host is managed on the i.MX baseboard** USB Host is managed on the i.MX module
JP44	open **closed**	USB Host is managed on the i.MX module **USB Host is managed on the i.MX baseboard**
JP45	**1+2** 2+3	**USB Host is managed on the i.MX baseboard** USB Host is managed on the i.MX module
JP46	**1+2** 2+3	**USB Host is managed on the i.MX baseboard** USB Host is managed on the i.MX module

Caution!
With the phyCORE-i.MX27 jumper JP6 and JP42 to JP46 always have to be set as described in the table above. The alternative functions of this jumpers are not available for the i.MX27 module.

1 Settings for the phyCORE-i.MX27 USB-Host interface are in **bold blue**

14.3.8 LCD Connectors

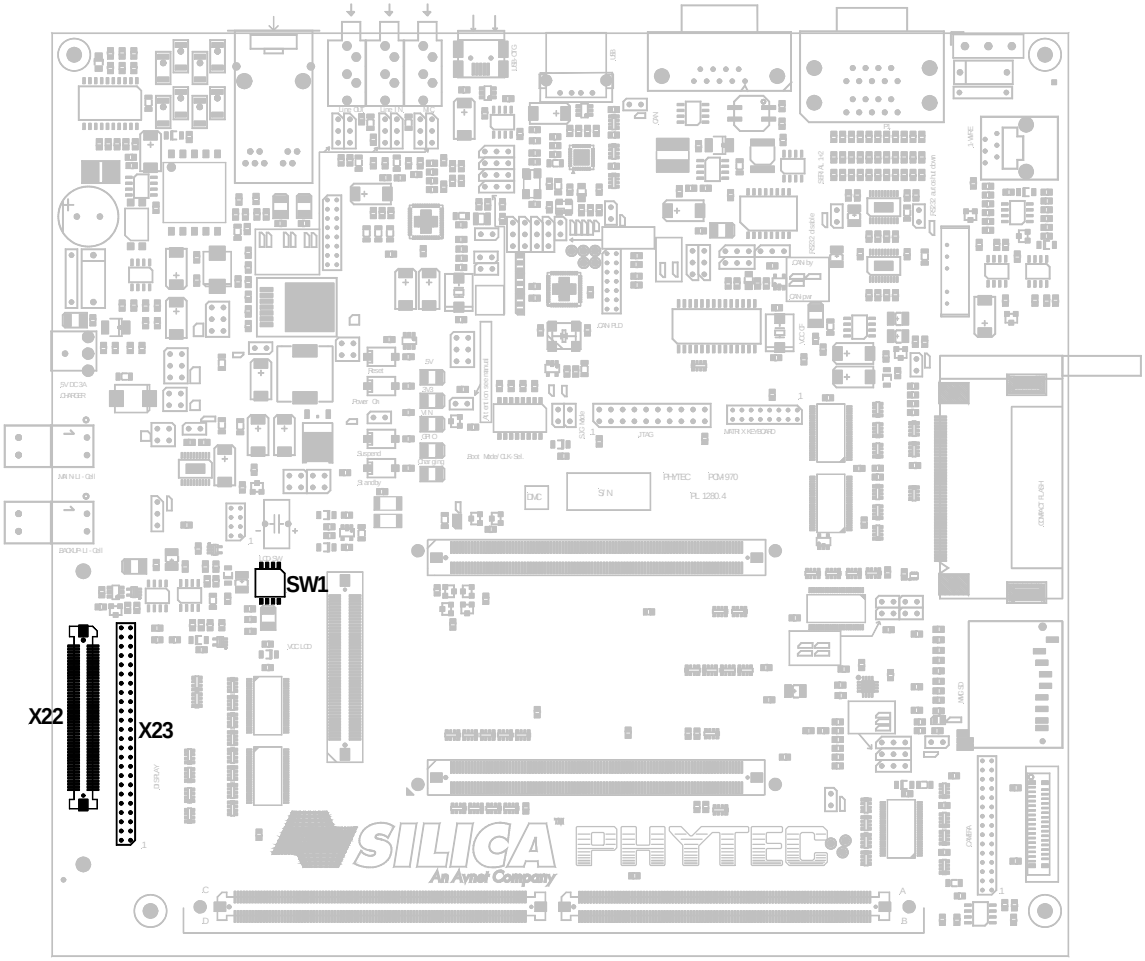

Figure 25: phyCORE-i.MX Carrier Board LCD Interfaces

The phyCORE-i.MX27 module comes with a 18-bit LCD interface. This 18-bit LCD interface is fully connected to the molex connectors X1 of the i.MX27 module and can be used in the customers application.

14.3.8.1 Serial LCD

Note:
Serial LCD is not supported by the phyCORE-i.MX27 module, because the i.MX27 microcontroller does not provide Serial LCD.

14.3.9 Camera Interface

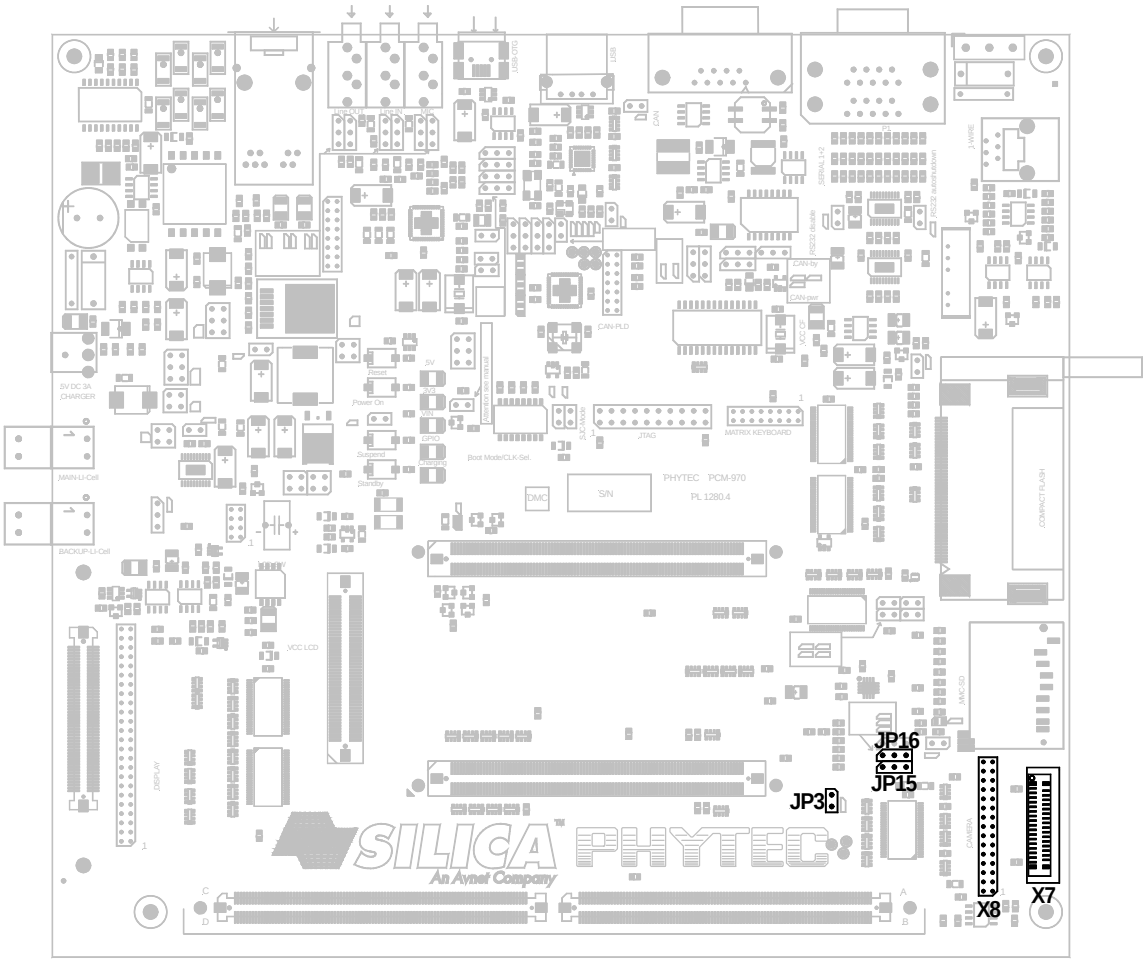

Figure 26: phyCORE-i.MX Carrier Board Camera Interface

The camera interface can be managed by the signal x_CSI_ENABLE connected to X_PB24 of the i.MX27 module.

Table 30: Camera interface jumper settings for i.MX27 module[1]

JUMPER	SETTING	DESCRIPTION
JP3	closed **open**	Outputs of level shifter U12 are enabled, CSI is active **Outputs of U12 are disabled or GPIO x_CSI_ENABLE (PB24 of i.MX27) can be used to control U12**
JP16	**1 + 2** 2 + 3	Jumper settings to chance camera sensor specific I²C address. *For more information refer to the manual of the used camera sensor.*
JP15	**1 + 2** 2 + 3	**Use of Camera Connector X7 with VCC_CAM supply (3.3V)** Use of Camera Connector X8 with external VCC_CAM_EXT supply

14.3.9.1 PHYTEC Camera Connector

Note:
i.MX27 only has an 8-bit camera interface so you need to have a Camera-Sensor with internal multiplexer. When ordering a Phytec Camera-Sensor, please consider to order a sensor with ordering option “MUX”.

1 Default Settings for the phyCORE-i.MX35 Camera Interface are in **bold blue**

14.3.10 JTAG Interface

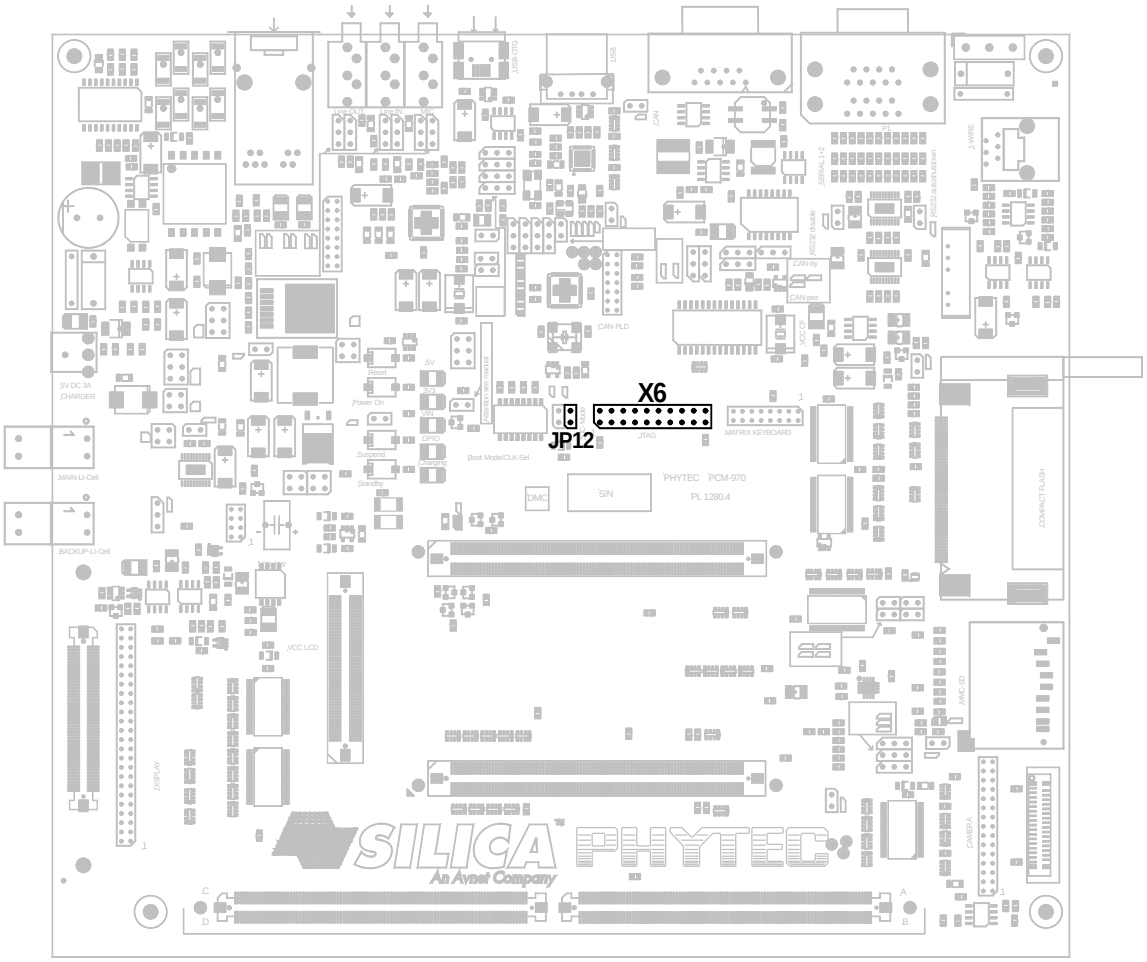

Figure 27: phyCORE-iMX Carrier Board JTAG Interface

Two JTAG modes are provided by the phyCORE-i.MX27 module dependent on the status of the JTAG_CTRL signal of the i.MX27 controller.
Jumper JP12 can be used to select the JTAG mode the controller should operate in.

Table 31: JTAG jumper settings for phyCORE-i.MX27 module[1]

JUMPER	SETTING	DESCRIPTION
JP12	**open** closed	**JTAG Controller is in ARM926 Platform mode** JTAG Controller is in i.MX27 JTAG Controller mode

1 Default Settings for the phyCORE-i.MX27 JTAG Interface are in **bold blue**

14.3.11 Complete jumper setting list for phyCORE-i.MX27 on the i.MX Carrier Board

The following table contains all jumper settings that can be set on the phyCORE-i.MX Carrier Board. Also it shows the default jumper settings for using the phyCORE-i.MX27 module with the i.MX Carrier Board. These default jumper settings are normally done prior to delivery.

Table 32: Jumper settings for i.MX27 module on i.MX Carrier Board[1]

JUMPER	SETTING	DESCRIPTION
JP1	**open**	**RS-232 transceivers are enabled**
	closed	RS-232 transceivers are disabled
JP2	**open**	**RS-232 auto shutdown is disabled**
	closed	RS-232 auto shutdown is enabled
JP3	**open**	**Camera interface is managed by x_CSI_ENABLE**
	closed	Camera interface is always enabled
JP4	open	Compact Flash is in overwrite mode
	closed	**Compact Flash is usable**
JP5	open	Compact-Flash is Slave
	closed	**Compact-Flash is Master**
JP6	**open**	**USBH2 transceiver Reset is not controllable**
	closed	USBH2 transceiver Reset is controllable via GPIO
JP7	**1+2**	**CAN is managed on the Carrier Board**
	2+3	CAN is managed on the module
JP8	1+2	CAN signals is are on the level VCC_CAN (from mapper)
	2+3	**CAN signals is are on the level VCC_5V**
JP9	**1+2**	**CAN is supplied via on Board 5 V Power-Supply**
	2+3	CAN is supplied via an external Power-Supply
JP10	**1+2**	**CAN is managed on the Carrier Board**
	2+3	CAN is managed on the module
JP11	**1+2**	**CAN is supplied via on Board Power-Supply**
	2+3	CAN is supplied via an external Power-Supply
JP12	**open**	**Only the System JTAG Controller**
	closed	All core's TAPS in a single daisy chain
JP13	open	USB Host transceiver is disabled
	closed	**USB Host transceiver is enabled**
JP14	**open**	**VCC_FUSE = 2.775 V (no FUSE programming)**
	closed	VCC_FUSE = 3,3V (use only for FUSE programming)
JP15	**1+2**	**Camera interface supplied via on-board 3.3 V supply**
	2+3	Camera interface is supplied via external supply
JP16	**1+2**	**CMOS-Sensor I²C address is 0x55**
	2+3	CMOS-Sensor I²C Address is 0x33
JP17	**open**	**Compact Flash expansion connector is enabled**
	closed	Compact Flash expansion connector is disabled

1 Default settings are in **bold blue**

JP18	1+2 **2+3**	MMC driver is disabled **MMC driver is enabled**
JP19	1+2 **2+3**	Stereo output is managed on the baseboard **Stereo output is managed on the module**
JP20	1+2 **2+3**	Stereo output is managed on the baseboard **Stereo output is managed on the module**
JP21	1+2 **2+3**	Stereo MIC is managed on the baseboard **Stereo MIC is managed on the module**
JP22	1+2 **2+3**	Stereo MIC is managed on the baseboard **Stereo MIC is managed on the module**
JP23	1+2 **2+3**	Stereo LINE IN is managed on the baseboard **Stereo LINE IN is managed on the module**
JP24	1+2 **2+3**	Stereo LINE IN is managed on the baseboard **Stereo LINE IN is managed on the module**
JP25	1+2 **2+3**	Touch screen is managed on the baseboard **Touch screen is managed on the module**
JP26	1+2 **2+3**	Touch screen is managed on the baseboard **Touch screen is managed on the module**
JP27	1+2 **2+3**	Touch screen is managed on the baseboard **Touch screen is managed on the module**
JP28	1+2 **2+3**	Touch screen is managed on the baseboard **Touch screen is managed on the module**
JP29	1+2 **2+3**	Backup voltage is supplied by ext. LICELL **Backup voltage is supplied by onboard Goldcap**
JP30	1+2 3+4 5+6	VCC_BOOT is deep-sleep test voltage VCC_CLK is deep-sleep test voltage VCC_JTAG is deep-sleep test voltage
JP31	1+3,2+4 **3+5,4+6**	Power source is Power Over Ethernet (POE) **Power source is 5 V adapter**
JP32	1+3,2+4 **3+5,4+6**	No power switching, direct supply of VCC_3V3 **Separate supply path**
JP33	1+2,3+4 **open,open**	No power switching, direct supply from VCC_3V3 **Separate supply path**
JP34	1+2,3+4 **open,open**	No power switching, direct supply from VCC_3V3 **Separate supply path**
JP35	**open** closed	**VCC_5V Power Supply is enabled** VCC_5V Power Supply is disabled
JP36	open **closed**	VCC_3V3 Power Supply is disabled **VCC_3V3 Power Supply is enabled**
JP37	open **closed**	Chargemode is Single Path **Chargemode is Dual Path**

JP38	**1+2,3+4** open,open	**Power switching, supply from 5 V adapter or POE** No power switching, direct supply from VCC_3V3
JP39	**1+2,3+4** open,open	**Power switching active, Battery charge path closed** No power switching, direct supply from VCC_3V3
JP40	open **closed**	No power switching active, minimum circuit **Power switching active**
JP42	**1+2** 2+3	**USB VBUS power enable managed on baseboard** USB VBUS power enable managed on module
JP43	**1+2** 2+3	**USB VBUS overcurrent managed on the baseboard** USB VBUS overcurrent managed on the module
JP44	open **closed**	USB Host is managed on the module **USB Host is managed on the baseboard**
JP45	**1+2** 2+3	**USB Host is managed on the baseboard** USB Host is managed on the module
JP46	**1+2** 2+3	**USB Host is managed on the baseboard** USB Host is managed on the module
JP47	**open** closed	**Reset of audio/touch device is not controllable** Reset of audio/touch device is controllable via GPIO
JP48	**open** closed	**IRQ of audio/touch device is not controllable** IRQ of audio/touch device is controllable via GPIO
JP49	**open** closed	**PENDOWN of audio/touch device is not controllable** PENDOWN of audio/touch device is controllable via GPIO
JP50	open **closed**	SD card write protect is not connected to the module **SD card write protect is connected to the module**
JP602	**open** closed	**PC_RW inverted** PC_RW non-inverted
JP604	open **closed**	CF power is manged by x_EXP007 **Force enabling VCC_CFL**

15 Revision History

Date	Version numbers	Changes in this manual
30-June-2009	Manual L-710e_4 PCM-038 PCB# 1281.2 PCM-970 PCB# 1280.4	Preliminary documentation. Describes the phyCORE-i.MX27 with phyMAP-i.MX27 and i.MX Carrier Board.
16-February-2011	Manual L-710e_5 PCM-038 PCB# 1281.4 PCM-970 PCB# 1280.4	Documentation Describes the phyCORE-i.MX27 with phyMAP-i.MX27 and i.MX Carrier Board.

16 Component Placement Diagram

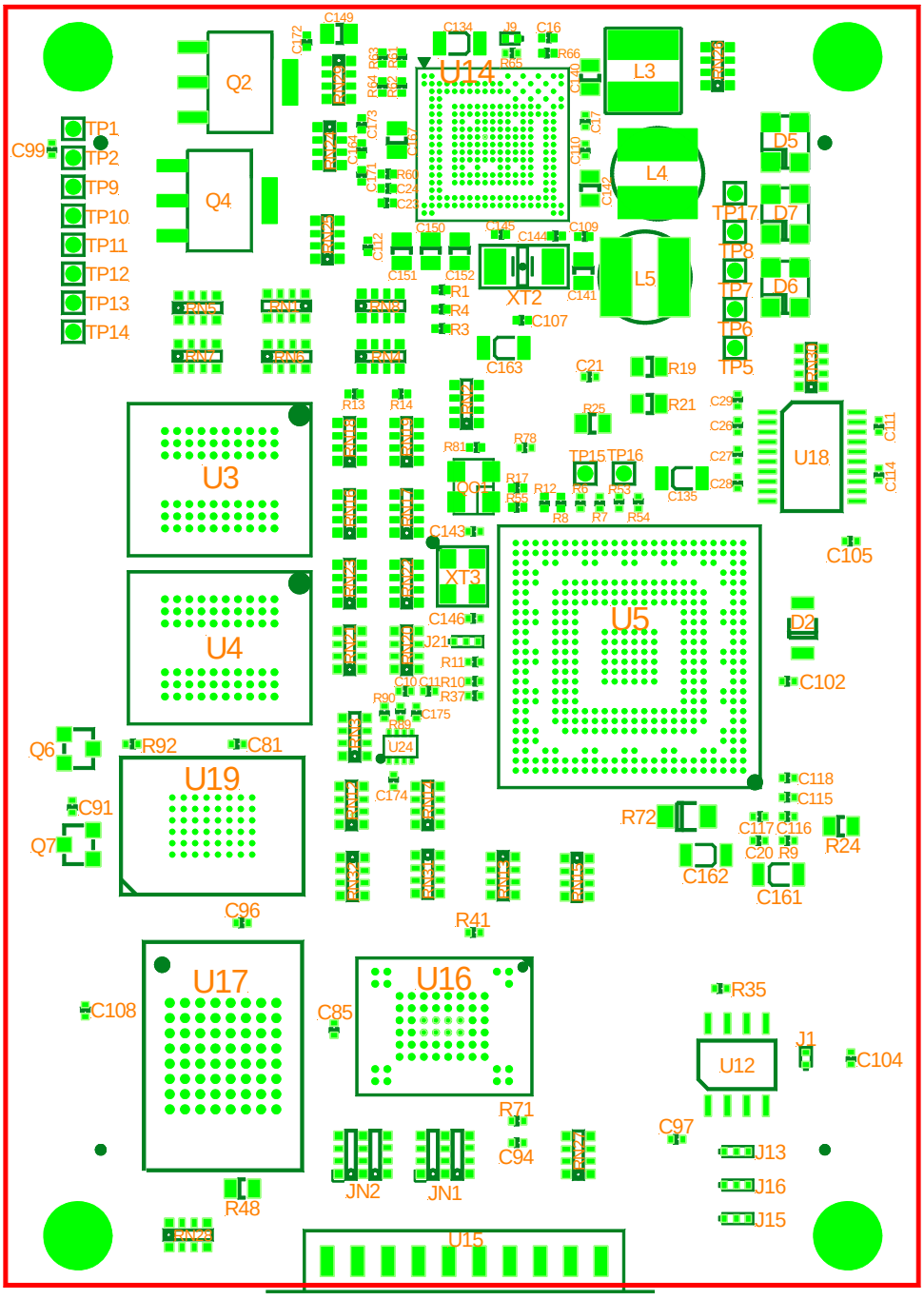

Figure 28: phyCORE-i.MX27 component placement (top view)

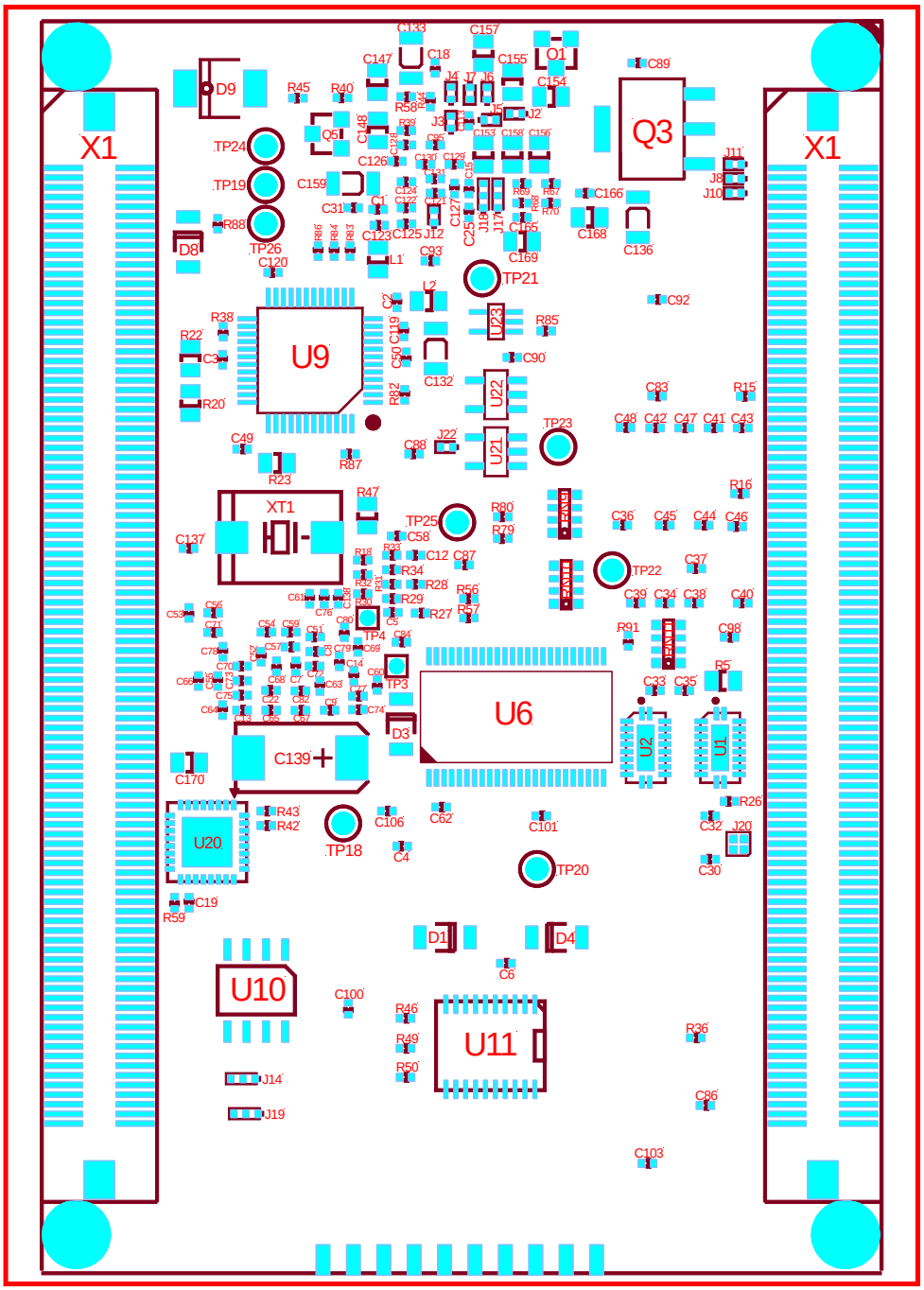

Figure 29: phyCORE-i.MX27 component placement (bottom view)

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Document number: **L-710e_5, February 2011**

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Return to:

PHYTEC Technologie Holding AG
Postfach 100403
D-55135 Mainz, Germany
Fax : +49 (6131) 9221-33

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