phyCORE-MPC5121e/3-tiny

Hardware Manual

Edition October 2009

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1st Edition October 2009

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Preface

This phyCORE-MPC5121e/3-tiny Hardware Manual describes the board's design and functions. Precise specifications for the Freescale MPC5121e/3 microcontroller series can be found in the enclosed MPC5121e/3B microcontroller Data Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic zero or low-level signal, while a "1" represents a logic one or high-level signal.

Default jumper settings for the appropriate hardware are denoted by a **bold** text in this hardware manual.

Declaration regarding Electro Magnetic Conformity of the PHYTEC phyCORE-MPC5121e/3-tiny

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Note:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header rows or connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-MPC5121e/3-tiny is one of a series of PHYTEC Single Board Computers that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports common 8-, 16- and numerous 32-bit controllers on two types of Single Boards Computers:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform
(2) as insert-ready, fully functional phyCORE OEM modules, which can be embedded directly into the user’s target design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market.

1 Introduction

The phyCORE-MPC5121e/3-tiny belongs to PHYTEC's phyCORE Single Board Computer module family. The phyCORE SBCs represent the continuous development of PHYTEC Single Board Computer technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a sub-miniature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments the phyCORE board design features an increased pin package. The increased pin package allows dedication of approximately 20 % of all pin header connectors on the phyCORE boards to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD components and laser-drilled microvias are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCORE-MPC5121e/3-tiny is a subminiature (76 x 60 mm^2) insert-ready Single Board Computer populated with Freescale’s PowerPC MPC5121e/3B microcontroller. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to high-density (0.635 mm) Molex pin header connectors aligning two sides of the board, allowing it to be plugged like a "big chip" into a target application.

Precise specifications for the controller populating the board can be found in the applicable controller Reference Manual or Data Sheet. The descriptions in this manual are based on the MPC5121e/3 controller. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCORE-MPC5121e/3-tiny.

The phyCORE-MPC5121e/3-tiny offers the following features:

- Single Board Computer in subminiature form factor (76 x 60 mm^2) according to phyCORE specifications
- all applicable controller and other logic signals extend to two high-density 160-pin Molex connectors
- processor: Freescale embedded PowerPC MPC5121e/3
- single 3.3 V (max. 1.2 A) supply voltage

Internal Features of the MPC5121e:

Major features of the MPC5121e are as follows:

• e300 Power Architecture processor core

- 760 MIPS at 400 MHz (-40 to +85 °C)
- 32 k instruction cache, 32 k data cache

• Power modes include doze, nap, sleep, deep sleep, and hibernate

• AXE – Auxiliary Execution Engine

• MBX Lite – 2D/3D graphics engine (not available in MPC5123)

• DIU – Display interface unit

• DDR1, DDR2, and LPDDR/mobile-DDR SDRAM memory

controller

- Multi port controller, listening on five incoming ports

• MEM – 128 Kbyte on-chip SRAM

• USB 2.0 OTG controller with integrated physical layer (PHY)

• DMA subsystem

- EMB – Flexible multi-function external memory bus interface
- NFC – NAND flash controller
- LPC – LocalPlus interface
- FEC – Fast Ethernet controller
  - Supports 100Mbps IEEE 802.3 MII, 10 Mbps IEEE 802.3 MII
- PCI interface, version 2.3
- PATA – Parallel ATA integrated development environment (IDE) controller
- SATA – Serial ATA controller with integrated physical layer (PHY)
- SDHC – MMC/SD/SDIO card host controller
- PSC – 12 programmable serial controllers
  - configurable for the following protocols: UART, Codec/PCM, serial audio data, I2S, multi-channel data, SPI, and AC97
- I^2C – 3 inter-integrated circuit communication interfaces
- S/PDIF – Serial audio interface
- CAN – Controller area network
  - Implementation of CAN protocol, version 2.0 A/B
- BDLC – J1850 interface
- VIU – Video Input, ITU-656 complient
- RTC – On-Chip real-time clock
- On-chip temperature sensor
- IIM – IC Identification module
- IEEE 1149.1 compliant JTAG boundary scan

Memory Configuration[1]:

[1]: Please contact PHYTEC for more information about additional module configurations.

- DDR2 SDRAM: 128 MByte to 512 MByte
- Flash: 16 MByte to 32 MByte Intel Strata Flash memory, 16-bit memory width, only asynchronous devices are supported
- Battery bufferable SRAM: 1MByte to 2MByte
- I²C memory: 4 kByte EEPROM

Other Board-Level Features:

- Two UART ports, RS-232 interfaces (RxD/TxD)
- One 10/100Mbit Ethernet port via optional Micrel PHY
- I²C Real-Time Clock with calendar and alarm function
- Optional industrial temperature range (-40…+85°C)
- On board Watchdog
- On board Reset Logic

1.1 Block Diagram

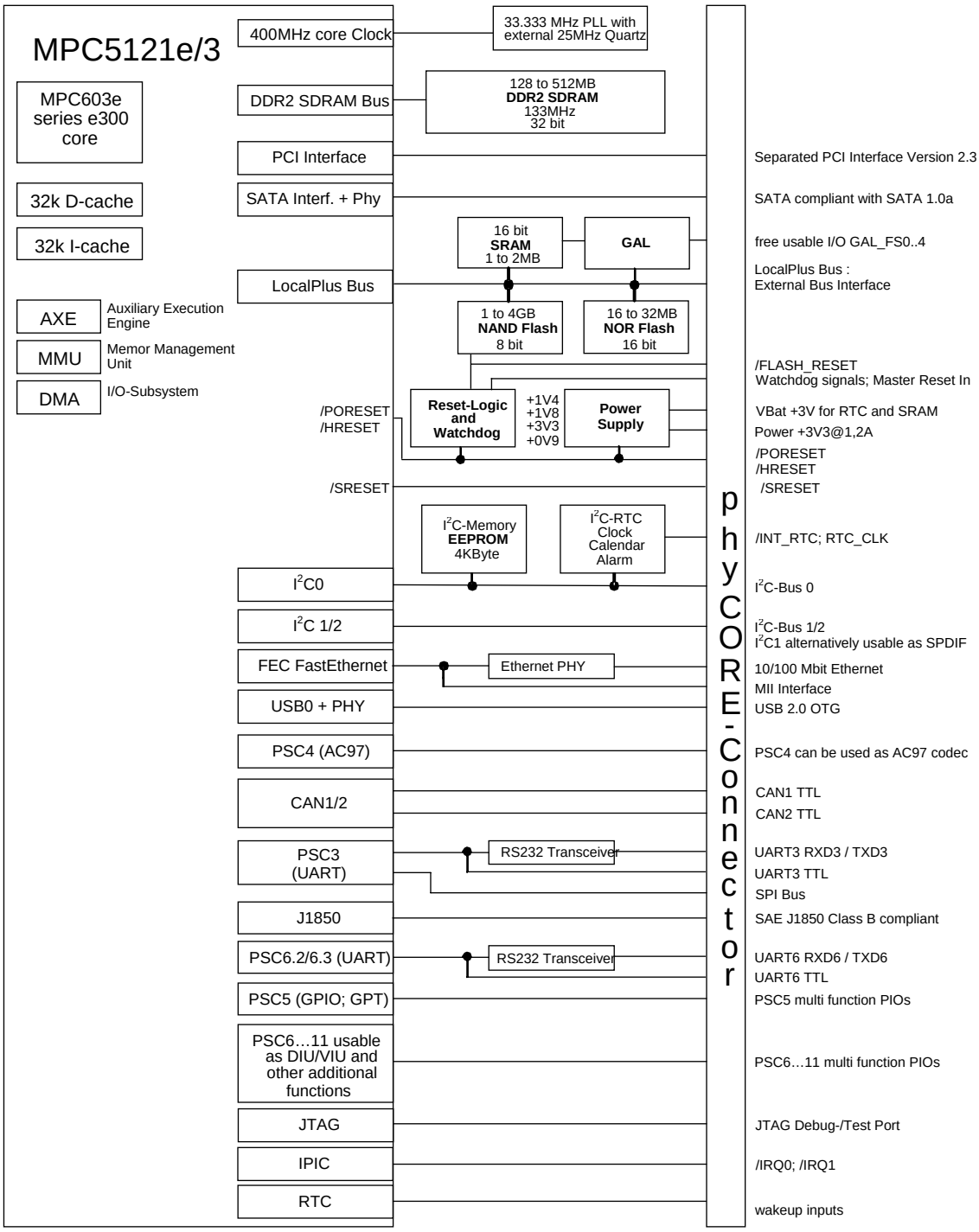


Figure 1: Block Diagram phyCORE-MPC5121e/3- tiny

1.2 View of the phyCORE-MPC5121e/3-tiny

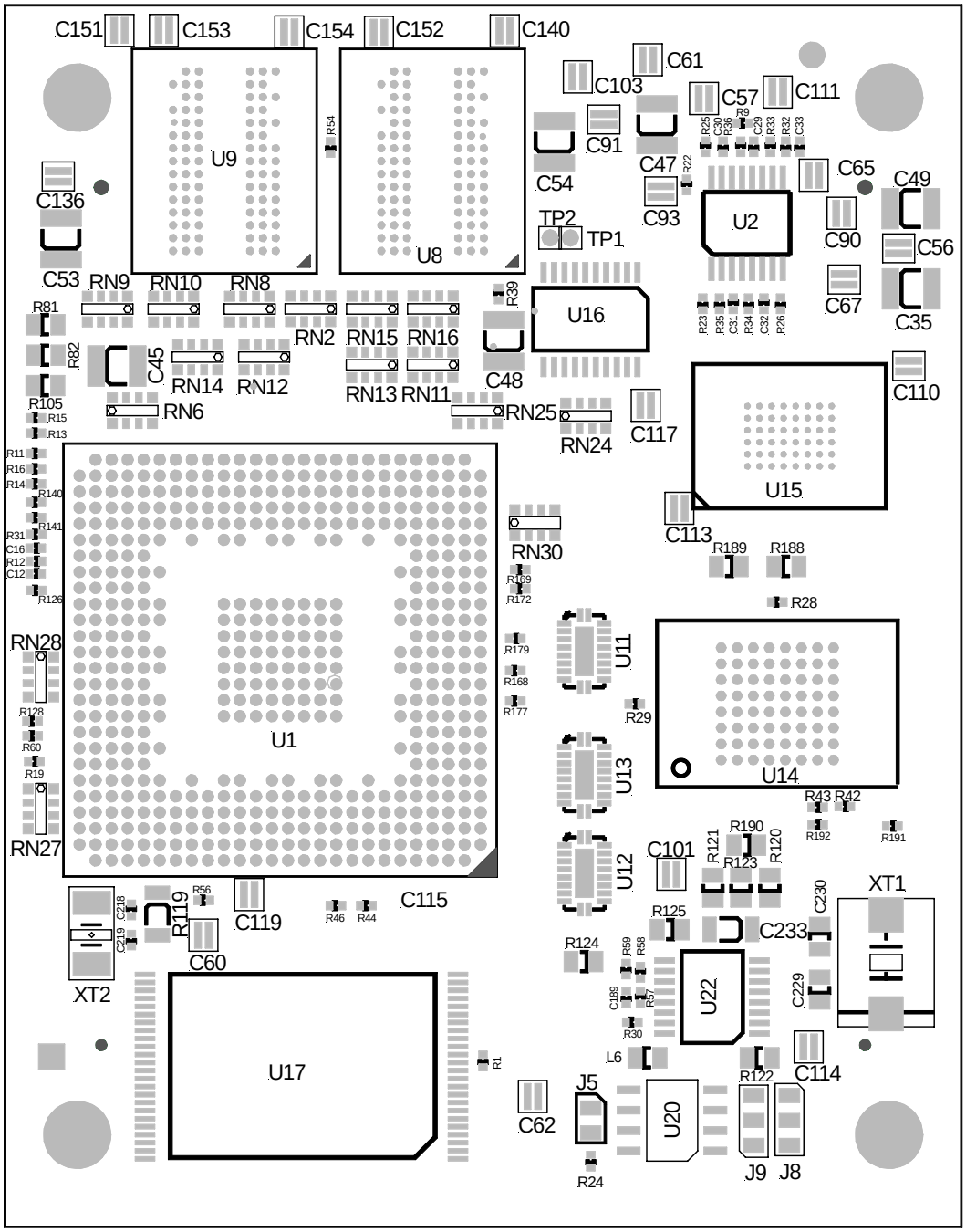


Figure 2: Top-View of the phyCORE-MPC5121e/3-tiny PCB Rev. 1326.1

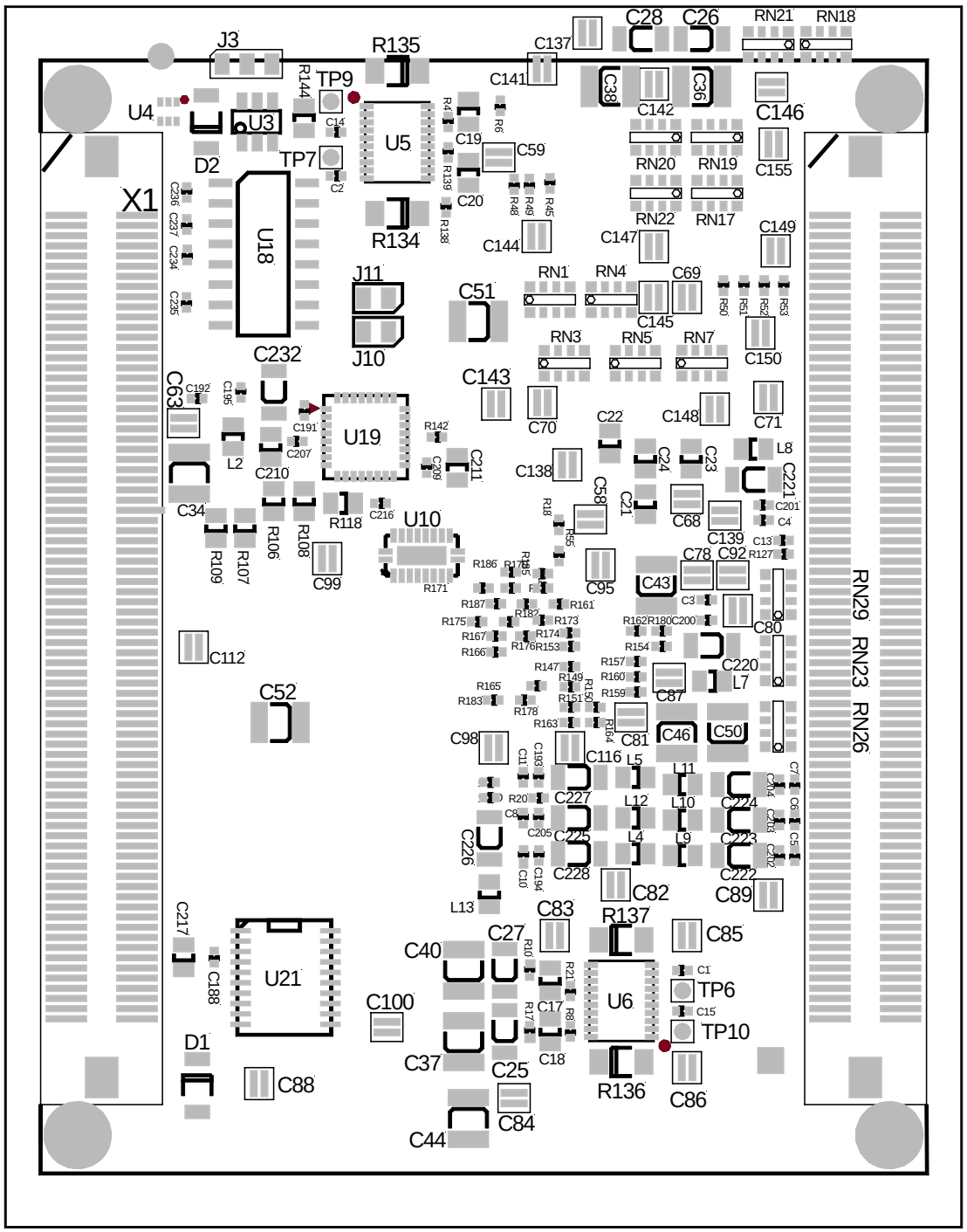


Figure 3: Bottom-View of the phyCORE-MPC5121e/3-tiny PCB Rev. 1326.1

1.3 Minimum Requirements to Operate the phyCORE-MPC5121e/3-tiny

Basic operation of the phyCORE-MPC5121e/3-tiny only requires supply of a +3V3 input voltage and the corresponding GND connection.

These supply pins are located at the phyCORE-Connector X1:

VCC +3V3:
X1 1C, 2C, 4C, 5C, 1D, 2D, 4D, 5D

corresponding GND:
X1 3C, 3D, 7C, 9D, 12C, 14D, 17D, 19C
Please refer to section 2 for information on additional GND Pins located at the phyCORE-Connector X1

Caution:
We recommend connecting all available +3V3 input pins to the power supply system on a custom carrier board housing the phyCORE-MPC5121e/3-tiny and at least the matching number of GND pins neighboring the +3V3 pins.

In addition, proper implementation of the phyCORE module into a target application also requires connecting all GND pins neighboring signals that are being used in the application circuitry.

Please refer to section 4 for more information.

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

All controller signals extend to surface mount technology (SMT) connectors (0.635 mm) lining two sides of the module (referred to as the phyCORE-Connector). This allows the phyCORE-MPC5121e/3-tiny to be plugged into any target application like a "big chip".

The numbering scheme for the phyCORE-Connector is based on a two dimensional matrix in which column positions are identified by a letter and row position by a number. Pin 1A, for example, is always located in the upper left hand corner of the matrix. The pin numbering values increase moving down on the board. Lettering of the pin connector rows progresses alphabetically from left to right (refer to Figure 4).

The numbered matrix can be aligned with the phyCORE-MPC5121e/3-tiny (viewed from above; phyCORE-Connector pointing down) or with the socket of the corresponding phyCORE Carrier Board/user target circuitry. The upper left-hand corner of the numbered matrix (pin 1A) is thus covered with the corner of the phyCORx-MPC5121e/3-tiny marked with a white triangle. The numbering scheme is always in relation to the PCB as viewed from above, even if all connector contacts extend to the bottom of the module.

The numbering scheme is thus consistent for both the module’s phyCORE-Connector as well as making connectors on the phyCORE Carrier Board or target hardware, thereby considerably reducing the risk of pin identification errors.

Since the pins are exactly defined according to the numbered matrix previously described, the phyCORE-Connector is usually assigned a single designator for its position (X1 for example). In this manner the phyCORE-Connector comprises a single, logical unit regardless of the fact that it could consist of more than one physical socketed connector. The location of row 1 on the board is marked by a white triangle on the PCB to allow easy identification.

Figure 4 illustrates the numbered matrix system. It shows a phyCORE-MPC5121e/3-tiny with SMT phyCORE-Connectors on its underside (defined as dotted lines) mounted on a Carrier board. In order to facilitate understanding of the pin assignment scheme, the diagram presents a cross-view of the phyCORE module showing these phyCORE-Connectors mounted on the underside of the module's PCB.

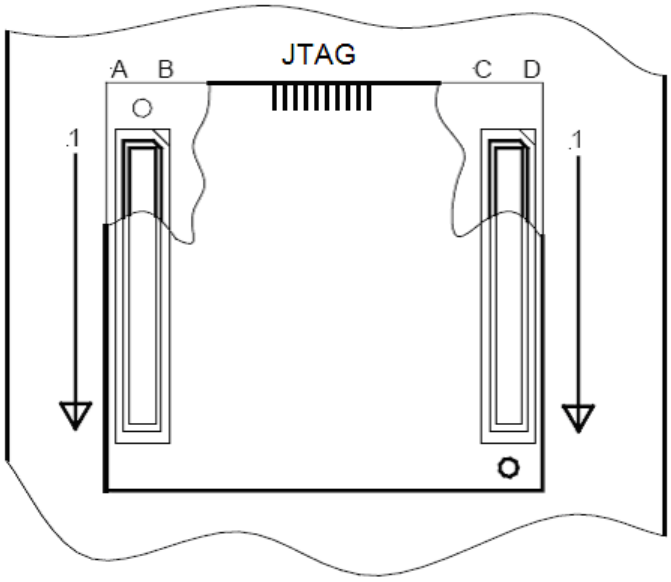


Figure 4: Pinout of the phyCORE-MPC5121e/3-tiny (Top View, with Cross Section insert)

Many of the phyCORE-MPC5121e/3-tiny pins offer alternative functions. These alternative functions must be activated by configuring the applicable controller registers prior to their use. Certain controller functions are pre-configured based on the module's

design and are shown in *Table 1*. Signals that are routed directly from the CPU to the Molex connectors can be configured to any available alternative function desired by the user. In contrast, signals that are used on the phyCORE-MPC5121e/3-tiny as listed in *Table 1* can only be used if a special module configuration was purchased (e.g. SBC version without on-board RS-232 transceivers. Please contact PHYTEC for more details).

Note:
The following sections of this manual assume use of the port pins according to configuration listed in *Table 1*.
Use of the phyCORE-MPC5121e/3-tiny Carrier Board reduces the number of alternative functions freely available (*Please refer to section 14.3.1 for more information.*)

CPU Port	Function	Used on phyCORE SBC
PSC0,1,2	Ethernet	Yes
PSC3	UART3	Yes
PSC4	AC97	No
PSC5	GPIO	No
PSC6	UART6/DIU	Yes
PSC7...11	DIU	No
USB	USB OTG	No
CAN	dedicated	No
J1850	dedicated	No
I2C0	dedicated	Yes
I2C1 / I2C2	dedicated	No

Table 1: Default Port Configuration

Table 2 provides an overview of the pinout of the phyCORE-Connector.

Please refer to the Freescale MPC5121e/3 Reference Manual/Data Sheet for details on the functions and features of controller signals and port pins.

Pin Number	Signal	I/O	Comments
Pin Row X1A			
1A	/INT_RTC	O	RTC Interrupt
2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A 67A, 72A, 77A	GND	-	Ground 0 V
3A	/IRQ1	I	Interrupt input 1 of the processor.
4A, 38A, 39A, 44A, 45A	NC	-	not connected
			LocalPlus Bus control signals
5A	/LPC_CS1	O	Chip Select 1
6A	/LPC_OE	O	Out Enable
8A	/LPC_ACK	I	Acknowledge
9A	EMB_AX1	O	used as signal Tsiz0 in muxed mode
10A	EMB_AX0	O	used as ALE signal in muxed mode
			LocalPlus Bus, multiplexed Address/Data Signals
11A	EMB_AD2	I/O	
13A	EMB_AD4		
14A	EMB_AD6		
15A	EMB_AD7		
16A	EMB_AD9		
18A	EMB_AD12		
19A	EMB_AD14		
20A	EMB_AD15		
21A	EMB_AD17		
23A	EMB_AD20		
24A	EMB_AD22		
25A	EMB_AD23		
26A	EMB_AD25		
28A	EMB_AD28		
29A	EMB_AD30		
30A	EMB_AD31		
31A	GPIO29	I	GPIO wake-up input
			Parallel ATA Interface Signals
33A	PATA_IOCHRDY	O	ATA negated to extend transfer
34A	PATA_INTRQ	I	ATA interrupt request
35A	PATA_DRQ	I	ATA DMA request
36A	/PATA_DACK	O	ATA DMA acknowledge
			Serial ATA Interface Signals
40A	SATA_RXP	I	Receiver positive differential pair input.
41A	/SATA_RXN	I	Receiver negative differential pair input.
43A	/PHY_INTR	O	Interrupt signal of the on-board Ethernet PHY

Pin Number	Signal	I/O	Comments
			Dedicated PCI Signals
46A	/PCI_INTA	O	PCI Interrupt output of the processor
48A	/PCI_GNT2	I/O	Bus grant 2
49A	/PCI_REQ2	I/O	Bus request
50A	/PCI_RST_OUT	O	Bus reset
51A	/PCI_GNT0	I/O	Bus grant 0
53A	PCI_AD31	I/O	PCI Address/Data signal
54A	PCI_AD29	I/O	"
55A	PCI_AD28	I/O	"
56A	PCI_AD26	I/O	"
58A	/PCI_CBE3	I/O	Command byte enable 3
59A	PCI_AD23	I/O	PCI Address/Data signal
60A	PCI_AD22	I/O	"
61A	PCI_AD20	I/O	"
63A	PCI_AD17	I/O	"
64A	/PCI_CBE2	I/O	Command byte enable 2
65A	/PCI_IRDY	I/O	Initiator (HOST) ready
66A	/PCI_DEVSEL	I/O	Device select
68A	/PCI_PERR	I/O	Parity error
69A	/PCI_SERR	I/O	System Error (open drain)
70A	/PCI_CBE1	I/O	Command byte enable 1
71A	PCI_AD14	I/O	PCI Address/Data signal
73A	PCI_AD11	I/O	"
74A	PCI_AD9	I/O	"
75A	PCI_AD8	I/O	"
76A	PCI_AD7	I/O	"
78A	PCI_AD4	I/O	"
79A	PCI_AD2	I/O	"
80A	PCI_AD1	I/O	"

Pin Number	Signal	I/O	Comments
Pin Row X1B			
1B	CLK_RTC	O	Clock output of the I²C RTC U5
2B	/IRQ0	I	Interrupt input 0 of the processor
3B	LPC_CLK	O	Clock output of the processor for EMB Bus
4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 51B, 54B, 59B, 64B, 69B, 74B, 79B	GND		Ground 0 V
			LocalPlus Bus Signals
5B	/LPC_CS2	O	Chip Select 2
6B	LPC_RNW	O	Read, not Write
7B	LPC_AX3	O	used as /TransferStart signal in muxed mode
8B	EMB_AX2	O	used as Tsiz1 Signal in muxed mode
		I/O	***LocalPlus Address/Data Signals***
10B	EMB_AD0		
11B	EMB_AD1		
12B	EMB_AD3		
13B	EMB_AD5		
15B	EMB_AD8		
16B	EMB_AD10		
17B	EMB_AD11		
18B	EMB_AD13		
20B	EMB_AD16		
21B	EMB_AD18		
22B	EMB_AD19		
23B	EMB_AD21		
25B	EMB_AD24		
26B	EMB_AD26		
27B	EMB_AD27		
28B	EMB_AD29		
30B	GPIO28	I	GPI Wake up signals
31B	GPIO30		
32B	GPIO31		
33B, 41B, 42B	NC	-	not connected
			Parallel ATA Interface Signals
35B	/PATA_CE1	I	Chip enable 1 signal
36B	/PATA_CE2		Chip enable 2 signal
37B	PATA_ISOLATE		Isolation strobe signal
38B	/PATA_IOR		Read strobe signal
40B	/PATA_IOW		Write strobe signal
			Serial ATA Interface Signals
43B	SATA_ANAVIZ	O	Analog test output
45B	SATA_TXP	O	Transmitter positive differential pair output
46B	/SATA_TXN	O	Transmitter negative differential pair output

Pin Number	Signal	I/O	Comments
			Dedicated PCI Signals
47B	/PCI_GNT1	I/O	
48B	/PCI_REQ1	I/O	PCI bus request 1
50B	PCI_CLK	O	PCI and external peripheral clock
52B	/PCI_REQ0	I/O	PCI bus request 0
53B	PCI_AD30	I/O	PCI Address/Data signal
55B	PCI_AD27	I/O	"
56B	PCI_AD25	I/O	"
57B	PCI_AD24	I/O	"
58B	PCI_IDSEL	I	Initial device select
60B	PCI_AD21	I/O	PCI Address/Data signal
61B	PCI_AD19	I/O	"
62B	PCI_AD18	I/O	"
63B	PCI_AD16	I/O	"
65B	/PCI_FRAME	I/O	Frame start
66B	/PCI_TRDY	I/O	Target ready
67B	/PCI_STOP	I/O	Transition stop
68B	PCI_PAR	I/O	Bus parity
70B	PCI_AD15	I/O	PCI Address/Data signal
71B	PCI_AD13	I/O	"
72B	PCI_AD12	I/O	"
73B	PCI_AD10	I/O	"
75B	/PCI_CBE0	I/O	Command byte enable 0
76B	PCI_AD6	I/O	PCI Address/Data signal
77B	PCI_AD5	I/O	"
78B	PCI_AD3	I/O	"
80B	PCI_AD0	I/O	"

Pin Number	Signal	I/O	Comments
Pin Row X1C			
1C, 2C, 4C, 5C	+3V3	I	Supply voltage +3.3 VDC
3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 72C, 77C	GND	-	Ground 0 V
46C, 48C	NC	-	not connected
6C	VBAT	I	Connection for external battery (+) 2.4 - 3.3 V to supply (backup) the RTC U5
8C	/WDO	O	Watchdog output (with weak pull-up) of the supply monitor at U2
9C	/FL_WP	I	Write protection of the NOR-Flash at U14
10C	/SRESET	I/O	External SRESET is an open drain signal which is connected to a 3,3 kOhm pull-up resistor on the module. Assertion of SRESET causes assertion of the internal soft reset. Internal soft reset is actually an interrupt that takes the same exception vector as HRESET. In particular, this means that SRESET cannot abort a hung XLB operation, and no device should use SRESET in a way that interferes with any bus operation in progress. SRESET can also be asserted by internal sources. When SRESET is asserted internally, external SRESET is also asserted.
11C	/HRESET	I/O	HRESET is a bi-directional signal with a Schmitt-trigger input and an open drain output. The HRESET signal is connected a 3,3 kOhm pull-up resistor on the module. Assertion of external HRESET causes external HRESET and SRESET as well as internal hard and soft resets to be asserted for at least 4096 reference clock cycles. During PORRESET or HRESET the reset configuration word is sampled to establish the initial state of various vital internal MPC5121e/3 functions. The reset configuration word is latched internally when PORRESET or HRESET is released.
			PSC4 (AC97 Interface signals)
13C	PSC4_4	O	Reset signal to the external AC97 device
14C	PSC4_1	O	Frame sync, or start-of-frame (SOF)
15C	PSC4_0	I	Driven by the external serial bit-clock
16C	PSC4_3	I	Receiver serial data input
18C	CAN2_TX	O	CAN transmit output of the second CAN interface
19C	PSC6_3_RXD	I	PSC6 receive data input of the MPC UART6. Can be disconnected from the RS-232 transceiver U18 with J10

Pin Number	Signal	I/O	Comments
20C	PSC6_2_TXD	O	PSC6 transmit data output of the MPC UART6 to the RS-232 transceiver U18
21C	RXD6_RS232	I	RxD input of the RS-232 transceiver U18 for MPC UART6 (PSC6_3)
23C	TXD6_RS232	O	TxD output of the RS-232 transceiver U18 for MPC UART (PSC6_2)
24C	J1850_TX	O	Transmit output channel for BDLC module
25C	J1850_RX	I	Receive input channel for BDLC module
			Second I²C Interface
26C	I2C1_SCL	I/O	Clock of the second I2C-Interface
28C	I2C1_SDA	I/O	Data of the second I2C Interface
29C	PSC5_0	I/O	PSC5 bit 0 of the MPC5121e/3
30C	PSC5_2	I/O	PSC5 bit 2 of the MPC5121e/3
31C	I2C0_SCL	I/O	Clock of first I2C-Interface
			10/100MBit TP Ethernet Interface (if on-board PHY is not populated, pins are NC)
33C	ETH_LED0	O	Link/Activity LED (L=link; toggle=act)
34C	ETH_LED1	O	Speed LED (H=10 Mbit/s, L=100 Mbit/s)
35C	ETH_RX-	I	Differential receive input
36C	ETH_TX-	O	Differential transmit output
38C	/PHY_INTR	I	Interrupt output of the Ethernet PHY
			JTAG Interface
39C	/JTAG_TRST	I	JTAG reset input. Via logic OR connected to /PORRESET resulting in /CPU_TRST signal.
40C	/JTAG_CKSTP_O	O	JTAG clock stop
			USB (OTG Interface signals)
41C	USB_PWRFAULT	I	
43C	USB_DP	I/O	
44C	USB_DM	I/O	
45C	USB_DRVVBUS	O	
			MII-Interface signals
49C	FEC_CRS	I	Carrier sense input
50C	FEC_COL	I	collision input
51C	FEC_TXD_1	O	transmit data bit 1 output
53C	FEC_TX_EN	O	transmit data valid output
54C	FEC_TX_ER	O	transmit error output
55C	FEC_RXD_3	I	receive data bit 3 input
56C	FEC_RXD_2	I	receive data bit 2 input
58C	FEC_RX_ER	I	receive error input
59C	FEC_MDC	O	management clock output
			free available GAL signals (programming dependent)
60C	GAL_FS0	I/O	free usable IO signal
61C	GAL_FS1	I/O	free usable IO signal
63C	GAL_FS4	I/O	free usable IO signal

Pin Number	Signal	I/O	Comments
			PSC6...11 signals (DIU Interface signals)
64C	PSC6_0	O	DIU Clock signal
65C	PSC6_4	O	DIU VSYNC signal
66C	PSC7_1	O	DIU red bit 6
68C	PSC7_3	O	DIU red bit 0
69C	PSC8_0	O	DIU green bit 0
70C	PSC8_2	O	DIU blue bit 0
71C	PSC8_4	O	DIU blue bit 3
73C	PSC9_0	O	DIU blue bit 4
74C	PSC9_2	O	DIU blue bit 6
75C	PSC10_0	O	DIU green bit 3
76C	PSC10_2	O	DIU green bit 5
78C	PSC10_3	O	DIU green bit 6
79C	PSC11_0	O	DIU red bit 2
80C	PSC11_3	O	DIU red bit 5

Pin Number	Signal	I/O	Comments
Pin Row X1D			
1D, 2D, 4D, 5D	+3V3	I	Supply voltage +3.3 VDC
3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D, 74D, 79D	GND	-	Ground 0 V
37D, 47D, 48D	NC	-	Not connected
6D	VDD_SRAM_V3V3	O	VCC_SRAM supply voltage is generated by VBAT or +3V3 using a battery backup circuit (MAX6364). VDD_SRAM_V3V3 serves as supply voltage for the on-board Real-Time Clock (U21), the on-chip Real-Time Clock of the MPC512x and the battery buffered SRAM.
7D	/HIB_MODE	I	hibernate mode input of the processor
8D	WDI	I	trigger input for the on-board watchdog LTC2901IGN
10D	/MR_IN	I	Master reset input signal of the phyCORE-MPC5121e/3-tiny. It could be asserted via connection to a reset push button. Signal connected to +3V3 via 4,7 kOhm pull-up resistor.
11D	/FLASH_RESET	O	Signal for resetting on-board/off-board Flashes, generated on-board by a logic depending on the signals /HRESET and /PORESET
12D	/PORESET	O	Power on reset output of the on-board reset supervisor
			PSC4 (AC97 Interface signal)
13D	PSC4_2	O	Receiver serial data output
15D	PSC3_4	I/O	PSC3 general purpose IO
16D	PSC3_3_RXD	I	PSC3 receive data input of the MPC UART6. Can be disconnected from the RS-232 transceiver U18 with J11
17D	PSC3_2_TXD	O	PSC3 transmit data output of the MPC UART6 to the RS-232 transceiver U18
18D	CAN2_RX	I	CAN receive of the second CAN interface
20D	CAN1_RX	I	CAN receive of the first CAN interface
21D	CAN1_TX	O	CAN transmit of the first CAN interface
22D	RXD3_RS232	I	RxD input of the RS-232 transceiver U18 for MPC UART3 (PSC3_3)
23D	TXD3_RS232	O	TxD output of the RS-232 transceiver U18 for MPC UART3 (PSC3_2).
25D	PSC3_0	O	PSC3 request to send signal
26D	PSC3_1	I	PCS3 clear to send signal
			I2C Interfaces
27D	I2C2_SCL	O	Clock of third I2C interface
28D	I2C2_SDA	I/O	Data of third I2C interface
32D	I2C0_SDA	I/O	Data of first I2C interface

30D	PSC5_1	I/O	PSC5 general purpose IO bit 1
31D	PSC5_3	I/O	PSC5 general purpose IO bit 3
33D	PSC5_4	I/O	PSC5 general purpose IO bit 4
			10/100MBit TP Ethernet Interface (if on-board PHY is not populated, pins are* NC0*)
35D	ETH_RX+	I	Differential receive input
36D	ETH_TX+	O	Differential transmit output
			MPC5121e/3 JTAG interface
38D	JTAG_TCK	I	Clock
40D	JTAG_TDI	I	Data in
41D	JTAG_TDO	O	Data out
42D	JTAG_TMS	I	Mode select
			USB OTG Interface signals
43D	USB_TPA	O	Analog output of the USB-OTG interfaces – should be left unconnected
45D	USB_VBUS	I/O	Analog IO of the USB-OTG interface - bus voltage reference
46D	USB_UID	I	Analog input of the USB-OTG interface – universal ID input
			MII-interface signals
50D	FEC_TXD_3	O	transmit data bit 3 output
51D	FEC_TXD_2	O	transmit data bit 2 output
52D	FEC_TXD_0	O	transmit data bit 0 output
53D	FEC_TX_CLK	I	transmit clock input
55D	FEC_RX_DV	I	receive data valid input
56D	FEC_RXD_1	I	receive data bit 1 input
57D	FEC_RXD_0	I	receive data bit 0 input
58D	FEC_RX_CLK	I	receive clock input
60D	FEC_MDIO	I/O	bidirectional management data
			free available GAL signals (programming dependent)
61D	GAL_FS2	I/O	free usable IO signal
62D	GAL_FS3	I/O	free usable IO signal
			PSC6...11 signals (DIU Interface signals)
63D	PSC6_1	O	DIU HSYNC signal
65D	PSC7_0	O	DIU red bit 7
66D	PSC7_2	O	DIU red bit 1
67D	PSC7_4	O	DIU green bit 1
68D	PSC8_1	O	DIU blue bit 1
70D	PSC8_3	O	DIU blue bit 2
71D	PSC9_1	O	DIU blue bit 5
72D	PSC9_3	O	DIU blue bit 7
73D	PSC9_4	O	DIU green bit 2
75D	PSC10_1	O	DIU green bit 4
76D	PSC10_4	O	DIU green bit 7
77D	PSC11_1	O	DIU red bit 3
78D	PSC11_2	O	DIU red bit 4
80D	PSC11_4		DIU ENABLE

Table 2: Pinout of the phyCORE-Connector X1

3 Jumpers

For configuration purposes, the phyCORE-MPC5121e/3-tiny has 6 solder jumpers, some of which have been installed prior to delivery. ***Fehler! Verweisquelle konnte nicht gefunden werden.*** illustrates the numbering of the jumper pads, while and *Figure 7* indicate the location of the solder jumpers on the board. There are 3 solder jumpers located on the top side of the module (opposite side of connectors) and 3 solder jumpers on the bottom side.

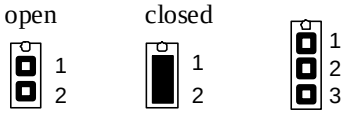


Figure 5: Numbering of the Jumper Pads

All jumpers are 0805 package with a 1/8W or better power rating.

If manual jumper modification is required please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

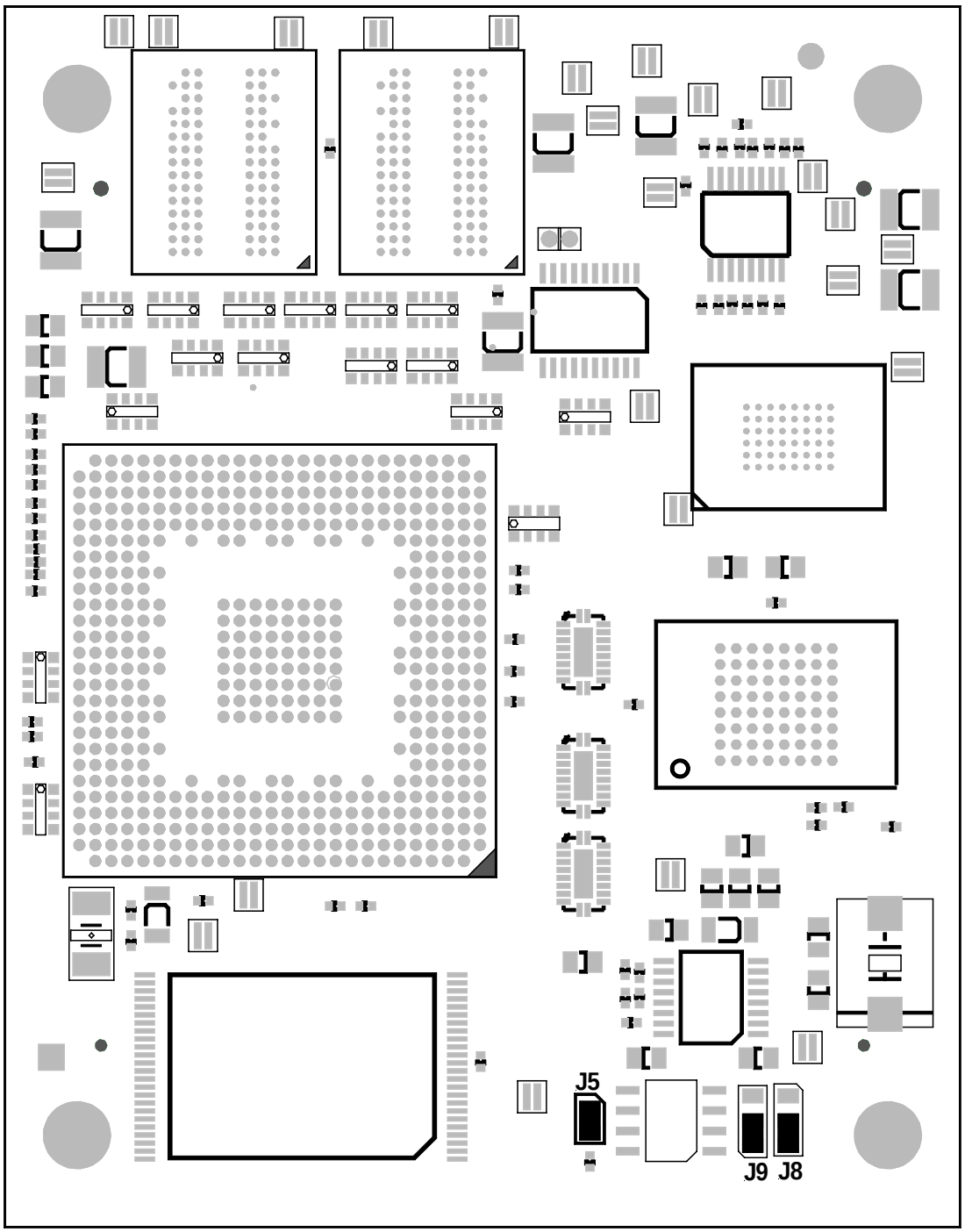


Figure 6: Location of the Jumpers (Controller Side)
(phyCORE-MPC5121e/3-tiny Standard Version)

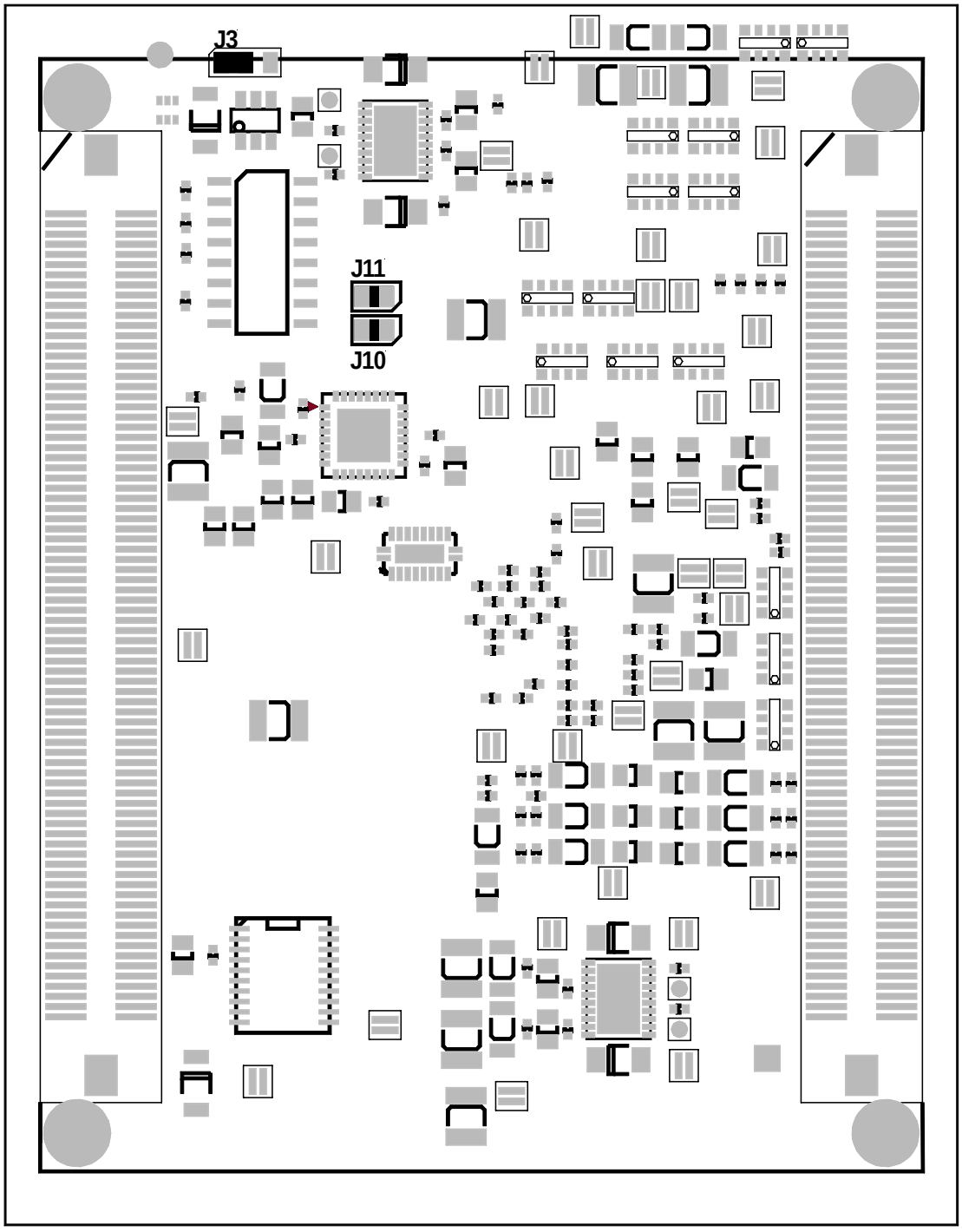


Figure 7 Location of the Jumpers (Bottom Side)
(phyCORE-MPC5121e/3-tiny Standard Version)

The jumpers (J = solder jumper) have the following functions:

Jumper	Comment
J10,	J10 disconnects the receive line (PSC6_3_RXD) of the MPC5121e/3's PSC6 from the RS-232 transceiver at U18. Thus the controller's TTL signals is available at pin X1C19 (PSC6_3_RXDL) which is useful, for instance, for optical isolation of the RS-232 interface.
open	The UART receive signal PSC6_3_RXD is disconnected from the RS-232 transceiver.
closed	The UART receive signal PSC6_3_RXD is connected to the on-board RS-232 transceiver.
J11	J11 disconnects the receive line (PSC3_3_RXD of the MPC5121e/3's PSC3 from the RS-232 transceiver at U18. Thus the controller's TTL signal is available at pin X1D16 (PSC3_3_RXD) which is useful, for instance, for optical isolation of the RS-232 interface.
open	The UART receive signal PSC3_3_RXD is disconnected from the RS-232 transceiver.
closed	The UART receive signal PSC3_3_RXD is connected to the on-board RS-232 transceiver.
J5	J5 connects pin 7 of the serial memory at U20 to GND. On many memory devices pin 7 enables/disables the activation of a write protect function. It is not guaranteed that the standard serial memory populating the phyCORE-MPC5121e/3-tiny will have this write protection function. Default: closed *Please refer to the corresponding memory data sheet for more detailed information.*
J8, J9	J8 and J9 define the slave addresses (A1 and A2) of the serial memory U20 on the I^2C2 bus. In the high-nibble of the address, I^2C memory devices have the slave ID 0xA. The low-nibble is build from A2, A1, A0, and the R/W bit. It must be noted that the RTC at U21 is also connected to the I^2C bus. The RTC has the address 0xA2/0xA3 which cannot be changed.
2+3, 2+3	A2= 0, A1= 1 (0xA4 / 0xA5 depending on R/W; A0= 0 per default) I^2C slave address 0xA4 for write operations and 0xA5 for read access.
J3	Enables or disables the clock output of the I²C RTC at U21. The RTC clock output is connected to X1B1.
1 + 2	RTC clock output disabled
2 + 3	RTC clock output enabled

Table 3: Jumper Settings

4 Power Requirements

The phyCORE-MPC5121e/3-tiny must be supplied with one supply voltage only:

Supply voltage: +3.3 V ±5 % with 1.5 A load

The supply pins are located at the phyCORE-Connector X1:

VCC +3V3:
X1 1C, 2C, 4C, 5C, 1D, 2D, 4D, 5D

corresponding GND:
X1 3C, 3D, 7C, 9D, 12C, 14D, 17D, 19C
Please refer to section 2 for information on additional GND Pins located at the phyCORE-Connector X1

Caution:
Connect all +3V3 input pins to your power supply and at least the matching number of GND pins neighboring the +3V3 pins.

As a general design rule we recommend connecting all GND pins neighboring signals which are being used in the application circuitry

Optional Supply Input VBAT

VDD_VBAT_V3V3 (X1C6) is the input pin that supplies the Real-Time Clock (U21) and the SRAM (U15). The MAX6364 battery supervisor IC (U3) senses the 3.3 V main supply and VDD_VBAT_3V3 and switches to the voltage with the higher level. VDD_VBAT_3V3 should be supplied from a 3 V source (i.e. lithium battery).

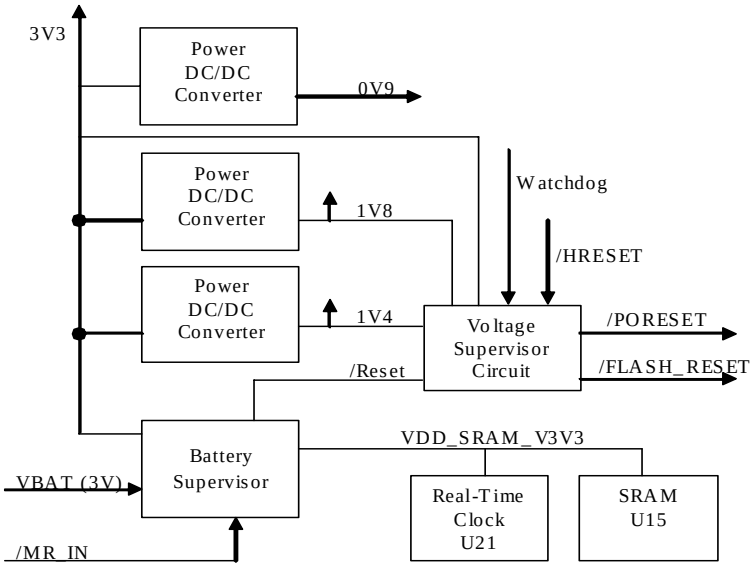


Figure 8: Power Supply Diagram

External voltages: 3V3, 3V VBAT optional

- 3V3 PowerPC I/O, Flash memory, Ethernet PHY, ser. EEPROM, RS232 Transceiver
- 3V VBAT (optional) SRAM, RTC, on chip RTC

Internally generated voltages: 1V4, 1V8, 0V9

- 1V8 DDR2 SDRAM
- 1V4 PowerPC Core
- 0V9 DDR2 termination Voltage

4.1 Voltage Supervision and Reset

The input voltage 3V3 as well as the on-board generated operation voltages 1V8 and 1V4 are monitored by a voltage supervisor device at U2. This circuitry is responsible for generation of the system reset signal /PORESET. The voltage supervisor IC initiates a reset cycle if any operating voltage drops below its minimum threshold value. After all voltages reach their required value, the supervisor chip adds an additional 200 ms delay until the /PORESET line will be inactive (high). /PORESET connects to the processor’s reset input.

/PORESET is combined via a multiple function gate 74LVC1G57 with /HRESET to a logic AND with /FLASH_RESET (on-board flash memory reset) as output. This logic connection is used to ensure a proper reset of the NOR-Flash at U14 independent of the occurring reset.

The voltage supervisor's master reset input /MR_IN can be connected to an external signal or switch through pin X1D10 to release a asynchronous reset manually.

5 System Start-Up Configuration

During the reset cycle the MPC5121e/3 processor reads the state of selected controller signals to determine the basic system configuration. The configuration circuitry (pull-up or pull-down resistors) is located on the phyCORE module.

The system start-up configuration includes:

- Clock/PLL configuration
- Basic LocalPlus characteristic for boot memory configuration
- Boot device select configuration
- PCI configuration
- On-chip watchdog configuration
- NAND Flash configuration

Note:
Since most of these signal lines are routed to the phyCORE connector care must be taken not to overwrite the startup configuration accidentally when connecting these signals to external devices. Please refer also to section *4.6 "Reset Configuration Word (RST_CONF)"* of the Freescale MPC5121e/3 Reference Manual.
-

The following default configuration is read by the processor with the rising edge of the reset line /PORESET.

Signal Name	Register Bit	Logic Level	Description
EMB_AX02	RCWHR[28]	0	System Oszillator Mode disabled
LPC_AX03 EMB_AD31 EMB_AD30 EMB_AD29 EMB_AD28 EMB_AD27	RCWLR [13..8]	0 0 0 0 0 0	System clock ratio, System clock : PLL clock = 1 : 2, 800MHz / 2 = 400 MHz
EMB_AD26 EMB_AD25 EMB_AD24 EMB_AD23	RCWLR [27..24]	0 1 0 1	PLL clock ratio, PLL clock : Input Clock = 24:1, 33.33MHz * 24 = 800MHz
EMB_AD22	RCWHR[2]	0	Check Stop signal disabled
EMB_AD21	RCWHR[6]	0	NAND Flash Port Size 8 bit
EMB_AD20	RCWHR[7]	0	NAND Flash Page Size 2k
EMB_AD19 EMB_AD18	RCWHR[9..8]	0 1	Local Plus Data Port Size 16 bit
EMB_AD17	RCWHR[10]	0	Byte addressing disabled
EMB_AD16	RCWHR[11]	1	Local Plus Bus in multiplexed mode
EMB_AD15	RCWHR[29]	0	PCI Arbiter disabled per default
EMB_AD14	RCWHR[31]	1	PCI Interface in host mode
EMB_AD13 EMB_AD12 EMB_AD11 EMB_AD10	RCWLR [19..16]]	0 1 0 0	Core PLL clock ratio, Core Clock : CSB Clock = 2 : 1, 200 MHz * 2 = 400 MHz
EMB_AD9 EMB_AD8	RCWHR[5..4]	0 0	No LPC Address extensions available
EMB_AD7	RCWHR[30]	0	PCI operates with a clock frequency of 33MHz
EMB_AD6	RCWHR[3]	0	Little Endian Mode
EMB_AD5	RCWHR[26]	1	Booting from Address 0xfff00100
EMB_AD4	RCWHR[27]	0	e300 Core enabled
EMB_AD3	RCWHR[20]	0	e300 Core Test mode disabled
EMB_AD2	RCWHR[23]	0	on-chip watchdog disabled
EMB_AD1 EMB_AD0	RCWHR [22..21]	0 0	booting from LPC Device

Table 4: System Start-Up Configuration

6 System Memory

The system memory consist of Flash memory, DDR2 SDRAM (Double Data Rate 2 Synchronous Dynamic Random Access Memory) a battery bufferable SRAM and a small non-volatile memory device:

- 16 MByte Intel Strata Flash memory (1x 16-bit, multiplexed mode)
- 128 MByte DDR SDRAM (2x 16-bit)
- 2MByte battery bufferable SRAM
- 4 kByte serial memory (EEPROM)

The Flash memory is connected to the PowerPC LocalPlus bus and is controlled by /CS0. This chip select signal is used for boot operation.

The DDR2 SDRAM is connected to the special SDRAM interface of the MPC5121e/3 processor and operates at the maximum frequency (200 MHz).

The SRAM memory is connected to the PowerPC LocalPlus bus and is controlled by /CS1. This memory device can be used to store non volatile data, when buffered by a backup battery.

Communication to the small non-volatile memory device (EPROM) is established over the processor's first I^2C bus. This memory device holds the boot loader (U-Boot) environment variables in its first two kilobytes and can be used for parameter storage. Optionally, the environment variable can be stored in the parallel flash device connected to the Local Plus Bus.

6.1 Flash Memory

6.1.1 The NOR Flash Memory (U14)

Use of NOR-Flash as non-volatile memory on the phyCORE-MPC5121e/3-tiny provides an easily reprogrammable means of code storage.

- 16 up to 64 MByte Intel Strata Flash memory
- 16-bit bus width
- Only asynchronous operation is possible

The Flash memory bank supports the following Intel memory devices:

Type	Size	Manufacturer	Device Code	Manufacturer Code
Asynchronous Devices				
28F128P33-T	16 MByte	Intel	0x881E	0x0089
28F128P33-B	16 MByte	Intel	0x8821	0x0089
28F256P33-T	32 MByte	Intel	0x891F	0x0089
28F256P33-B	32 MByte	Intel	0x8922	0x0089
28F512P33-T	64 MByte	Intel	0x891F	0x0089
28F512P33-B	64 MByte	Intel	0x8922	0x0089

Table 5: Choice of Flash Memory Devices and Manufacturers[1]

The organization of the Flash memory bank is 16-bit. The Flash memory bank is controlled by the processor chip select signal /CS0. This chip select signal is the dedicated control signal for boot purposes.

The MPC5121e/3's LocalPlus bus can be configured for many different bus modes. For /CS0 the 32-bit address / 16-bit data multiplexed mode was chosen because it offers the largest address space without interfering the ATA or NAND Flash bus. With 32 address lines a total of 4 GByte of data/code can be addressed. It is possible to use different bus modes on other available Chip Select signals.

1: Flash types in the shaded lines are the preferred parts for the phyCORE-MPC5200B tiny.

The Flash memory bank 0 starts at address 0x0000_0000 or 0xFFE0_0000 depending on the startup configuration of the processor. By default the start address 0xFFE0_0000 is chosen based on the hardware configuration of the phyCORE modul.

The access speed depends on the equipped memory device. The LocalPlus Bus clock cycle is determined by the LPC clock which is configured by the LPC- and IPS clock divider. A typical configuration selects 33 MHz. The resulting basic cycle time is 30.30 ns.

The MPC5121e/3 processor multiplexed read or write is divided into a address tenure and a data tenure. Because the chip select signal is generated with the start of the data tenure only this period is of interest for access time calculation.

The equation for access time calculation is: $(2+WS) * t_{LPCCK} - 8.5$ ns

To support all memory speed grades up to 85 ns at least 2 wait states must be added for /CS0.

- 2 wait state and 1 dead cycle for /CS0
  (supports 33 MHz LPC clock)
- 5 wait states and 2 dead cycles for /CS0
  (supports 66 MHz LPC clock)

No additional voltages are needed for in-system programming. As of the printing of this manual, Flash devices generally guarantee at least 100,000 erase/programming cycles. *Refer to the applicable INTEL data sheet for detailed description of the erasing and programming procedure.*

6.1.2 The NAND Flash Memory (U17)

Additional use of NAND Flash as non-volatile memory on the phyCORE-MPC5121e/3-tiny provides a second, easily reprogrammable means of code storage.

The phyCORE-MPC5121e/3-tiny is capable of using 8-Bit NAND Flash devices. The following Flash devices can be used on the phyCORE-MPC5121e/3-tiny.

Manufacturer	NAND Flash	Density(GByte)
ST Microelectronics	NAND08GW3C2A	1
ST Microelectronics	NAND16GW3C4A	2
Samsung	K9K8G08U0A	1

Table 6: Choice of NAND Flash Memory Devices and Manufacturers

Additionally, any parts that are footprint (TSSOP48) and functionally compatible with the NAND Flash devices listed above may also be used with the phyCORE-MPC5121e/3-tiny.

These Flash devices are programmable with 3.3 V. No dedicated programming voltage is required.

As of the printing of this manual these NAND Flash devices generally have a life expectancy of at least 100,000 erase/program cycles and a data retention rate of 10 years.

6.2 NOR vs. NAND

Typically both NOR and NAND Flash are not needed in the end system. The system designer will choose between one or the other. NAND Flash provides high densities and low cost per bit, but suffers from bad blocks and slower access times. NOR Flash provides fast access times, execute-in-place functionality, and error free sectors, but suffers from a higher cost per bit. It is up to the system designer to decide which characteristics are important for the system at hand. In addition the system designer should consider the total flash size requirement. Although the cost per bit is more for NOR flash and it could very well be that the system requires only 2MB of flash, in which 2MB of NOR may be cheaper than the required minimum 16MB of NAND.

6.3 DDR2 SDRAM

The phyCORE-MPC5121e/3-tiny is equipped with fast **D**ouble **D**ata **R**ate 2 **S**ynchronous **D**ynamic **R**andom **A**ccess **M**emory (DDR2 SDRAM) devices. This memory is connected to a dedicated SDRAM interface provided by the MPC5121e/3 processor.

The DDR2 SDRAM memory bank consist of two devices with a 16-bit data bus each. In order to support the 32-bit bus width of the processor one device is connected to the lower data bus word and the other to the upper data bus word. The memory bank is controlled by chip select signal /DDR2_MCS of the processor's DDR2 SDRAM controller.

Table 7 shows all possible memory configurations.

Available Capacity	Device Organization	Devices (two)
128 MByte	1 GBit 8 MBit x 16 x 4 banks	MT47H32M16 BGA84 packaging
256 MByte	2 GBit 8 MBit x 16 x 8 banks	MT47H64M16 BGA84 packaging
512 MByte	4 GBit 16 MBit x 16 x 8 banks	MT47H128M16 BGA84 packaging

Table 7: DDR2 SDRAM Device Selection

6.4 Battery bufferable SRAM

The phyCORE-MPC5121e/3-tiny is equipped with a **S**tatic **R**andom **A**ccess **M**emory (SRAM) devices. This memory is connected to the LPC bus interface provided by the MPC5121e/3 processor.

The SRAM memory bank consist of one device with a 16-bit data bus which is connected parallel to the 32-bit bus of the processor without using the upper data bus word. The memory bank is controlled by chip select signal /CS1 of the processor's LPC bus controller.

Table 77 shows all possible memory configurations.

Available Capacity	Device Organization	Device
1 MByte	8 MBit	CY7C62157DV30LL BGA48 packaging
2 MByte	16 MBit	CY7C62167DV30LL BGA48 packaging

Table 8: SRAM Device Selection

6.5 Serial Memory

The phyCORE-MPC5121e/3-tiny features a non-volatile memory device (EEPROM) with a serial I^2C interface at U20. This memory can be used for storage of configuration data or operating parameters that must be maintained in the event of a power interruption. The available capacity is 4 kByte.

Note:
The first 2 kilobytes section of the EEPROM may already used for storing the boot manager (U-Boot) environment variables. This portion must then not be used by user data.

The MPC5121e/3 processor provides three on-chip I^2C interfaces (I2C0 to I2C2). The memory device is connected to I²C interface I2C0.

Table 9 gives an overview of the possible devices for use at U20 as of the printing of this manual.

Type	Size	I^2C Frequency	Address Pins	Write Cycles	Life of Data	Device	Manufacturer
EEPROM	4 kBytes	400 kHz	A2, A1, A0	1 000 000	100 yrs.	CAT24WC32	CATALYST

Table 9: Serial Memory Options for U20

It is important to note that the RTC U21 is also connected to I^2C interface I2C0. The RTC can operate with a bus frequency up to 400 kHz. Therefore the use of high bus frequencies for accessing the serial memory is not recommended. The RTC has the I^2C bus slave address 0xA2 / 0xA3. The slave address of the serial memory must be selected accordingly using solder jumpers J8 (A2) and J9 (A1) to avoid bus collision.

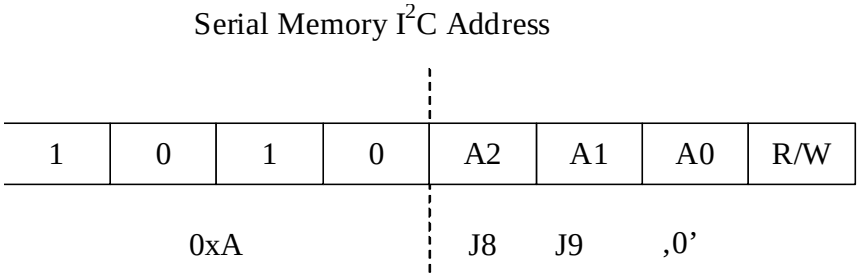


Figure 9: Serial Memory I²C Slave Address

Possible configuration options are shown below:

I²C Address	**J9 A1**	**J8 A2**
0xA0 / 0xA1	1 + 2	2 + 3
0xA4 / 0xA5	2 + 3	2 + 3
0xA8 / 0xA9	1 + 2	1 + 2
0xAC / 0xAD	2 + 3	1 + 2

Table 10: Serial Memory I²C Address (Examples)

Note:
Address lines A1 and A2 are not always made available with certain serial memory types. This should be noted when configuring the I²C bus slave address.

The serial memory U20 can also be write protected. Per default Jumper J5 is populated and the content of the serial memory can be modified. Removing Jumper J5 protects the seriel memory U20.

7 Real-Time Clock RTC-8564 (U21)

For real-time or time-driven applications, the phyCORE-MPC5121e/3-tiny is equipped with an RTC-8564 Real-Time Clock at U21. This RTC device provides the following features:

- Serial input/output bus (I^2C), address 0xA2(write)/0xA3(read)
- Power consumption
  Bus active (400 kHz): < 1 mA
  Bus inactive, CLKOUT inactive: = 275 nA
- Clock function with four year calendar
- Century bit for year 2000-compliance
- Universal timer with alarm and overflow indication
- 24-hour format
- Automatic word address incrementing
- Programmable alarm, timer and interrupt functions

The Real-Time Clock is programmed via the I^2C bus (address 0xA2 / 0xA3). Since the MPC5121e/3 is equipped with an internal I^2C controller, the I^2C protocol is processed very effectively without extensive processor action.

The Real-Time Clock also provides an interrupt output that extends to the /INT_RTC signal X1A1. An interrupt occurs in the event of a clock alarm, timer alarm, timer overflow and event counter alarm. It has to be cleared by software. With the interrupt function, the Real-Time Clock can be utilized in various applications.

If the RTC interrupt is to be used as a software interrupt via a corresponding interrupt input of the processor, the signal /INT_RTC must be connected externally with a processor interrupt input.

The RTC_CLKOUT signal, which can be found at X1B1, can be programmed to various frequencies e.g. 1Hz. The RTC_CLKOUT output must be enabled via solder jumper J3.

For more information on the features of the RTC-8564, refer to the corresponding Data Sheet.

Note:
After connection of the supply voltage the Real-Time Clock generates **no** interrupt. The RTC must be first initialized (*see RTC Data Sheet for more information*).

8 Serial Interfaces

The phyCORE- MPC5121e/3-tiny provides on-board transceivers for three serial interfaces:

1. A multichannel RS-232 transceiver supporting 250kbps on UART1(PSC3) and 250kbps on UART2 (PSC6).
2. A high speed on chip USB OTG transceiver supporting the MPC5121e/3 USB OTG interface.
3. An Auto-MDIX enabled 10/100 Ethernet PHY supporting the MPC5121e/3 Ethernet MAC.

The following sections of this chapter detail each of these serial interfaces and any applicable configuration jumpers.

8.1 RS-232 Interface

A dual-channel RS-232 transceiver is located on the phyCORE-MPC5121e/3-tiny at U18. This device adjusts the signal levels of the PSC3_3_RXD/PSC3_2_TXD and PSC6_3_RXD/ PSC6_2_TXD TTL signal lines (MPC5121e/3 PSC3/PSC6). The RS-232 interface enables connection of the module to a COM port on a host-PC or other peripheral devices. In this instance, the RXD3-RS232 or RXD6-RS232 line (X1D22/X1C21) of the transceiver is connected to the corresponding TXD line of the COM port; while the TXD3-RS232 or TXD6-RS232 line (X1D23/X1C23) is connected to the RXD line of the COM port. The Ground circuitry of the phyCORE-MPC5121e/3 tiny must also be connected to the applicable Ground pin on the COM port.

The processor's on-chip UART supports handshake signal communication. Use of an RS-232 signal level in support of handshake communication requires use of an external RS-232 transceiver. If using the phyCORE-MPc5121e/3 carrier board the appropriate transceivers are populated on the carrier board.

Furthermore it is possible to use the TTL signals of both of the UART channels externally. These signals are available at X1D16, X1D17 (PSC3_3_RXD, PSC3_2_TXD) and X1C19, X1C20 (PSC6_3_RXD, PSC6_2_TXD) on the phyCORE-Connector. External connection of TTL signals is required for galvanic isolation of the interface signals. Using solder jumpers J10 and J11, the TTL transceiver outputs of the on-board RS-232 transceiver devices can be disconnected from the receive lines PSC3_3_RXD and PSC6_3_RXD. This is required to avoid that the external transceiver drives signals against the on-board transceiver. The transmit lines PSC3_2_TXD / PSC6_2_TXD can be connected parallel to the transceiver input without causing any conflicts.

The following table shows the possible settings of jumpers J10 and J11:

Jumper	Comment
J10,	J10 disconnects the receive line (PSC6_3_RXD) of the MPC5121e/3's PSC6 from the RS-232 transceiver at U18. Thus the controller's TTL signals is available at pin X1C19 (PSC6_3_RXDL) which is useful, for instance, for optical isolation of the RS-232 interface.
open	The UART receive signal PSC6_3_RXD is disconnected from the RS-232 transceiver.
closed	The UART receive signal PSC6_3_RXD is connected to the on-board RS-232 transceiver.
J11	J11 disconnects the receive line (PSC3_3_RXD of the MPC5121e/3's PSC3 from the RS-232 transceiver at U18. Thus the controller's TTL signal is available at pin X1D16 (PSC3_3_RXD) which is useful, for instance, for optical isolation of the RS-232 interface.
open	The UART receive signal PSC3_3_RXD is disconnected from the RS-232 transceiver.
closed	The UART receive signal PSC3_3_RXD is connected to the on-board RS-232 transceiver.

Table 11: Jumper Settings for the serial interface

8.2 Ethernet Interface

Connection of the phyCORE-MPC5121e/3-tiny to the world wide web or a local network (LAN) is possible using the integrated FEC (Fast Ethernet Controller) of the Freescale processor. The FEC operates with a data transmission speed of 10 or 100 Mbit/s.

8.2.1 PHY Physical Layer Transceiver

With a physical layer transceiver mounted at U19 the phyCORE-MPC5121e/3-tiny has been designed for use in 10Base-T and 100Base-T networks. The 10/100Base-T interface with its LED signals extends to phyCORE-Connector X1. In order to connect the module to an existing 10/100Base-T network an external circuitry, which consists of the magnetics and the appropriate Ethernet plug, is required. The required 49,9 Ohm +/-1% termination resistors on the analog signals (ETH_RX±, ETH_TX±) are already populated on the module.

If you are using the applicable Development Board for the phyCORE-MPC5121e/3-tiny (part number PCM-962-tiny), the external circuitry mentioned above is already integrated on the board (*refer to section 14*).

The default PHY address configured with the boot-strapping option is 0x0.

Table 12 shows the interface signals for the Ethernet channel.

FEC Channel PHY U19	Pin Function	Location at phyCORE-Connector
ETH_RX+	Differential positive receive input signal	X1D35
ETH _RX-	Differential negative receive input signal	X1C35
ETH _TX+	Differential positive transmit output signal	X1D36
ETH _TX-	Differential negative transmit output signal	X1C36
ETH _LED0	Link/activity LED output "H"/LED off no link "L"/LED on link "toggle"/LED toggle activity	X1C33
ETH _LED1	Speed LED output "H"/LED off 10BT "L"/LED on 100BT	X1C34

Table 12: Signal Definition PHY Ethernet Port (U19)

8.2.2 MAC Address

In a computer network such as a local area network (LAN), the MAC (Media Access Control) address is a ***unique*** computer hardware number. For a connection to the Internet, a table is used to convert the assigned IP number to the hardware's MAC address.

In order to guarantee that the MAC address is unique, all addresses are managed in a central location. PHYTEC has acquired a pool of MAC addresses. The MAC address of the phyCORE-MPC5121e/3-tiny is located on the bar code sticker attached to the module. This number is a 12-digit HEX value.

8.3 USB OTG Interface

The MPC5121e implements two USB modules (USB0 and USB1) which are capable of dual-role (DR) or On-The-Go (OTG). USB0 and USB1 can be connected to an external PHY using the ULPI protocol. Additionally, USB0 can be connected to an on-chip UTMI+ PHY. The USB0 and USB1 modules have the following features:

- USB device mode support
- USN On-The-Go mode support including host capability
- Complies with USB specification Rev. 2.0
- Support for high-speed (480Mbps), full-speed (12 Mbps) and low-speed (1.5Mbps) operations
- External PHY support with UTMI+ low pin count (ULPI)interface

The following table lists the USB-Signal extensions at the phyCORE-Connector X1:

Interface	Signal	Location at phyCORE-Connector
USB-OTG	USB_PWRFAULT	X1C41
	USB_DP	X1C43
	USB_DM	X1C44
	USB_DRVVBUS	X1C45
	USB_TPA	X1D43
	USB_VBUS	X1D45
	USB_UID	X1D46

Table 13: USB-OTG Interface Signal Location

For additional information of the USB OTG controller refer to the MPC5121e/3 Reference Manual as well as the USB-OTG bus specification provided by www.usb.org.

8.4 SATA Interface

The MPC5121e/3's SATA interface is a high-speed serialized ATA data link interface compliant with SATA Revision 1.0a. The interface includes DMA controller, command layer, transport layer, link layer PhyCtrl layer, Physical Coding Sublayer and the physical layer. The interface itself supports only one SATA device.

The phyCORE-MPC5121e/3-tiny provides the MPC5121e/3's SATA Interface at the phyCORE-Connector at the following locations:

Interface	Signal	Location at phyCORE-Connector
SATA	SATA_RXP	X1A40
	SATA_RXN	X1A41
	SATA_TXP	X1B45
	SATA_TXN	X1B46
	SATA_ANAVIZ	X1B43

Table 14: SATA Interface Signal Location

8.5 CAN Interface

The CAN Interfaces of the MPC5121e/3 are communication controller implementing the CAN 2.0 A/B protocol as defined in the BOSCH specification.

The phyCORE-MPC5121e/3 supports up to four CAN interfaces which are available at the following phyCORE-Connector locations:

Interface	Signal/port function	Schematic signal reference name	Location at phyCORE-Connector
CAN1	CAN1_RX	CAN1_RX	X1D20
	CAN1_TX	CAN1_TX	X1D21
CAN2	CAN2_RX	CAN2_RX	X1D18
	CAN2_TX	CAN2_TX	X1C18
CAN3	CAN3_RX	/IRQ1	X1A3[3]
	CAN3_TX	/IRQ0	X1B2[1]
CAN4	CAN4_RX	I2C2_SDA	X1D28[1]
	CAN4_TX	I2C2_SCL	X1D27[1]

Table 15: CAN Interface Signal Location

Alternatively the CAN signals can be rerouted by the IO control registers of the MPC5121e/3 so that necessary signal functions like IRQs are available. If the CAN signals are not used the IO ports of the controller are available for alternative functions like GPIO.

Please refer to section IO control in the processors reference manual for more information.

[3] *The mentioned port functions are not the default port functions for the phyCORE-MPC5121e/3-tiny and have to be configured separately. Refer to the controllers reference manual for more information.*

8.6 I²C Interface

The Inter-Integrated Circuit (I^2C) interface is a two-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The phyCORE-MPC5121e/3-tiny contains three identical and independent I^2C modules which are available on the phyCORE-Connector. The following table lists the I^2C ports at the phyCORE-Connector:

Interface	Signal	Location at phyCORE-Connector
I2C0	I2C0_SCL	X1C31
	I2C0_SDA	X1D32
I2C1	I2C1_SCL	X1C26
	I2C1_SDA	X1C28
I2C2	I2C2_SCL	X1D27
	I2C2_SDA	X1D28

Table 16: I^2C Interface Signal Location

The I^2C-RTC and I^2C-EEPROM populated on the phyCORE-Module are connected to I^2C Interface 0 of the MPC5121e/3 processor.

8.7 J1850 Interface (BDLC)

The BDLC module of the MPC5121e/3 is a serial communication module which allows the user to send and receive messages across a Society of Automotive Engineers (SAE) J1850 serial communication network.

The phyCORE-MPC5121e/3-tiny provides the signals of the SAE network at the following pins of the phyCORE-Connector:

Interface	Signal	Location at phyCORE-Connector
(SAE) J1850	J1850_TX	X1C24
	J1850_RX	X1C25

Table 17: J1850 Interface Signal Location

8.8 JTAG Interface

The MPC5121e/3 CPU provides a JTAG interface which allows connection to debuggers, emulators and boundary scan. The JTAG interface signals extend to the module's phyCORE-Connector X1. The pinout of the JTAG interface at X1 is described in the following table.

Interface	Pin Row	Signal	Description
JTAG	X1D41	JTAG_TDO	Test data output.
	X1D40	JTAG_TDI	Test data input with internal 10k pull-up.
	X1D42	JTAG_TMS	Test mode select input with internal 10k pull-up.
	X1D38	JTAG_TCK	Test clock input with internal 10k pull-down.
	X1C39	/JTAG_TRST	Test controller reset input with internal 10k pull-up.
	X1C10	/SRESET	Bidirektional low active SRESET Signal of the MPC5121e/3 with 3k3 pull-up
	X1C11	/HRESET	Bidirektional low active SRESET Signal of the MPC5121e/3 with 3k3 pull-up
	X1C40	/JTAG_CKSTP_O	Test controller CKSTOP output with internal 10k pull-up.

Table 18: JTAG Interface

9 Parallel Interfaces

9.1 PCI Interface

The MPC5121e/3's PCI controller connects the processor and memory system to the I/O components via the PCI system bus. This interface acts as initiator (master) and target (slave) device. The PCI controller uses a 32-bit multiplexed, address/data bus. The interface provides address and data parity with error checking and reporting. The interface provides three physical address spaces – 32-bit address memory, 32-bit address I/O, and PCI configuration space. It supports up to three external masters.

In order to support all features of the MPC5121e/3's PCI interface with the phyCORE-MPC5121e/3-tiny all PCI signals extend to the phyCORE-Connector X1.

The following table displays the location of the PCI-Signals at the phyCORE-Connector:

Interface	Pin Row	Signal	Description
PCI	X1A46	/PCI_INT	PCI interrupt output.
	X1A51, X1B47, X1A48	/PCI_GNT[0] /PCI_GNT[1] /PCI_GNT[2]	PCI Arbiter Grant Signals 0…2
	X1B52 X1B48 X1A49	/PCI_REQ[0] /PCI_REQ[1] /PCI_REQ[2]	PCI Arbiter Request Signals 0…2
	X1A50	/PCI_RST_OUT	PCI Reset Output Signal
	X1B50	PCI_CLK	PCI Clock Output Signal
	X1B58	PCI_IDSEL	PCI Initialization Device Select
	X1A53, X1B53, X1A54, X1A55, X1B55, X1A56, X1B56, X1B57,	PCI_AD[31] PCI_AD[30] PCI_AD[29] PCI_AD[28] PCI_AD[27] PCI_AD[26] PCI_AD[25] PCI_AD[24]	multiplexed PCI Address/Data Signals

X1A59, X1A60, X1B60, X1A61, X1B61, X1B62, X1A63, X1B63, X1B70, X1A71, X1B71, X1B72, X1A73, X1B73, X1A74, X1A75, X1A76, X1B76, X1B77, X1A78, X1B78, X1A79, X1A80, X1B80	PCI_AD[23] PCI_AD[22] PCI_AD[21] PCI_AD[20] PCI_AD[19] PCI_AD[18] PCI_AD[17] PCI_AD[16] PCI_AD[15] PCI_AD[14] PCI_AD[13] PCI_AD[12] PCI_AD[11] PCI_AD[10] PCI_AD[9] PCI_AD[8] PCI_AD[7] PCI_AD[6] PCI_AD[5] PCI_AD[4] PCI_AD[3] PCI_AD[2] PCI_AD[80] PCI_AD[0]	
X1A65	/PCI_IRDY	PCI Initiator Ready Signal
X1B65	/PCI_FRAME	PCI Cycle Frame Signal
X1A66	/PCI_DEVSEL	PCI Device Select Signal
X1B66	/PCI_TRDY	PCI Target Ready Signal
X1B67	/PCI_STOP	PCI Stop Signal
X1A68	/PCI_PERR	PCI Parity Error Signal
X1B68	PCI_PAR	PCI Parity Signal
X1A69	/PCI_SERR	PCI System Error Signal
X1B75, X1A70, X1A64, X1A58	PCI_CBE[0] PCI_CBE[1] PCI_CBE[2] PCI_CBE[3]	PCI Bus Command / Byte Enable Signals

Table 19: PCI Interface Signals

9.2 PATA Interface

The MPC5121e/3's Parallel Advanced Technology Attachment (PATA) interface is primarily used to connect the processor to IDE hard disc drives and ATAPI optical disc drives.

For supporting the PATA functionality the phyCORE-MPC5121e/3-tiny extends all necessary PATA signals and the additional EMB Bus Signals to the phyCORE-Connector X1.

Interface	Pin Row	Signal	Description
PATA	X1A33	PATA_IOCHRDY	PATA Bus IO-Channel Ready Signal
	X1A34	PATA_INTRQ	PATA Bus Interrupt Request Signal
	X1A35	PATA_DRQ	PATA Bus DMA Request Signal
	X1B35, X1B36	/PATA_CE[1] /PATA_CE[2]	PATA Bus Chip Select Signals
	X1A36	/PATA_DACK	PATA Bus Host DMA Acknowledge
	X1B37	PATA_ISOLATE	PATA Bus Isolation Signal
	X1B38	/PATA_IOR	PATA Bus Read Strob Signal
	X1B40	/PATA_IOW	PATA Bus Write Strobe Signal
	X1B10, X1B11, X1A11, X1B12, X1A13, X1B13 X1A14, X1A15, X1B15, X1A16, X1B16, X1B17, X1A18, X1B18 X1A19, X1A20	EMB_AD[0] EMB_AD[1] EMB_AD[2] EMB_AD[3] EMB_AD[4] EMB_AD[5] EMB_AD[6] EMB_AD[7] EMB_AD[8] EMB_AD[9] EMB_AD[10] EMB_AD[11] EMB_AD[12] EMB_AD[13] EMB_AD[14] EMB_AD[15]	PATA Data Bus Signals
	X1A10 X1A9 X1B8	EMB_AX0 EMB_AX1 EMB_AX2	PATA Address Bus Signals

Table 20: PATA Interface Signals

10 The U-Boot Boot Loader

"U-Boot" is a universal boot loader firmware based on GPL (Gnu Public License). Its main function is initializing the system hardware after a reset followed by starting application software such as an operating system.

Furthermore, U-Boot provides various functions to query system information and to change the start-up behavior of the target system. For example U-Boot allows to choose from different boot sources (such as Ethernet, etc.). It also provides functions to download application code into Flash.

The serial interface is used to communicate with U-Boot on the target system. The U-Boot for phyCORE-MPC5121e/3-tiny uses PSC3 (PSC3_3_RXD[X1D16], PSC3_2_TXD [X1D17]) with 115200 Baud, 8, N, 1. The U-Boot boot messages can be viewed within a terminal program running on a host PC using the above mentioned communication settings.

Note:
PHYTEC delivers all phyCORE-MPC5121e/3-tiny modules with a pre-installed U-Boot allowing the user immediate startup. The U-Boot software project is subject to continuous maintenance and improvements. Firmware updates will occur without special notification. Should you require a specific version of U-Boot pre-installed at the time of delivery please contact PHYTEC's sales department.

If U-Boot is used as boot loader firmware and basic component of the system software, the user should be familiar with the following topics in order to ensure proper function:

- U-Boot default system configuration
- system resources required by U-Boot
- modifying the U-Boot loader

10.1 U-Boot Default System Configuration

The U-Boot boot loader changes the following default settings to different than the reset values of the controller on the phyCORE-MPC5121e/3-tiny:

Clock: Core = 400 MHz, CSB=200 MHz, PCI=33 MHz, LPC=33 MHz

Memory Base Address Register (MBAR): 0x80000000

DDR2-RAM: Automatic storage size detection; start address 0x0

Flash: Chip Select = /CSBoot, 16-bit data bus width, 32 address lines, multiplexed mode, 2 wait state; 16 MByte starting at address 0xFFE00000

PSC0, 1, 2: Ethernet: 100 Mbit/s with MD

PSC3: UART, 115200 baud, 8,N,1 ; SPI

PCI: Enabled 33MHz, PCI Arbiter disabled

I²C_0: EEPROM at address 0x54, RTC at address 0x51

10.2 System Resources Required by U-Boot

U-Boot is located at address 0xFFF0 0000 in the module's Flash and occupies three sectors (3 x 128kByte). The boot loader itself makes sure that these sectors are protected using the Flash's "locked sector" mechanism. This makes accidental erasure of U-Boot almost impossible. Following a system start at address 0xFFF0 0100 (high boot), U-Boot first initializes the DDR2-RAM interface, then copies itself to the upper end of the RAM memory space and transfers program execution to this address. As a result U-Boot now runs out of RAM which allows for reprogramming itself in Flash (firmware update).

So called environment variables are used to configure U-Boot. Such variables define the IP number as well as the MAC address using Ethernet configuration as example. The variables are saved in the module's EEPROM (U20) or in the parallel Flash (U14) connected to the Local Plus Bus and occupies 2 kByte. If stored in the EEPROM (U20) the environment variables occupy the first 2 kBytes.

When using the RAM memory, care should be taken to not overwrite the U-Boot code as well as the trap table which is located in the lower portion of the RAM. Among other factors, the size of the U-Boot stack determines how much memory at the upper end of the RAM memory range is occupied by U-Boot. As U-Boot is used the stack size is growing and more memory space is required. It is recommended to reserve a sufficient RAM portion to be used for the stack beginning at the stack start address.

Please refer to Figure 10 for more information

10.2.1 The "Backup" U-Boot

In the event the "original" U-Boot at address 0xFFF0 0000 becomes corrupted (e.g. by overwriting the loader with a wrong version) a second U-Boot loader at address 0x0000 0000 in the NAND Flash is available as an "emergency" backup version providing the same functionality as the original copy. This backup U-Boot can be started by connecting a 4.7 kOhm pull down resistor at pin X1B10 during a hardware reset cycle.

Note:
When using the phyCORE-MPC5121e/3-tiny in conjunction with the applicable Carrier Board (part number PCM-962-tiny) the "Backup" U-Boot loader can be started by pushing button S8 at reset time.

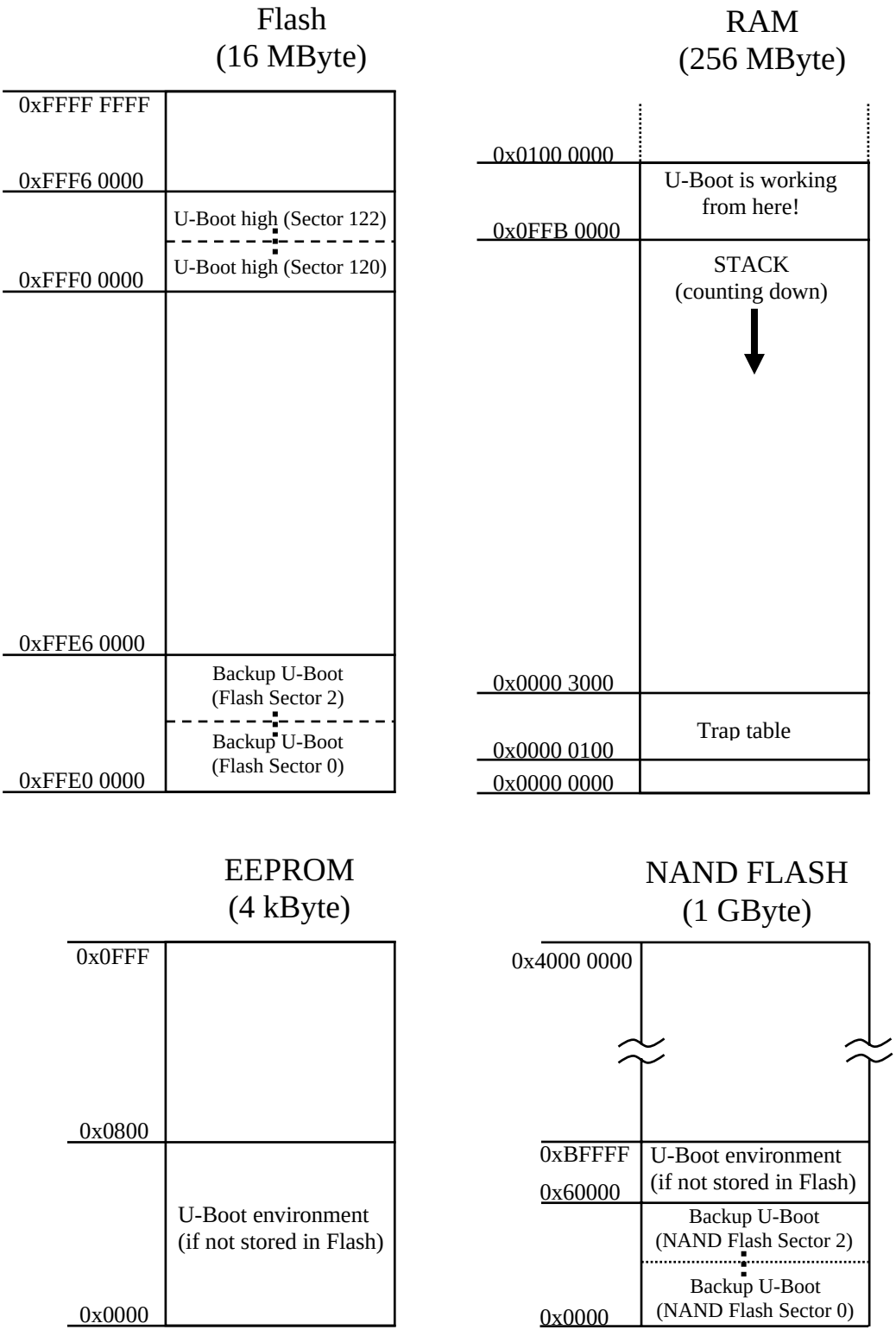


Figure 10: U-Boot Memory Map

10.3 Modifying the U-Boot Loader

Changing the U-Boot should always be compared to recompiling the program code and updating the Flash contents. A detailed description of each individual step would by far exceed the scope of this Hardware Manual. Please refer to the Application Note "Configuring and Updating the Boot Loader", document number LAN-044 for more details.

11 Component Placement Diagram

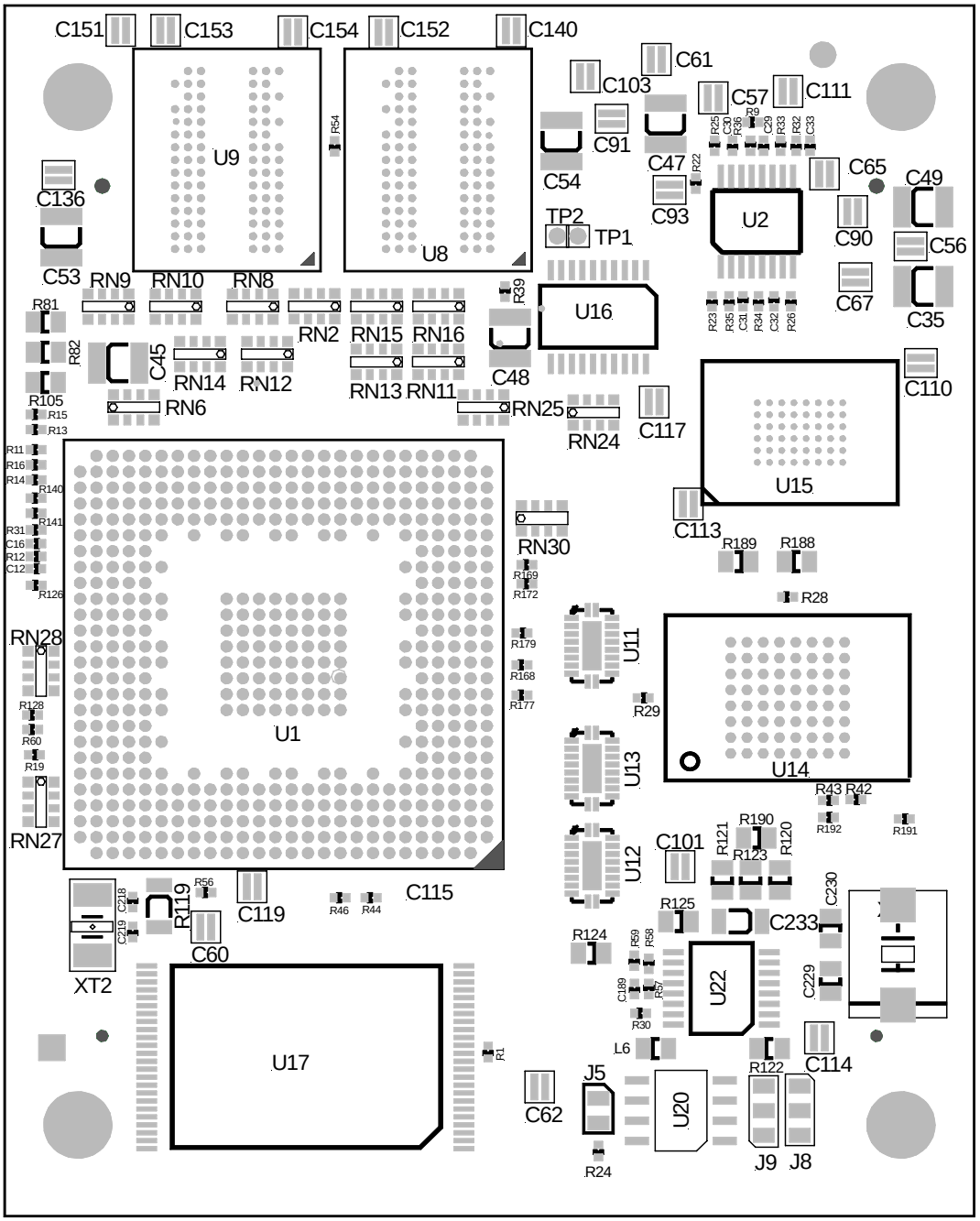


Figure 11: 1326.0 component placement Top view

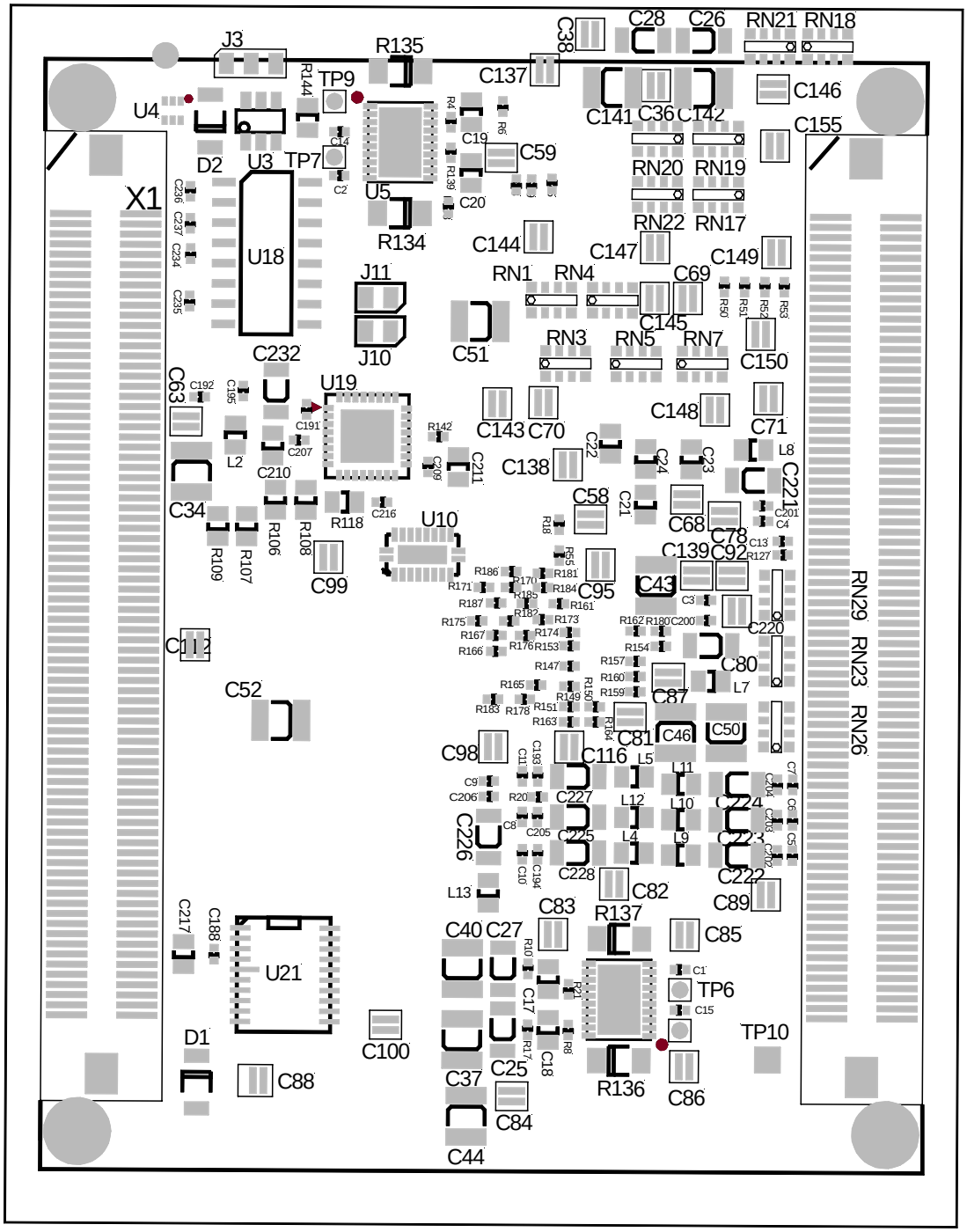


Figure 12: 1326.0 component placement Bottom view

12 Technical Specifications

The physical dimensions of the phyCORE-MPC5121e/3 tiny are represented in *Figure 13*.

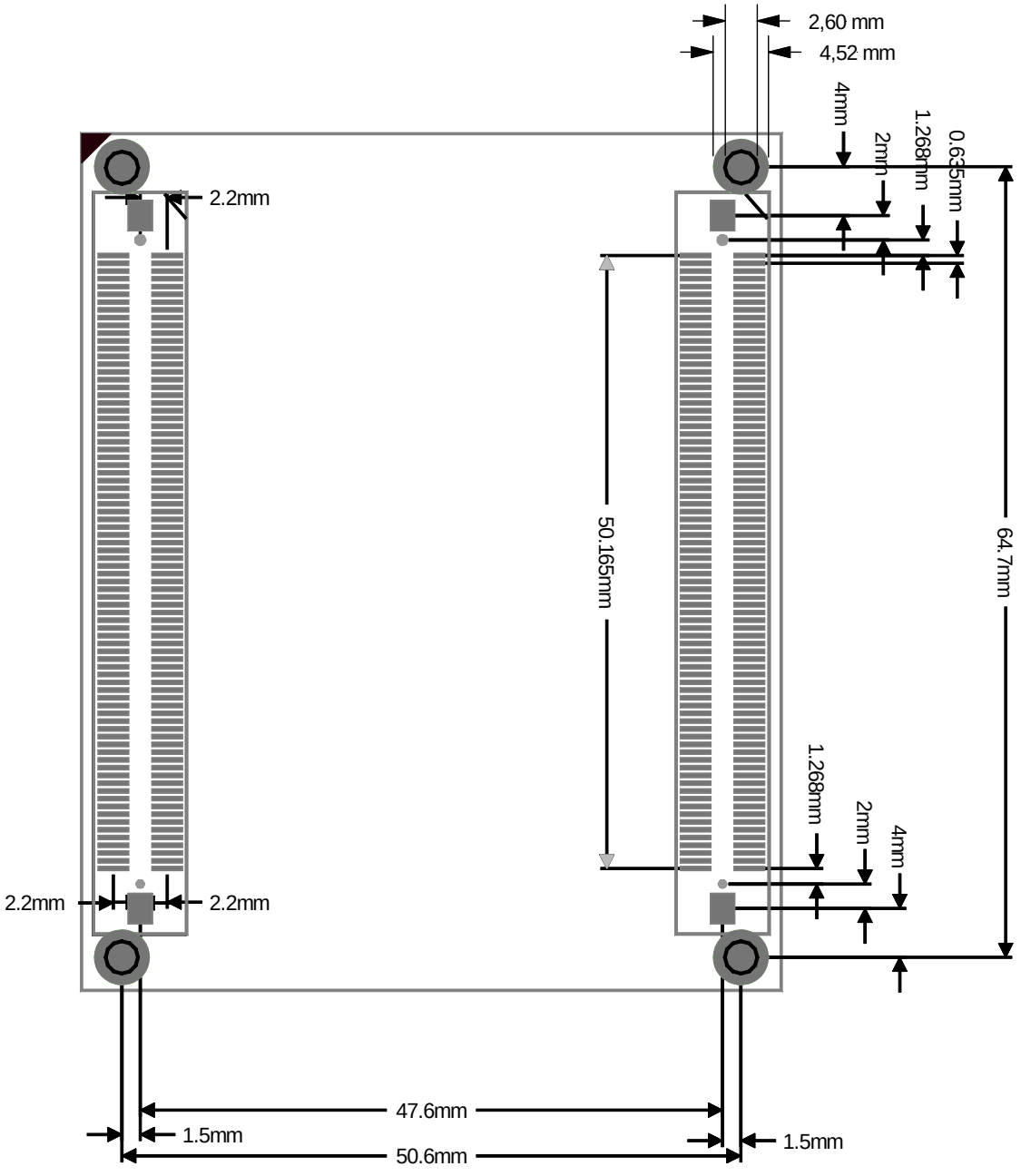


Figure 13: Physical Dimensions (Top View)

The height of all components on the top side of the PCB is ca. 2.5 mm. The PCB itself is approximately 1.6 mm thick. The Molex connector pins are located on the bottom side of the PCB, oriented parallel to its two long sides. The maximum height of components on the bottom side of the PCB is 2.5 mm.

When the phyCORE-Modul is populated on the carrier board the gap between the pcb of the phyCORE-Modul and the pcb of the carrier board is 6 mm because of the plug populated on the carrier board. That implies that the components on the carrier board can have a maximum high of 2.5 mm in respect to the thermal discharge. Optionally, in high increased plugs can be populated on the carrier board resulting in a pcb to pcb gap of 10.0 mm. Thus a maximal component high of 6.5 mm can be achieved.

Please refer to the following chaper *Connectors on the phyCORE-MPC5121e/3 tiny* for more information on the different connectors.

Note:
EMC critical components should not be placed below the phyCORE-Module, e.g.: power supplies, coils, etc.

Additional Technical Data:

Parameter	**Condition**	**Characteristics**
Dimensions		60 mm x 76 mm
Weight		approximately 30g with all optional components mounted on the circuit board
Storage Temp. Range		-40°C to +90°C
Operating Temp. Range: Extended		 -40°C to +85°C
Humidity		max. 95 % r.F. not condensed
Operating voltages: Voltage 3.3V		 3.3 V ±5 %
Power Consumption:	(depending on load)	max. 4.0 watts Operating Conditions: VCC = 3.3V CPU @ 400MHz, 256MB DDR2RAM @ 200MHz, 32MByte NOR, 1GByte NAND, Linux booted

Table 21: Technical *Data*

These specifications describe the standard configuration of the phyCORE-MPC5121e/3-tiny as of the printing of this manual.

Symbol	Description	Conditions	Min	Typ	Max	Unit
VDD_IO_V3V3	Primary SOM input voltage		3.135	3.3	3.465	V
VDD_VBAT_V3V3 [b]	Battery input voltage	MPC5121e on-chip RTC used	3.0	3.3	3.6	V
		off chip I2C RTC used	1.5	3.3	3.6	
ICC	Primary SOM operating current	Core @ 399MHz, 256MB SDRAM @ 200MHz, 16MB NOR, 1 GB NAND, Linux Kernel 2.6.31 booted, Ethernet enabled	-	1.05	-	A
ICCVBAT	Battery operating current	primary SOM input voltage disabled		TBD	-	uA

a. Tamb = -40C to +85C unless otherwise specified.
b. VBAT should always be less than VDD_IO_V3V3 for proper operation when VDD_IO_V3V3 is supplied.
c. Operating limits are per the Freescale MPC5121e datasheet

Connectors on the phyCORE-MPC5121e/3 tiny:

Manufacturer	Molex
Number of pins per contact rows	160 (2 rows of 80 pins each)
Molex part number (lead free)	52760-1679 (receptacle)

Two different heights are offered for the receptacle sockets that correspond to the connectors populating the underside of the phyCORE-MPC5121e/3-tiny. The given connector height indicates the distance between the two connected PCBs when the module is mounted on the corresponding carrier board. In order to get the exact spacing, the maximum component height (2,5 mm) on the bottom side of the phyCORE must be subtracted.

Component height 6 mm

Manufacturer	Molex
Number of pins per contact row	160 (2 rows of 80 pins each)
Molex part number (lead free)	55091-1674 (header)

Component height 10 mm

Manufacturer	Molex
Number of pins per contact row	160 (2 rows of 80 pins each)
Molex part number (lead free)	53553-1679 (header)

Please refer to the corresponding data sheets and mechanical specifications provided by Molex (www.molex.com).

13 Hints for Handling the Module

- **Modifications on the phyCORE Module**

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Caution!
If any modifications to the module are performed, regardless of their nature, the manufacturer guarantee is voided.

- **Integrating the phyCORE-MPC5121e/3-tiny into a Target Application**

Successful integration in user target circuitry greatly depends on the adherence to the layout design rules for the GND connections of the phyCORE module. For best results we recommend using a carrier board design with a full GND layer. It is important to make sure that the GND pins that have neighboring signals which are used in the application circuitry are connected. Just for the power supply of the module at least 8 GND pins that are located right next to the VCC pins must be connected

14 The phyCORE-MPC5121e/3-tiny on the Carrier Board

PHYTEC Carrier Boards are fully equipped with all mechanical and electrical components necessary for the speedy and secure start-up and subsequent communication to and programming of applicable PHYTEC Single Board Computer (SBC) modules. Carrier Boards are designed for evaluation, testing and prototyping of PHYTEC Single Board Computers in laboratory environments prior to their use in customer designed applications.

14.1 Concept of the Carrier Board phyCORE-MPC5121e/3-tiny

The Carrier Board phyCORE-MPC5121e/3-tiny provides a flexible development platform enabling quick and easy start-up and subsequent programming of the phyCORE-MPC5121e/3-tiny Single Board Computer module. The Carrier Board design allows easy connection of additional expansion boards featuring various functions that support fast and convenient prototyping and software evaluation.
This modular development platform concept is depicted in Figure 14 and includes the following components:

- The actual **Carrier Board** (1), which offers all essential components and connectors for start-up including: a power socket enabling connection to an **external power adapter** (2) and **DB-9 connectors** (3) allowing for use of the SBC's serial interfaces with standard cable.
- Most of the signals from the SBC module mounted on the Carrier Board extend to two mating receptacle connectors. The pin assignment of these **expansion bus** (4) depends entirely on the pinout of the SBC module mounted on the Carrier Board.

- As the physical layout of the expansion bus is standardized across all applicable PHYTEC Carrier Boards, we are able to offer various **expansion boards** (5) that attach to the Carrier Board at the **expansion bus connectors** (4). These modular expansion boards offer **supplemental I/O functions** (6) as well as peripheral support devices for specific functions offered by the controller populating the **SBC module** (9) mounted on the Carrier Board.

  - All controller and on-board signals provided by the SBC module mounted on the Carrier Board are broken out 1:1 to the expansion board by means of its **patch field** (7). The required connections between SBC module / Carrier Board and the expansion board are made using **patch cables** (8) included with the expansion board.

Figure 14 illustrates the modular development platform concept:

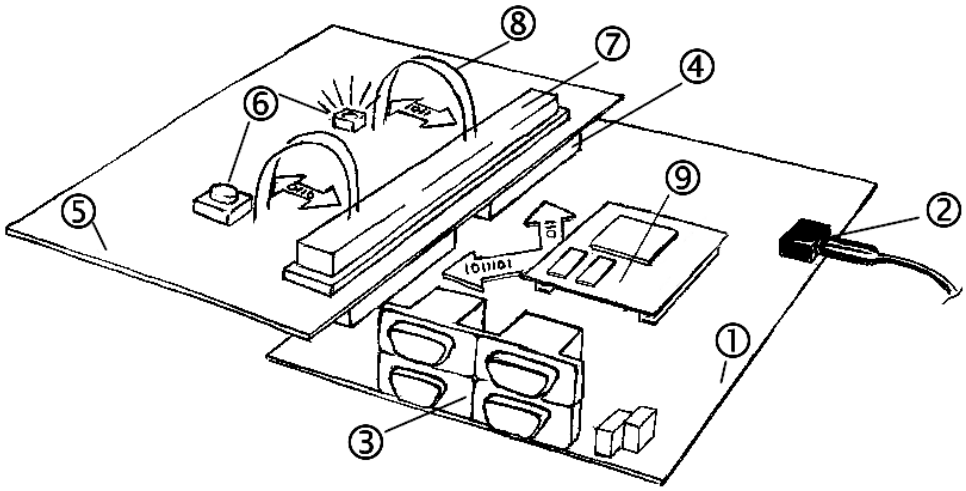


Figure 14: Modular Development and Expansion Board Concept with the phyCORE-MPC121e/3- tiny

The following sections contain specific information relevant to the operation of the phyCORE-MPC5121e/3-tiny mounted on the Carrier Board phyCORE-MPC5121e/3-tiny (PCM-962-tiny).

14.2 Carrier Board phyCORE-MPC5121e/3-tiny Connectors, Jumpers and Switches

14.2.1 Connectors

As shown in *Figure 15* and *Figure 16*, the following connectors are available on the phyCORE Development Board PCM-962-tiny:

Note: Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller Reference Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

X1-	JTAG pin header for CPLD EPM570F256 U8 on the Development Board
X2-	User signals pin header (9 pins; double row male header)
X3-	SD/MMC card slot
X4	combined analogue IO pin header of the WM9712 (U21 on the Development Board)
X5-	combined Audio Interface of the WM9712
X6-	Touch Interface header of the WM9712 JST B5B-EH-A
X8-	USB OTG connector Mini-AB
X9-	SATA connector
X11-	RJ45 Interface for Ethernet connection 10/100MBit
X13-	JTAG pin header for PCI insert card connector X26
X17-	phyCORE-Connector for phyCORE module with 320 pins (e.g. phyCORE-MPC5121e/3-tiny)
X18-	Molex connector for connecting TTL display adapters (e.g. LCD-011 for the Hitachi TX09D70VM1CCA)
X19-	Power jack for supply voltage +9 - +14V

X20- Connector for supply voltage generated by a standard ATX power supply (4 positions)

X21- Connector for supply voltage generated by a standard ATX power supply (24 positions)

X22- LVDS Graphic connector DF19G20P

X23- SMD Touch connector FPC4

X24- LED Backlight Connector

X25- JTAG pin header for MPC5121e/3 controller

X26- PCI connector for compatible 3.3V PCI insert cards (SLOT 0)

X27- PCI connector for compatible 3.3V PCI insert cards (SLOT 1)

X28- Mini PCI ,connector for compatible 3.3V Mini PCI cards

X30- 400-pin mating receptacle for connecting a GPIO expansion board

X31- 3-pin CCFL connector

X32- IDE Interface connector

X33- Compact Flash card socket

P1- dual DB-9 plugs for CAN interface connectivity

P2- dual DB-9 sockets for serial RS232 interface connectivity

GND1 GND connector for measurement purposes

As also shown in Figure 16, the following connectors, jumper and switches (shadowed) are not available on the phyCORE Development Board PCM-962-tiny:

X7- phyCORE-Connector for phyCORE module with 400 pins (e.g. phyCORE-MPC5121e/3)

X10- RJ45 Interface for industrial Ethernet connection 10/100MBit of netX Controller

X12- RJ45 Interface for industrial Ethernet connection 10/100MBit of netX Controller

X14- USB Host interface of netX-Controller

X15- JTAG pin header of netX Controller

X29- DB-9 female connector for serial RS232 interface connectivity with netX Controller

JP9- Jumper for enabling USB power supply netX50

JP12- Jumper for connecting over current signal USB interface netX50

S3- Boot button for netX50 controller

Note:

A detailed description of the assembled connectors, jumpers and switches is explained in the following functional structured chapters.

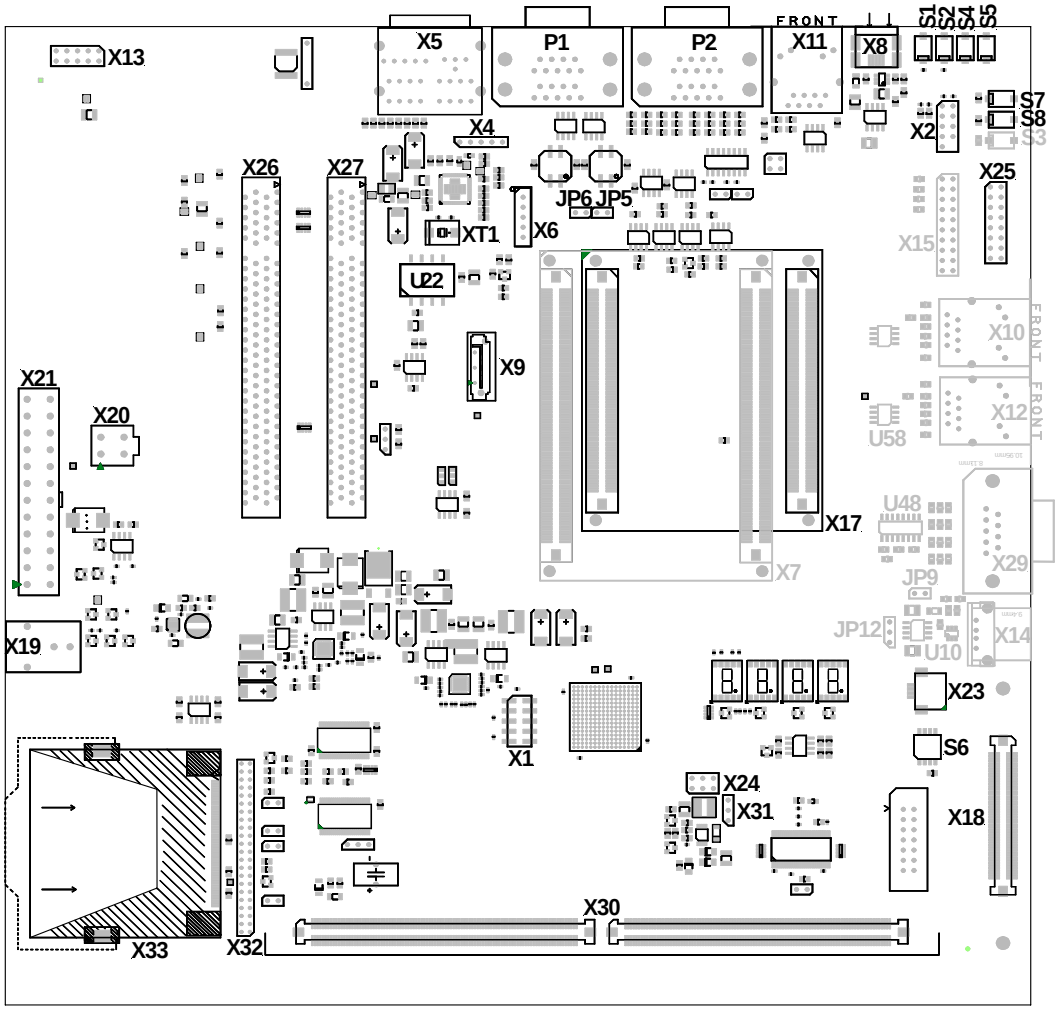


Figure 15: Location of Connectors on the phyCORE-MPC-5121e/3-tiny Carrier Board - top side

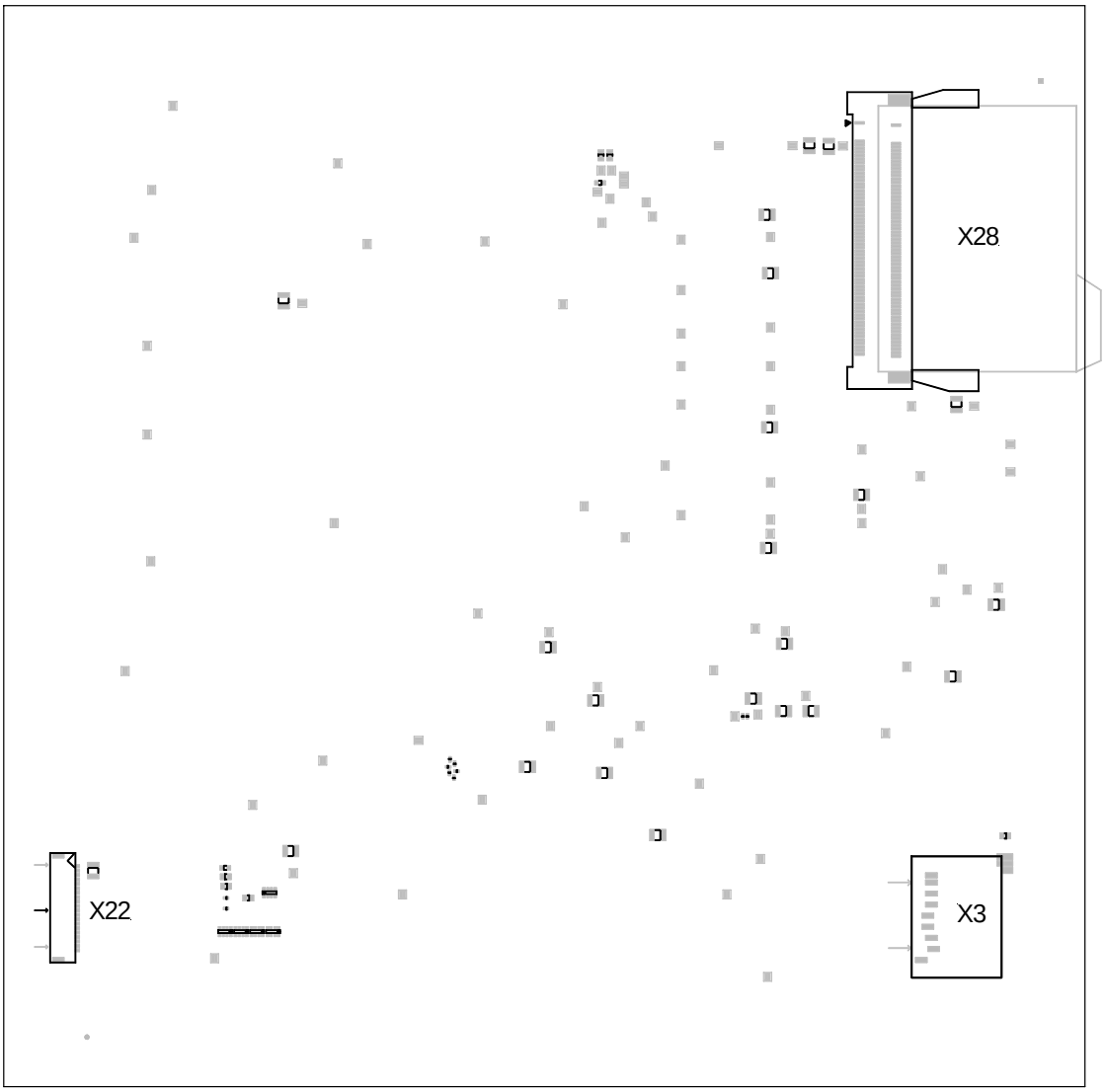


Figure 16: Location of Connectors on the phyCORE-MPC-5121e/3-tiny Carrier Board - bottom side

14.2.2 Jumpers on the Carrier Board phyCORE-MPC5121e/3-tiny

Peripheral components of the phyCORE-MPC5121e/3-tiny Carrier Board can be connected to the signals of the phyCORE-MPC5121e/3-tiny by setting the applicable jumpers.

The Carrier Board's peripheral components are configured for use with the phyCORE-MPC5121e/3-tiny by means of removable jumpers. If no jumpers are set, the serial interface signals are connected to the DB-9 connectors at P1, whereas the control and display units and the CAN transceivers are unconnected. The Reset input on the phyCORE-MPC5121e/3-tiny connects to the Reset button (S5) via the CPLD U8. Figure 17 illustrates the numbering of the jumper pads, while Figure 18 indicates the location of additional jumpers on the Carrier Board.

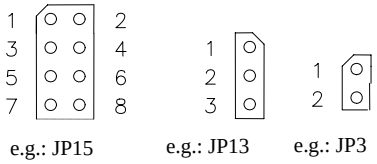


Figure 17: Numbering of the Jumper Pads

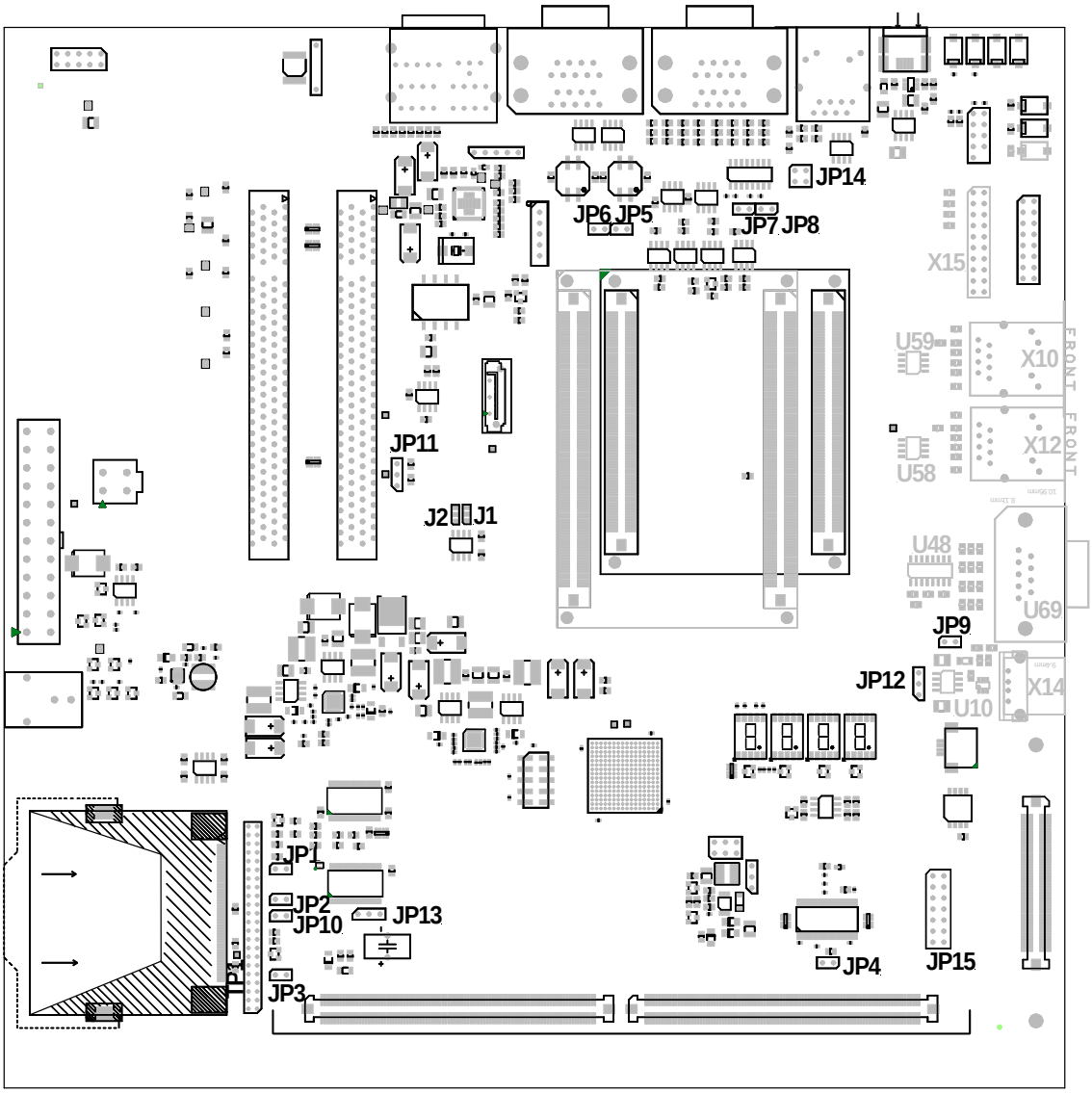


Figure 18: Location of the Jumpers (View of the Component Side)

Figure 19 shows the factory default jumper settings for operation of the phyCORE-MPC5121e/3-tiny Carrier Board with the standard phyCORE-MPC5121e/3-tiny (standard = MPC5121e controller, use of first and second RS-232, both CAN interfaces on the Carrier Board). Jumper settings for other functional configurations of the phyCORE-MPC5121e/3 tiny module mounted on the Carrier Board are described in the following sections.

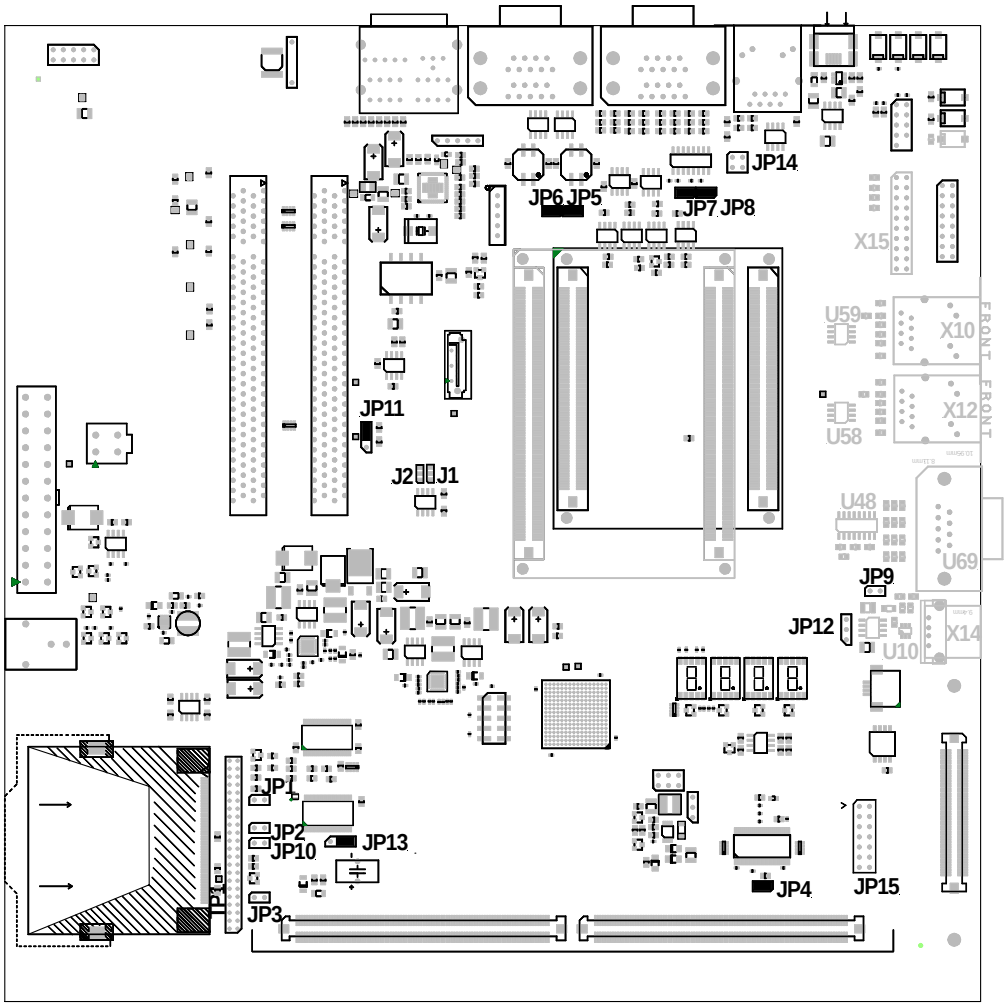


Figure 19: Default Jumper Settings of the phyCORE Development Board MPC5121e/3-tiny with phyCORE-MPC5121e-tiny

14.2.3 Switches and Buttons on the Carrier Board phyCORE-MPC5121e/3-tiny

The phyCORE-MPC5121e/3-tiny Development Board is populated with some switches which are essential for the operation of the phyCORE-Module on the Development Board. These switches are described in the following:

Switch	Description
S1	User Button - freely available for user defined functions
S2	User Button - freely available for user defined functions
S4	Power Button – powering on and off main supply voltages of the Development Board
S5	System Reset Button – system reset signal generation
S6	Display Configuration Switch – display configuration
S7	Configuration of the default reset vector address of the MPC512x processor at startup – NOR Flash low boot option
S8	Configuration of the default reset vector address of the MPC512x processor at startup – NAND Flash boot option

Table 22: Switches of the phyCORE-*MPC5121e/3 Carrier Board*

14.2.4LEDs on the Carrier Board phyCORE-MPC5121e/3-tiny

The phyCORE-MPC5121e/3-tiny Development Board is populated with some LEDs which are helpful in operation of the phyCORE-Module on the Development Board. These LEDs are described in the following:

LED	Description
D4	The LED indicates the supply Voltage VCC12V0 if carrier board is suppied through X19. The LED will remain off by powering the board with a standard atx power supply.
D6	The LED indicates the VCC5V0STBY supply voltage
D8	The LED indicates the VCC3V3PCI supply voltage
D14	The LED indicates the VCC3V3 supply voltage
D15	The LED indicates the status of the cplds /USER_LED0 output
D16	The LED indicates the PATA activity of the hard disk interface
D17	The LED indicates the PATA activity of the compact flash interface
D18	The LED indicates the VCCLCD3V3 supply voltage
D19	The LED indicates the VCCLCD5V0 supply voltage
D20	The LED indicates the VCC3VSTBY supply voltage
D21	The LED indicates the VCC5V0 supply voltage
D23	The LED indicates the status of the cplds /USER_LED1 output

Table 23: LEDs of the phyCORE-*MPC5121e/3 Carrier Board*

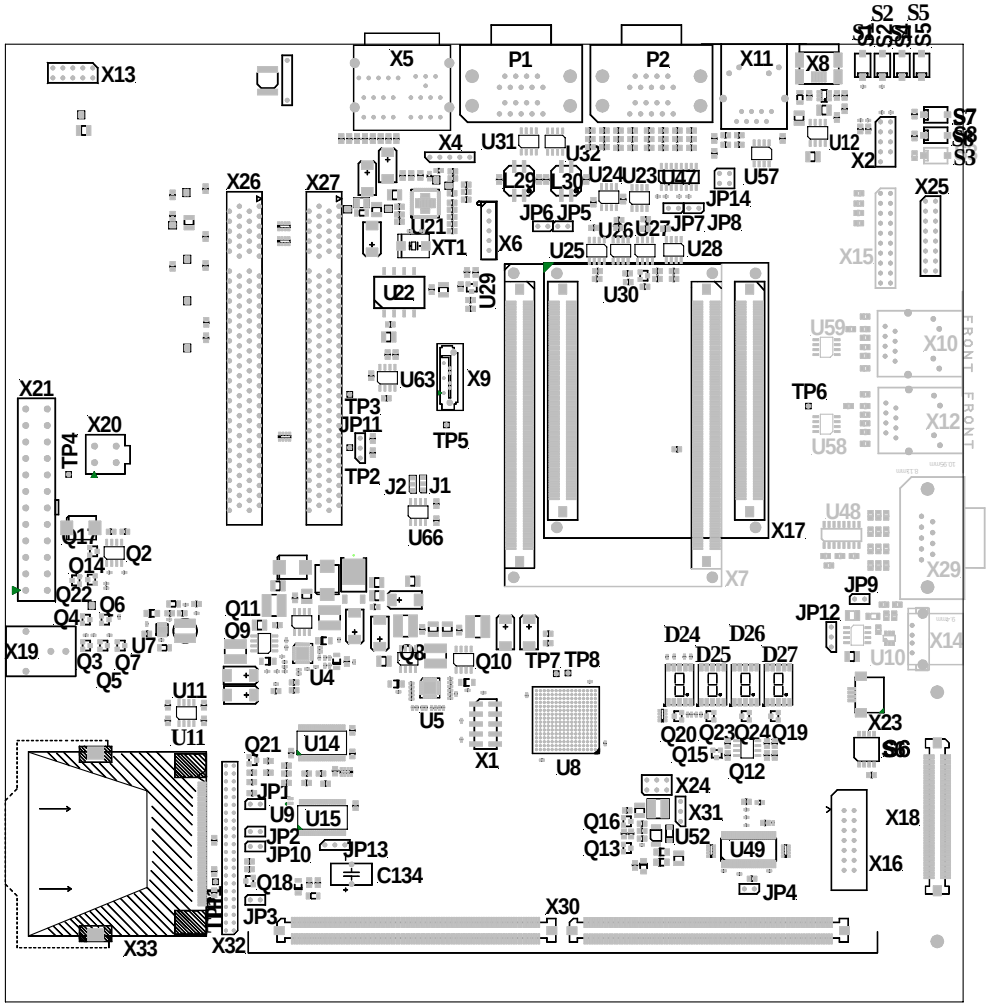


Figure 20: Location of the Switches Buttons and LEDs on the phyCORE Development Board MPC5121e/3-tiny

14.3 Functional Components on the phyCORE-MPC5121e/3-tiny Carrier Board

This section describes the functional components of the phyCORE-MPC5121e/3-tiny Carrier Board supported by the phyCORE-MPC5121e/3-tiny and appropriate jumper settings to activate these components. Depending on the specific configuration of the phyCORE-MPC5121e/3-tiny module, alternative jumper settings can be used. These jumper settings are different from the factory default settings as shown in Figure 19 and enable alternative or additional functions on the phyCORE-MPC5121e/3tiny Carrier Board depending on user needs.

14.3.1 Used miscellaneous Signals of the phyCORE-MPC5121e/3-tiny on the Carrier Board

For implementation of additional functions on the Carrier Board of the phyCORE-MPC5121e/3-tiny a set of IO-Signals of the phyCORE-module is used which are not describe in the following sections. These signals are necessary to ensure proper operation of the phyCORE-MPC5121e/3 on the Carrier Board PCM-962-tiny and can't be used for further functions in this constellation. Will the phyCORE-MPC5121e/3 be used in a customized environment the signals will unrestricted be available for custom implementations.

The following table specifies the used peripheral signals of the phyCORE-MPC5121e/3 tiny on the Carrier Board PCM-962-tiny with their corresponding functions:

phyCORE-Signal	Functional usage on the Carrier Board
PSC3_4	Connected to Chip Select Signal of CPLD U8
/IRQ0	Connected to CPLD U8 Interrupt Signal output

Table 24: Used phyCORE-Signals on the Carrier Board

The phyCROE-MPC5121e/3-tiny carrier board is an assistive equipment for starting up with the phyCORE-MPC5121e/3. For this the carrier board comes with a set of functions which are supported by the phyCORE-Modul and makes so the signals unavailable for custom usage.

The following table specifies the used peripheral sections of the phyCORE-MPC5121e/3 tiny on the Carrier Board PCM-962-tiny with their corresponding functions:

CPU Port	Function	Used on phyCORE SBC	Used on carrier board
PSC0,1,2	Ethernet	Yes	Yes
PSC3	UART3	Yes	Yes
PSC4	AC97	No	Yes
PSC5	GPIO	No	No
PSC6	UART6/DIU	Yes	Yes
PSC7...11	DIU	No	Yes
USB	USB OTG	No	Yes
CAN	dedicated	No	Yes
J1850	dedicated	No	No
I2C0	dedicated	Yes	Yes
I2C1 / I2C2	dedicated	No	No

Table 25: Used phyCORE-Sections on the Carrier Board

14.3.2 Power Supply at X19, X20, X21 and Power LEDs

Caution:
Only use the included power adapter at X19 to supply power to the Carrier Board! Do not change modules or jumper settings while the Carrier Board is supplied with power!

Permissible input voltage at X19: +9 - +14 V DC unregulated.

The required current load capacity of the power supply depends on the specific configuration of the phyCORE-MPC5121e/3-tiny mounted on the Carrier Board as well as whether an optional expansion board is connected to the Carrier Board. An adapter with a minimum supply of 2.0 A is recommended.

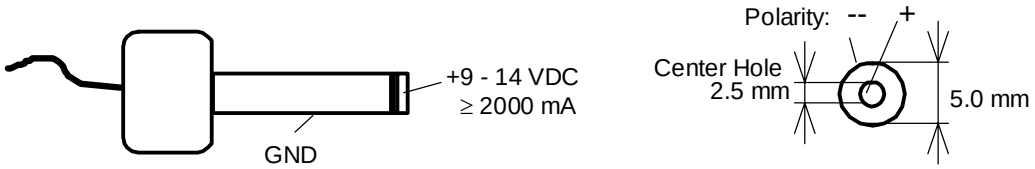


Figure 21: Connecting the Supply Voltage at X19

No jumper configuration is required in order to supply power to the phyCORE-MPC5121e/3-tiny module!

Connector X20 and X21 allow for powering the Development Board PCM-962-tiny with a standard ATX power supply.

The Carrier Board phyCORE-MPC5121e/3-tiny is assembled with a few power LEDs whose functions are described in the following table:

LEDs	Description
D4	LED to indicate VCC12V0 is powered on
D6	LED to indicate VCC5V0STBY is powered on
D8	LED to indicate VCC3V3PCI is powered on
D14	LED to indicate VCC3V3 is powered on
D20	LED to indicate VCC3V3STBY is powered on
D21	LED to indicate VCC5V0 is powered on

Table 26: LEDs assembled on the Carrier Board

Note:
For powering up the phyCORE-MPC5121e/3-tiny the following actions have to be done:

1. Plug in the power supply connector
   » The Standby LEDs D6 and D20 of the Development Board should light up
2. Press button S4 for a minimum time of 1000ms seconds.
   » All power LEDs should light up and the phyCORE-MPC5121e/3-tiny puts serial output to serial line 0 at P2A.

For powering down the phyCORE-MPC5121e/3-tiny button S4 should be pressed for a minimum time of 5000ms.

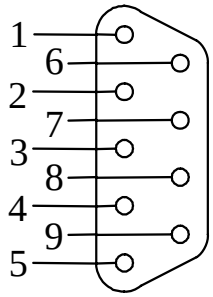
14.3.3 First Serial Interface at Socket P2A

Female connector P2A is the lower connector of the double DB-9 connector at P2. P2A is directly connected to the serial RX and TX lines of the module's serial interface PSC3. The only signal configurable with Jumper JP14 is PSC3_1 (CTS) coming from PSC3 on the MPC5121e/3.

Jumper	Setting	Description
JP14	1+2	Signal PSC3_1 (CTS) is connected to the RS-232 transceiver U47 on the phyCORE-MPC5121e/3-tiny Carrier Board, interface signals with RS-232 level are available at connector P2A
JP14	open*	PSC3_1 (CTS) signal is freely available at X1D26

**- default*

Table 27: Jumper Configuration for the First RS-232 Interface



Pin 2: TxD3-RS232
Pin 7: CTS3-RS232
Pin 3: RxD3-RS232
Pin 8: CTS3-RS232

Pin 5: GND

Figure 22: Pin Assignment of the DB-9 female connector P2A as RS-232 interface(PSC3) - (Front View)

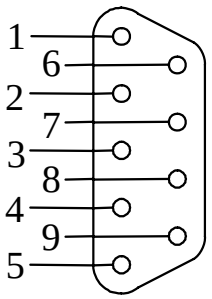
14.3.4 Second Serial Interface at Socket P2B

Female connector P2B is the upper connector of the double DB-9 connector at P2. P2B is connected directly to the RX and TX lines of the module's serial interface PSC6. The only signal configurable with Jumper JP14 is PSC6_1 (CTS) coming from PSC6 on the MPC5121e/3.

Jumper	Setting	Description
JP14	3 + 4	Signal PSC6_1 (CTS) is connected to the RS-232 transceiver U47 on the phyCORE-MPC5121e/3-tiny Carrier Board, interface signals with RS-232 level are available at connector P2B
JP14	open*	PSC6_1 (CTS) signal is freely available at X1D63

** - default*

Table 28: Jumper Configuration of the DB-9 female connector P2B (PSC6)



Pin 2: TxD6_RS232
Pin 7 : CTS6_RS232
Pin 3: RxD6_RS232
Pin 8: RTS6_RS232

Pin 5: GND

Figure 23: Pin Assignment of the DB-9 female connecP2B as second RS-232 interface (PSC6) - (Front View)

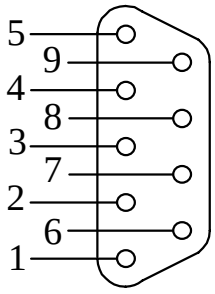
14.3.5 First CAN Interface at Plug P1A

Male connector P1A is the lower connector of the double DB-9 connector at P1. P1A is connected to the first CAN interface (CAN1) of the phyCORE-MPC5121e/3-tiny via jumpers. There are no CAN transceivers available on the phyCORE-MPC5121e/3-tiny therefore the transceivers on the Carrier Board must be used.

CAN signals generated by the Carrier Board's CAN transceiver (U23) extend to connector P1A **with galvanic separation:**

Jumper	Setting	Description
JP7	**closed**	Input of the optocoupler U27 on the Carrier Board connected to CAN1_TX signal from the phyCORE-MPC5121e/3-tiny
JP8	**closed**	Output of the optocoupler U28 on the Carrier Board connected to CAN1_RX signal of the phyCORE-MPC5121e/3-tiny

Table 29: Jumper Configuration for CAN male connector P1A using the CAN transceiver on the Carrier Board



Pin 3: GND (Carrier Board Ground)
Pin 7: CAN_H1 (with galvanic separation)
Pin 2: CAN_L1 (with galvanic separation)
Pin 6: GND (Carrier Board Ground)

Figure 24: Pin Assignment of the DB-9 male connector P1A (CAN transceiver on Carrier Board)

Caution:
When using the DB-9 connector P1A as CAN interface and the CAN transceiver on the Carrier Board the following jumper settings are not functional and could damage the module:

Jumper	Setting	Description
JP7	open	CAN1_TX signal not connected to transceiver, no CAN communication is possible
JP8	open	CAN1_RX signal not connected to transceiver, no CAN communication is possible

Table 30: Improper Jumper Settings for the CAN male connector P1A (CAN transceiver on the Carrier Board)

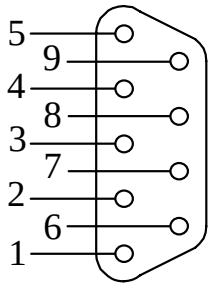
14.3.6 Second CAN Interface at Plug P1B

Male connector P1B is the upper connector of the double DB-9 connector at P1. P1B is connected to the second CAN interface (CAN2) of the phyCORE-MPC5121e/3-tiny via jumpers. There are no CAN transceivers available on the phyCORE-MPC5121e/3-tiny therefore the transceivers on the Carrier Board must be used.

CAN signals generated by the Carrier Board's CAN transceiver (U24) extend to connector P1B **with galvanic separation:**

Jumper	Setting	Description
JP6	**closed**	Input of the optocoupler U26 on the Carrier Board connected to CAN2_TX signal from the phyCORE-MPC5121e/3-tiny
JP5	**closed**	Output of the optocoupler U25 on the Carrier Board connected to CAN2_RX signal of the phyCORE-MPC5121e/3-tiny

Table 31: Jumper Configuration for CAN male connector P1B using the CAN Transceiver on the Carrier Board



Pin 3: GND (Carrier Board Ground)
Pin 7: CAN_H2 (no galvanic separation)
Pin 2: CAN_L2 (no galvanic separation)
Pin 6: GND (Carrier Board Ground)

Figure 25: Pin Assignment of the DB-9 male connector P1B (CAN transceiver on Carrier Board)

Caution:
When using the DB-9 connector P1B as second CAN interface and the CAN transceiver on the Carrier Board the following jumper settings are not functional and could damage the module:

Jumper	Setting	Description
JP6	open	CAN2_TX signal not connected to transceiver, no CAN communication possible
JP5	open	CAN2_RX signal not connected to transceiver, no CAN communication possible

Table 32: Improper Jumper Settings for the CAN male connector P1B (CAN transceiver on the Carrier Board)

14.3.7 Programmable LEDs D15 and D23

The phyCORE Carrier Board MPC5121e/3-tiny offers two programmable LEDs at D15 and D23 for user applications. These LEDs are connected to port pins of the CPLD U8. A low-level at applicable port pin causes the LEDs to illuminate, The LEDs D15 and D23 remain off when writing a high-level. There is no jumper setting necessary for illuminating the user LEDs.

The LEDs can be illuminated by writing to offset 0x04 bit 6 and bit 7 at /CS6 of the MPC5121e/3. A low level written into register offset 0x04 bit 6 illuminates LED D23, writing a high level causes the led to remain off. A low level written into register offset 0x04 bit 7 illuminates LED D15, writing a high level causes the led to remain off.

14.3.8 Ethernet Interface X11

The Ethernet interface of the phyCORE-MPC5121e/3-tiny is accessible at an RJ45 connector (X11) on the Carrier Board. Due to its characteristics this interface is hard-wired and can not be configured via jumpers. The LEDs for LINK and SPEED indication are integrated in the connector.

14.3.9 USB OTG Interface X8

The USB OTG interface of the phyCORE-MPC5121e/3-tiny is accessible at the Mini-AB OTG connector X8 on the Carrier Board. This interface is compliant with USB revision 2.0.

No jumper settings are necessary for using the USB OTG port.

14.3.10 SATA Interface X9

The SATA interface of the phyCORE-MPC5121e/3-tiny is accessible at connector X9 on the Carrier Board. This interface is compliant with SATA revision 1.0a.

No jumper settings are necessary for using the SATA port. The following table describes the signal configuration at X9

Location	Signal	Description
X9-1, X9-4, X9-7	GND	GND
X9-2	SATA_TXP	positive differential SATA transmit signal
X9-3	SATA_TXN	negative differential SATA transmit signal
X9-5	SATA_RXP	positive differential SATA receive signal
X9-6	SATA_RXN	negative differential SATA receive signal

Table 33: SATA Interface Connector Configuration

14.3.11 CPU JTAG Interface X25

The JTAG interface of the phyCORE-MPC5121e/3-tiny is accessible at connector X25 on the Carrier Board. This interface is compliant with JTAG specification IEEE 1149.1.

No jumper settings are necessary for using the JTAG port. The following table describes the signal configuration at X25

Location	Signal	Description
X25-1	JTAG_TDO	JTAG Chain Data Output
X25-2, X25-5, X25-8, X25-10, X24-14	NC	*Not connected*
X25-3	JTAG_TDI	JTAG Chain Data input
X25-4	/JTAG_TRST	JTAG Chain Test Reset
X25-6	VCC3V3	JTAG Chain reference voltage
X25-7	JTAG_TCK	JTAG Chain Clock signal
X25-9	JTAG_TMS	JTAG Chain Test Mode Select signal
X25-11	/SRESET	CPU Software Reset output
X25-12, X25-16	GND	GND
X25-13	/HRESET	bidirectional CPU Hardware Reset
X25-15	/JTAG_ CKSTP_O	output of the JTAG Chain Clock Stop signal

Table 34: JTAG Interface Connector Configuration

14.3.12 Audio Interface

The AC97 interface on the phyCORE-MPC5121e/3-tiny connects to a Wolfson WM9712L audio codec controller on the Carrier Board. A variety of signals generated by the WM9712 IC are available at the different sections of audio connector X5 and the 5-pin male header rows X4 and X6. Figure 26 shows the audio codec connector X5 and its numbering scheme.

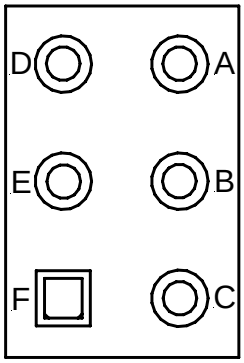


Figure 26: X5 - Audio Connector numbering scheme (front view)

Audio Outputs:

- X5B - Speaker Output - LOUT2/ROUT2
- X5C - Headphone Output - HPOUTL/HPOUTR/HPCRTL
- X5F - SPDIF Output - SPDIF

Audio Inputs:

- X5D - Auxiliary Input - AUX1/AUX2
- X5A - Microphone Inputs - MIC1/MIC2
- X5E - Line Inputs - LINE IN R/L

Connector X4 and X6 are supporting additional signals provided by the audio codec.

X4 supports additional audio signals:

- X4-1 - Mono Out
- X4-2 - OUT3
- X4-3 - PCBeep Input
- X4-4 - PHONE Input
- X4-5 – AGND

X6 supports the 4- and 5-wire touch panel interface signals:

- X6-1 - Left side touch contact - X-
- X6-2 - Top side touch contact - Y+
- X6-3 - Bottom side touch contact - Y-
- X6-4 - Right side touch contact - X+
- X6-5 - AUX4

Please refer to the audio codec's reference manual for additional information regarding the special interface specification.

14.3.13 Compact Flash Card Socket X33

The phyCORE-MPC5121e/3-tiny Carrier Board provides a Compact Flash (CF) card socket at X33. CF cards used in this socket can only be operated in IDE mode. Activity on the CF card socket is indicated by LED D17. Jumpers JP2, JP3 and JP10 are available for configuration of the Compact Flash card interface. The following configuration options are possible:

Jumper	Setting	Description
JP3	**open**	Compact Flash card write protection not active
	closed	Compact Flash card write protection active
JP2	**open**	Compact Flash card write enable not active
	closed	Compact Flash card write enable active
JP10	**open**	Compact Flash slave mode selected
	closed	Compact Flash master mode selected
JP13	**open**	The secondary side of the PATA bus transceivers are not supplied with power
	1 + 2	Secondary side of the PATA bus transceiver is supplied with 5,0V so only 5V CF-Cards can be used
	2 + 3	Secondary side of the PATA bus transceiver is supplied with 3,3V so only 3,3V CF-Cards can be used

Table 35: JP2, JP3, JP10 and JP13 - CF Card Interface Configuration

Due to the multiplexed function of the PATA control signals the Compact Flash Card Socket can only be used if no SDHC interface card is inserted. Inserting a SDHC interface card will disable the Compact Flash Card Socket.

14.3.14 IDE Interface X32

The phyCORE-MPC5121e/3-tiny Carrier Board provides an IDE interface header at X32 for connection to external 2.5” hard disks. The 44-pin header connector in 2.0 mm pin spacing allows easy and convenient connection to peripheral devices using a ribbon cable. Activity on the IDE socket is indicated by LED D16. Due to the multiplexed function of the PATA control signals the IDE Interface can only be used if no SDHC interface card is inserted. Inserting a SDHC interface card will disable the IDE hardware interface.

Jumper	Setting	Description
JP1	**open**	Selecting 8bit data bus width for PATA transfers
	closed	Selecting 16bit data bus width for PATA transfers
JP13	**open**	The secondary side of the PATA bus transceivers are not supplied with power
	1 + 2	Secondary side of the PATA bus transceivers are supplied with 5,0V so only 5V compatible hard disks can be attached
	2 + 3	Secondary side of the PATA bus transceivers are supplied with 3,3V so only 3,3V compatible hard disks can be attached

Table 36: JP1 and JP13 - IDE Interface Configuration

14.3.15 SDHC Interface X3

The phyCORE-MPC5121e/3-tiny Carrier Board provides a standard SDHC card slot at X3 for connection to SDHC interface cards. It allows easy and convenient connection to peripheral devices like SDHC- and MMC cards. Power to the SDHC interface is supplied by sticking the appropriate card into the SDHC slot. Due to the multiplexed function of the PATA/SDHC Interface and the higher priority of the SDHC interface, the SDHC Interface card slot can be used by plugging in an SDHC interface card without further user actions. Inserting a SDHC interface card will then disable the IDE hardware interface.

14.3.16 PCI Card Slot X26 and X27

The phyCORE-MPC5121e/3-tiny Carrier Board provides two 3.3V PCI interface connectors at X26 and X27 which are directly connected to the PCI interface of the phyCORE-MPC5121e/3-tiny. All common 3.3V PCI insert cards can be used in this slots allowing the user to add additional interface features to this hardware platform. Pin adaption of the PCI-connectors is realized as describe in the appropriate PCI-specification. Configuration of the PCI interfaces can be done by the following jumper.

Jumper	Setting	Description
JP11	open	**not allowed, jumper should always be configured when using PCI interface**
	1 + 2	PCI interface card slots X26 and X27 configured for 66MHz Operation – depends on the functionality of the card inserted
	2 + 3	PCI interface card slots X26 and X27 configured for 33MHz Operation

Table 37: JP11 - PCI Interface Configuration

The 10-pin double row male header X13 functions as PCI-JTAG connector which facilitates debugging of the PCI interface card's functions at X26. This debug functionality depends on the features of the appropriate PCI card inserted. Connector X13 supports the following signals:

Location	Signal	Description
X13-1	PCI_TCK	JTAG test clock input PCI
X13-3	PCI_TMS	JTAG test mode select input
X13-5	PCI_TDI	JTAG test data input
X13-7	PCI_TDO	JTAG test data output
X13-9	/PCI_TRST	JTAG test reset input (low active)
X13-2 X13-4 X13-8	GND	Ground connections
X13-6	VCC3V3PCI	JTAG test interface reference voltage 3.3V
X13-10	NC	No signal connected

Table 38: X13 – PCI-JTAGDebug Interface

Note:
The current draw of the PCI application in combination with the power consumption of all other circuitry used at the same time must not exceed the allowed maximum current draw for the phyCORE-MPC5121e/3-tiny and Carrier Board hardware combination.

14.3.17 Mini-PCI Card Slot X28

The phyCORE-MPC5121e/3-tiny Carrier Board provides a 3.3V Mini-PCI interface connector at X28 which is directly connected to the PCI interface of the phyCORE-MPC5121e/3-tiny. All common 3.3V Mini-PCI insert cards can be used in this slots allowing the user to add additional interface features to this hardware platform. Pin adaption of the Mini-PCI-connector is realized as describe in the appropriate specification. Configuration of the Mini-PCI interfaces via jumpers is not necessary.

Note:
The current draw of the Mini-PCI application in combination with the power consumption of all other circuitry used at the same time must not exceed the allowed maximum current draw for the phyCORE-MPC5121e/3-tiny and Carrier Board hardware combination.

14.3.18 Display Interfaces of the Carrier Borad phyCORE-MPC5121e/3-tiny

14.3.18.1 LVDS Display Interface X22

The phyCORE-MPC5121e/3-tiny Carrier Board provides a 3.3V LVDS Display interface connector at X22 (connector type: DF19G20P). The LVDS signals provided at X22 are generated by a TTL to LVDS converter at U49. Configuration of the LVDS interfaces is possible via jumper JP15 and JP4. The following table describes the signal configuration at X22.

Location	Jumper JP15	Signal	Description
X22-1 X22-2	-	VCC	3,3V supply voltage
X22-3 X22-4 X22-7 X22-10 X22-11 X22-13 X22-21 X22-22	-	GND	GND
X22-5	-	TXOUT0-	Negative LVDS differential data output 0
X22-6	-	TXOUT0+	Positive LVDS differential data output 0
X22-8	-	TXOUT1-	Negative LVDS differential data output 1
X22-9	-	TXOUT1+	Positive LVDS differential data output 1
X22-11	-	TXOUT2-	Negative LVDS differential data output 2
X22-12	-	TXOUT2+	Positive LVDS differential data output 2

X22-14	-	TXCLK OUT-	Negative LVDS differential clock output
X22-15	-	TXCLK OUT+	Positive LVDS differential clock output
X22-16	open	*NC*	*No signal connected*
	1 + 2	DDC_ CLOCK	Free available DDC_Clock signal from pin B72 of the expansion connector X30
	1 + 3	GND	GND
X22-17	open	*NC*	*No signal connected*
	6 + 4	TXOUT3-	Negative LVDS differential data output 3
	6 + 5	DIU_U_D	Signal DIU_U_D from switch 1 of Dip Switch S6
X22-18	open	*NC*	*No signal connected*
	7 + 8	TXOUT3+	Positive LVDS differential data output 3
	7 + 9	DIU_L_R	Signal DIU_L_R from switch 2 of Dip Switch S6
X22-19	open	*NC*	*No signal connected*
	13 + 14	GND	GND
	13 + 11		
X22-20	open	*NC*	*No signal connected*
	12 + 10	DDC_ DATA	The free available DDC_DATA signal from pin B73 of the expansion connector X30
	12 + 11	GND	GND

Table 39: Pin-out and configuration of LVDS display interface at X22

Configuration of the strobe select signal of the LVDS converter is possible via Jumper JP4. This jumper configures the strobe signal of the TTL based display signals and has to be configured as the signal is programmed by the processors display interface registers. The strobe signal is programmed as falling edge strobe in the default uboot so that jumper JP4 has to be closed for normal operation.

Jumper JP4	Description
open	Rising edge strobe configured for U49
closed	Falling edge strobe configured for U49

Table 40: JP4 – *Configuration* of LVDS converter

Note:
The current draw of the LVDS-Display application in combination with the power consumption of all other circuitry used at the same time must not exceed the allowed maximum current draw for the phyCORE-MPC5121e/3-tiny and Carrier Board hardware combination.

14.3.18.2 TTL Display Interface X18

The phyCORE-MPC5121e/3-tiny Carrier Board provides a 3.3V TTL Display interface connector at X18 (MOLEX, 55091-1079) which allows direct connection between an appropriate display adaptor card and the display interface unit of the phyCOE-MPC5121e/3-tiny. Some display adaptors are available at Phytec, e.g. LCD-011.
Configuration of the TTL interfaces via jumper is not necessary. The following table describes the pin out of X18.

Location	Signal	Description
X18A43, X18A44, X18B43, X18B44	VCCLCD3V3	3,3V supply voltage
X18A46, X18A47, X18B46, X18B47	VCCLCD5V0	5,0V supply voltage
X18A1, X18A6, X18A11, X18A16, X18A21, X18A26, X18A31, X18A36,	GND	GND

X18A42, X18A45, X18A48, X18B3, X18B8, X18B13,X18B18, X18B23, X18B28, X18B33, X18B38, X18B42, X18B45, X18B48, X18S1, X18S2, X18S3, X18S4		
X18A2	DIU_HSYNC	Horizontal synchronization signal
X18A3	DIU_VSYNC	Vertical synchronization signal
X18A4	DIU_R0	Display Interface Unit red bit[0]
X18A5	DIU_R2	Display Interface Unit red bit[2]
X18A7	DIU_R4	Display Interface Unit red bit[4]
X18A8	DIU_R6	Display Interface Unit red bit[6]
X18A12	DIU_B1	Display Interface Unit blue bit[1]
X18A13	DIU_B3	Display Interface Unit blue bit[3]
X18A14	DIU_B5	Display Interface Unit blue bit[5]
X18A15	DIU_B7	Display Interface Unit blue bit[7]
X18A19	DIU_G0	Display Interface Unit green bit[0]
X18A20	DIU_G2	Display Interface Unit green bit[2]
X18A22	DIU_G4	Display Interface Unit green bit[4]
X18A23	DIU_G6	Display Interface Unit green bit[6]
X18A27	I2C2_SCL	I2C Interface Clock
X18A28	I2C2_SDA	I2C Interface Data
X18A37	DIU_ENA	Display Interface Enable from switch 4 of Dip Switch S6
X18A49	TOUCHXP	Four Wire Touch Interface – Right side Touch contact
X18A50	TOUCHXM	Four Wire Touch Interface – Left side Touch contact
X18B1	DIU_CLK	Display Interface Unit Clock
X18B2	DIU_DE	Display Interface Unit Data Enable
X18B4	DIU_R1	Display Interface Unit red bit[1]

X18B5	DIU_R3	Display Interface Unit red bit[3]
X18B6	DIU_R5	Display Interface Unit red bit[5]
X18B7	DIU_R7	Display Interface Unit red bit[7]
X18B11	DIU_B0	Display Interface Unit blue bit[0]
X18B12	DIU_B2	Display Interface Unit blue bit[2]
X18B14	DIU_B4	Display Interface Unit blue bit[4]
X18B15	DIU_B6	Display Interface Unit blue bit[6]
X18B19	DIU_G1	Display Interface Unit green bit[1]
X18B20	DIU_G3	Display Interface Unit green bit[3]
X18B21	DIU_G5	Display Interface Unit green bit[5]
X18B22	DIU_G7	Display Interface Unit green bit[7]
X18B32	DIU_BRIGHT	Display Interface Unit brightness control signal, available from CPLD
X18B34	DIU_U_D	Display Interface Unit – Vertical display mode select signal from switch 1 of Dip Switch S6
X18B35	DIU_L_R	Display Interface Unit – Horizontal display mode select signal from switch 2 of Dip Switch S6
X18B36	DIU_V_Q	Display Interface Unit – VGA/QVGA display mode select signal from switch 3 of Dip Switch S6
X18B49	TOUCHYP	Four Wire Touch Interface – Top side Touch contact
X18B50	TOUCHYM	Four Wire Touch Interface – Bottom side Touch contact

Table 41: Pin-Out of the TTL Display Connector X18

Note:
The current draw of the TTL-Display application in combination with the power consumption of all other circuitry used at the same time must not exceed the allowed maximum current draw for the phyCORE-MPC5121e/3-tiny and Carrier Board hardware combination.

14.3.18.3 Powering display interfaces

Powering display interfaces of the carrier board is independent of the main power supply switch. The voltages VCCLCD3V3 and VCCLCD5V0 have to be powered on separately by field effect transistor Q12. The signals for powering on and off the VCCLCD voltages are generated by the carrier board's CPLD U8 derived form the implemented control register. The bit in the control register which is responsible for switching on and off the voltage sources are displayed in the following table:

Power Source	control register bit	Status	Description
VCCLCD3V3, VCCLCD5V0	bit [2]	- 0 -	signal /VCCLCD3V3ON remains high, signal VCCLCD5V0ON remains low – both power sources remains off
		- 1 -	signal /VCCLCD3V3ON switches to low, signal VCCLCD5V0ON switches to high – both power sources are switched on and LED D18 and D19 should be illuminated

Table 42: Display power switch description

Please refer to section 14.3.25 CPLD Functionality for more information about accessing control register of CPLD U8.

Checking the switched-on VCCLCD voltage sources are possible by inspecting the LEDs D18 and D19 assembled on the carrier board. D18 is illuminated if voltage VCCLCD3V3 is switched on, D19 is illuminated if voltage VCCLCD5V0 is switched on. If the power sources are switched off the appropriate LED remains off.

14.3.19 Touch Interface Connector X23 and X6

The phyCORE-MPC5121e/3-tiny Carrier Board provides two four-wire Touch interface connectors at X23 (MOLEX, 52207-0485) and X6 (Friction Lock Header JST B5B-EH-A). The signals are connected to the audio interface codec U21 and can there be analyzed. The following table describes the pin out of X23 and X6:

Location		Signal	Description
X23-1	X6-2	TOUCHYP	Four Wire Touch Interface – Top side Touch contact
X23-2	X6-1	TOUCHXM	Four Wire Touch Interface – Left side Touch contact
X23-3	X6-3	TOUCHYM	Four Wire Touch Interface – Bottom side Touch contact
X23-4	X6-4	TOUCHXP	Four Wire Touch Interface – Right side Touch contact
X23-5	-	GND	GND

Table 43: Pin Out of the Four wire Touch Connector Interface

14.3.20 LED Backlight Connector X24

The phyCORE-MPC5121e/3-tiny Carrier Board provides a LED Backlight interface connector at X24. The output voltage of the backlight voltage converter itself can be influenced by a PWM-Signal (LED_IADJ) and a shut down signal (LEDBACKLIGHTSHDN) generated by the CPLD U8 which are controllable by user. A description of the PWM interface register and the register to manipulate the shut down signal of the CPLD U8 will follow in the appropriate CPLD section. The following table describes the pin out of X24:

Location	Signal	Description
X24-1, X24-2	VCCLED	switched LED Backlight supply voltage
X24-3, X24-4	GND	GND
X24-5	/SHDN	Shutdown pin of LED Backlight Converter U52
X24-6	IADJ	IADJ pin of LED Backlight Converter U52

Table 44: Pin Out of LED Backlight Connector

The used LED backlight driver IC LT1618EMS (U52) is wired as a White LED Driver and its output voltage is determined by the following equitation:

$$R_1 = R_2 * (V_{out} / 1.263V - 1)$$

The resistor divider R1, R2 is shown in the following figure:

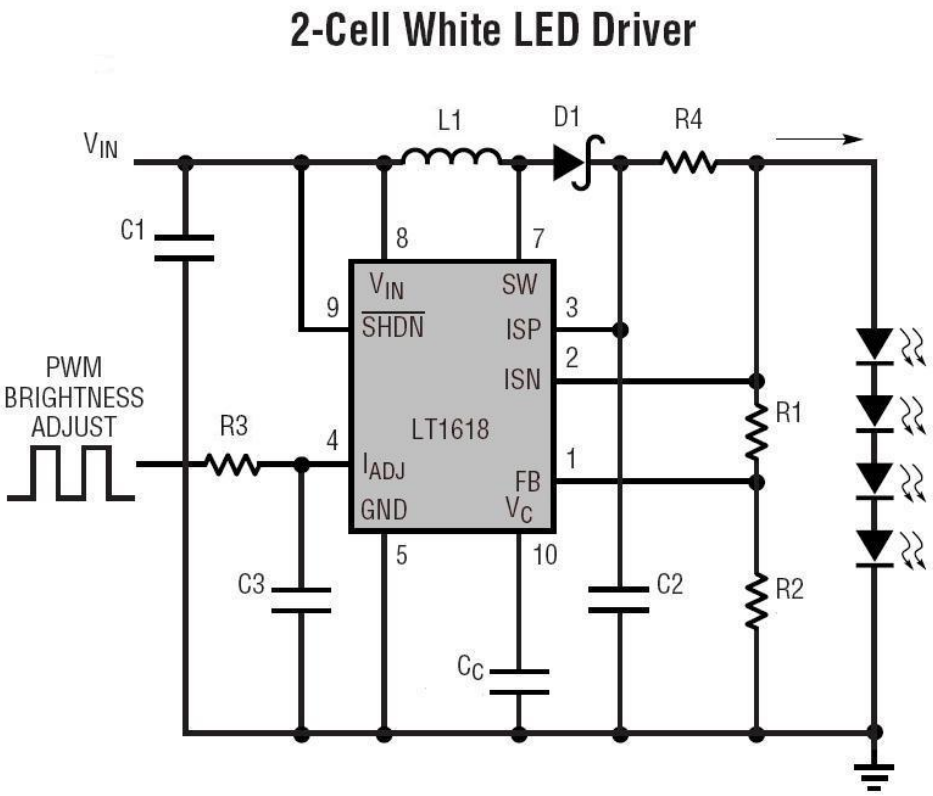


Figure 27: U52 – LED Backlight Converter – resistor divider R1, R2

As designed in the schematic of the carrier board the output voltage of the LED Backlight Driver is configured to 9.85V output voltage and the maximal current flow through resistor R4 is determined to 160mA by the equitation:

$$I_{max} = 50mV/R_{sense}$$

Adjusting the output current through resistor R4 is possible by changing the ratio between impulse and pause of the applied PWM signal at IADJ.

Please refer to the datasheet of the LTC1618 for more information about the LED Backlight Driver operation.

14.3.21 CCFL Backlight Connector X31

The phyCORE-MPC5121e/3-tiny Carrier Board provides a CCFL Backlight interface connector at X31. The PWM-signal output is also controllable by user with the CPLD's register interface. A description of the PWM register of CPLD U8 will follow in the appropriate CPLD section. The following table describes the pin out of X31:

Location	Signal	Description
X31-1	VCCLCD V5V0	5V power supply
X31-2	IADJ	PWM signal for backlight dimming
X31-3	GND	GND

Table 45: Four wire Touch Connector Configuration

14.3.22 Front Panel Connector X2

The phyCORE-MPC5121e/3-tiny Carrier Board provides a 9-position 0.1"/2.54mm double row male header at X2 to connect a front panel with keys for user interaction. The connector allows the usage of some important signals externally. The pin-out is shown in the following table:

Location	Signal	Description
X2-1	-	Pull Up Resistor to VCC3V3STBY for connecting the anode of an external user LED
X2-2	-	Pull Up Resistor to VCC3V3STBY for connecting the anode of an external user LED
X2-3	/USER_LED0	User LED0 Signal Output
X2-4	GND	Ground Connection
X2-5	/SYSRST_BTN	alternative input to the System Reset Button S5
X2-6	/PWR_BTN	alternative input to the Power Button S6
X2-7	/USER_LED1	User LED1 Signal Output
X2-8	GND	Ground Connection
X2-9	NC	not connected

Table 46: Front Panel Connector X2

14.3.23 Temperature Sensor on the Carrier Board phyCORE-MPC5121e/3-tiny U66

The phyCORE-MPC5121e/3-tiny Carrier Board is assembled with a temperature sensor LM77-3 with which the temperature of the environment could be sensed. The temperature sensor is connected to the first I2C-Interface I2C0 of the phyCORE-MPC5121e/3-tiny and it could be accessed per default with the read/write address 0x96/0x97.

The interrupt output /LM77_INT of the temperature sensor is connected to the CPLD U8 populated on the carrier board and is there connected by the implementation to /IRQ0 of the phyCORE-MPC5121e/3-tiny. The critical temperature output of the device is also connected to the CPLD U8 but is not used for any further implementation.

The read/write address of the sensor is configurable by solder jumper J1 and J2 whose configuration is represented in the following table:

I^2C Address	**J1** **A1**	**J2** **A0**
0x90 / 0x91	2 + 3	2 + 3
0x92 / 0x93	2 + 3	1 + 2
0x94 / 0x95	1 + 2	2 + 3
0x96 / 0x97	**1 + 2**	**1 + 2**

Table 47: Adress *settings* for temperature sensor

14.3.24 Misc. Configuration Switches on the Carrier Board

The following table describes additional switches provided for start up configuration of the phyCORE-MPC5121e/3-tiny or user interactions while the System is operating:

Switch	Setting	Description
S1	open	no additional action
	closed	User Button 0 generates an Interrupt at cpu signal /IRQ0 (X17B2) with cpld interrupt number 13
S2	open	no additional action
	closed	User Button 1 generates an Interrupt at cpu signal /IRQ0 (X17B2) with cpld interrupt number 14
S3	open	no additional action
	closed	no additional action (only for phyCORE-MPC5121e/3- not for –tiny)
S4	open	no additional action
	closed	S4 performs a power on or power off action if button is pressed for the appropriate time, 1000ms – power on, 5000ms power off
S5	open	no additional action
	closed	S5 performs a board reset for all components populated on the phyCORE-MPC5121e/3-tiny and the Carrier Board
S6	OFF	no additional action
	ON at Switch 1	Signal DIU_U_D connected to GND – Select signal for Vertical display mode pulled low
	ON at Switch 2	Signal DIU_L_R connected to GND – Select signal for Horizontal display mode pulled low
	ON at Switch 3	Signal DIU_V_Q connected to GND – Select signal for VGA/QVGA display mode pulled low.
	ON at Switch 4	Signal DIU_ENA connected to VCC3V3 – Display enabled
S7	open	MPC5121e/3 boots from default boot location, refer to

		section 5 System Start-Up Configuration
	closed during RESET	MPC5121e/3 boots the Backup Boot Loader at address 0x00000000 in NOR Flash, refer to section 5 System Start-Up Configuration
S8	open	no additional action
	closed during RESET	MPC5121e/3 boots the Backup Boot Loader at address 0x00000000 in NAND Flash, refer to section 5 System Start-Up Configuration

Table 48: Misc. Configuration Switches S1, S2, S3, S4, S5, S6, S7 and S8

14.3.25 CPLD Functionality

The CPLD U8 which is populated on the Carrier Board adds some functionalities to control peripheral functions. One of this functions is a state machine which turns the main supply voltage of the development board and an other functions on and off. This is to provide additional registers for accessing the peripheral elements like the 4 digit 7 segment display, the PWM output signal of the LED Backlight Driver and the generation/analyzation of interrupt signals to the phyCORE-MPC5121e/3-tiny. An additional control register allows the user to influence peripheral interfaces assembled on the carrier board.

Access to the CPLD U8 is possible by chip select signal /CS6 of the phyCORE-MPC5121e/3-tiny (PSC3_4 at X17D15) which is configured by uboot to 32-bit data width, 64k page size, 5 read and 5 write wait states, low active address latch enable and address latch enable width of one LPC clock cycle. The following figure shows the register implementation of the CPLD U8:

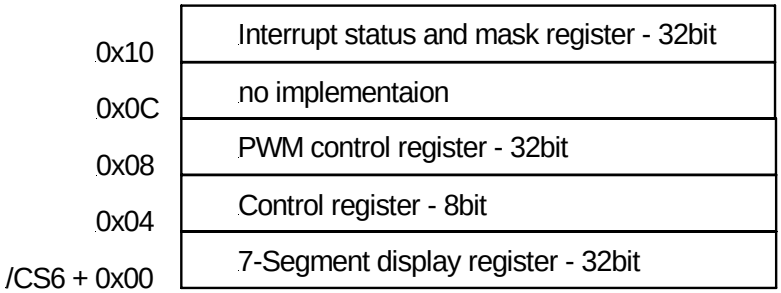


Figure 28: U8 –CPLD register implementation

In the following sections the CPLD functionalities will be described in more detail.

14.3.25.1 Power state machine of the Carrier Board

The CPLD U8 contains a state machine with which the carrier board can be powered on and off. The state machine counts therefore the rising edges of the cpld's internal generated clock when button S4 is pressed and decides in respect to the current power state to switch it on or off. For powering on the development board button S4 has to be pressed with a minimum of 1 second. Switching off the development board is possible by pressing button S4 with a minimum of 5 seconds. Powering off the carrier board is also possible by software. Writing a "1" in register bit [3] of the control register initiates a power down of the main supply voltages of the development board within the next 5 seconds. Please refer to the next chapters, where the registers bits of the cpld will be described in more detail.
The following figure shows the state machine of the CPLD U8 with its power on and off function:

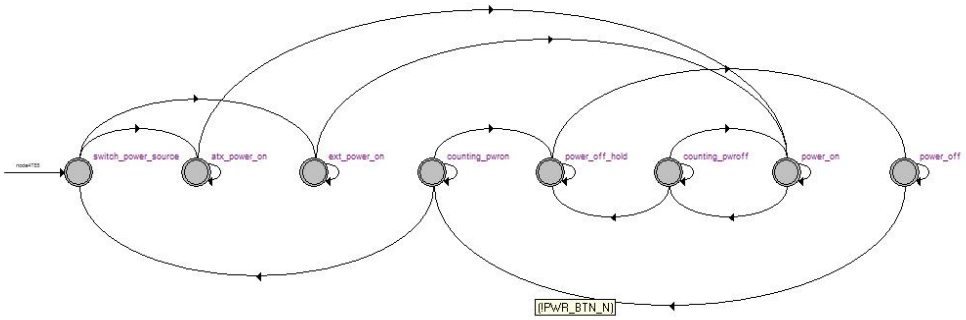


Figure 29: U8 –CPLD state machine implementation

14.3.25.2 The 4 digit 7 Segment Display

The 4 digit 7 segment display can be used for displaying software and hardware status information. The interface of the 4 digit 7 segment display consists of two register, which can be written or read to display status information. The register will be described as follows.

Register	Register Size	Address	Functionality
Data (r/w)	32 bit	CS-CPLD + 0x00	Data Register for displaying status information on the 4-digit 7-segment display, only 16 bit can be displayed once.
Control(r/w)	8-bit	CS-CPLD + 0x04	control register for switching status information between high word and low word, only bit [0] of control register used
Address(w)	5- bit	-	register which is always written in the address phase of a cpld access

Table 49: CPLD Register for displaying status information

14.3.25.3 The Control Register of the CPLD U8

The control register of the CPLD U8 occupies additional functions in respect to control peripheral elements. The register consist of totally 8 bits whereby 6 register bits were used to control peripheral functions. The functionality and the corresponding settings are described in the following table.

Register Bit	Settings	Description
Control [0]	- 0 -	Low word of status information for 7-segment display displayed
	- 1 -	High word of status information for 7-segment display displayed
Control [1]	- 0 -	DP output of 7-segment display active
	- 1 -	DP output of 7-segment display inactive
Control [2]	- 0 -	display supply Voltage powered off
	- 1 -	display supply Voltage powered on
Control [3]	- 0 -	no action
	- 1 -	shutting down all supply voltages within the next 3 seconds
Control [4]	- 0 -	LED Backlight switched on
	- 1 -	LED Backlight switched off
Control [5]	- 0 -	PATA Reset is inactive
	- 1 -	PATA reset active
Control [6]	- 0 -	User LED0 illuminated
	- 1 -	User LED0 remains off
Control [7]	- 0 -	User LED1 illuminated
	- 1 -	User LED1 remains off

Table 50: Control Register Bit description

14.3.25.4 The PWM Control Register

The PWM control register is a 32-bit register with which modifies the impulse pause ratio of the PWM signal generated by the CPLD U8 at signal pin LED_IADJ. The register is a 32-bit register of whose register bits 9..0 are only used to influence the impulse pause ratio.
To generate the PWM three main design implementations are done in the CPLD:

- 10 bit PWM load register
- 10 bit PWM counter
- PWM output stage (10bit-adder)

The PWM load register loads the content of the PWM control register bit 9..0 each time the PWM counter reaches the over flow state. The PWM counter itself counts from the zero state to its maximum value and then rolls over with generation of a reload signal to reload the PWM load register with the value of the PWM control register and itself by zero. The sum of both, the PWM load register and the PWM counter is always build by the PWM output stage. In this case the 16bit adder reaches its maximum value the adder generates a over flow bit that acts as PWM output signal. The following figure shows the general design implementation of the PWM module of the CPLD U8 where N is 9 and DATA is the input of the PWM load register generated by the PWM control register:

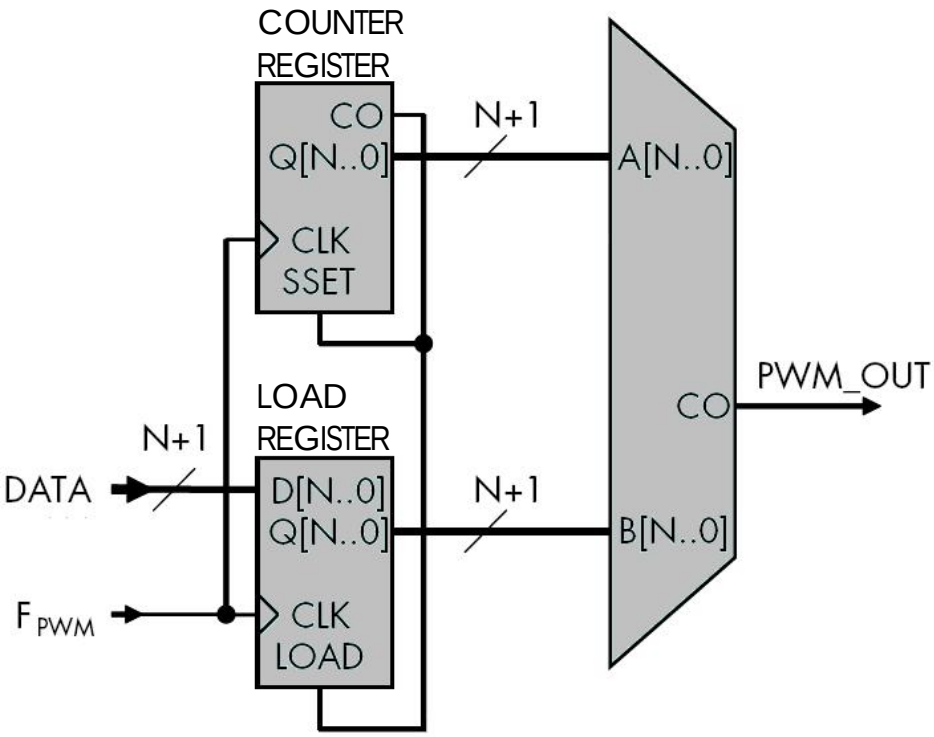


Figure 30: CPLD U8 - PWM implementation

The base frequency of the PWM is setup by hardware implementation of the CPLD and can only be modified by the user when changing the LPC bus clock frequency. The PWM output frequency is determined by the following equitation:

$$F_{PWM} = F_{LPC} / 2^N \text{ with } N = 10$$

For a frequency of the LPC bus with 33,333MHz, as setup in the default boot loader, the base frequency of the PWM is determined to:

$$33.333MHz / 2^{10} = 32,55KHz.$$

14.3.25.5 The Interrupt Status and Mask Register

The interrupt status and mask register provides information to the user about pending interrupts connected to the CPLD U8. The lower 16 bits of the interrupt status and mask register are reflecting the pending interrupts whereby the upper 16 bits of the register give the possibility to mask out some of the interrupts going to the phyCORE-MPC5121e/3's interrupt input /IRQ0. The interrupts connected to the CPLD U8 are all low active so that the contention of the interrupt status bits (bit 15..0) is always 0xffff if no interrupt is pending. The default setting of the upper 16bits of interrupt status and mask register is 0x0000 so that, without user configuration, all interrupts are reported to the CPU. The following table shows the interrupts connected to the CPLD U8 and their corresponding interrupt bit in the interrupt status and mask register:

Interrupt status and mask register bit	Status	Description
Bit [0]	- 0 -	PCI Interrupt SLOT 0 /INTA pending
	- 1 -	no interrupt pending
Bit [1]	- 0 -	PCI Interrupt SLOT 0 /INTB pending
	- 1 -	no interrupt pending
Bit [2]	- 0 -	PCI Interrupt SLOT 0 /INTC pending
	- 1 -	no interrupt pending
Bit [3]	- 0 -	PCI Interrupt SLOT 0 /INTD pending
	- 1 -	no interrupt pending
Bit [4]	- 0 -	PCI Interrupt SLOT 1 /INTA pending
	- 1 -	no interrupt pending
Bit [5]	- 0 -	PCI Interrupt SLOT 1 /INTB pending
	- 1 -	no interrupt pending
Bit [6]	- 0 -	PCI interrupt SLOT 1 /INTC

		pending
	- 1 -	no interrupt pending
Bit [7]	- 0 -	PCI interrupt SLOT 1 /INTD pending
	- 1 -	no interrupt pending
Bit [8]	- 0 -	Mini-PCI interrupt /INTA pending
	- 1 -	no interrupt pending
Bit [9]	- 0 -	Mini-PCI interrupt /INTB pending
	- 1 -	no interrupt pending
Bit [10]	- 0 -	interrupt temperature sensor LM77 pending
	- 1 -	no interrupt pending
Bit [11]	- 0 -	Ethernet PHY interrupt pending
	- 1 -	no interrupt pending
Bit [12]	- 0 -	user button S1 interrupt pending
	- 1 -	no interrupt pending
Bit [13]	- 0 -	user button S2 interrupt pending
	- 1 -	no interrupt pending
Bit [14]	- 0 -	AC97 interrupt pending
	- 1 -	no interrupt pending
Bit [15]	- 0 -	off chip RTC interrupt pending
	- 1 -	no interrupt pending
Bit [16]	- 0 -	interrupt unmasked – interrupt will be reported to CPU
	- 1 -	interrupt /INTA SLOT0 masked
Bit [17]	- 0 -	interrupt unmasked – interrupt will be reported to CPU
	- 1 -	interrupt /INTB SLOT0 masked
Bit [18]	- 0 -	interrupt unmasked – interrupt

		will be reported to CPU
	- 1 -	interrupt /INTC SLOT0 masked
Bit [19]	- 0 -	interrupt unmasked – interrupt will be reported to CPU
	- 1 -	interrupt /INTD SLOT0 masked
Bit [20]	- 0 -	interrupt unmasked – interrupt will be reported to CPU
	- 1 -	interrupt /INTA SLOT1 masked
Bit [21]	- 0 -	interrupt unmasked – interrupt will be reported to CPU
	- 1 -	interrupt /INTB SLOT1 masked
Bit [22]	- 0 -	interrupt unmasked – interrupt will be reported to CPU
	- 1 -	interrupt /INTC SLOT1 masked
Bit [23]	- 0 -	interrupt unmasked – interrupt will be reported to CPU
	- 1 -	interrupt /INTD SLOT1 masked
Bit [24]	- 0 -	interrupt unmasked – interrupt will be reported to CPU
	- 1 -	interrupt /INTA Mini-PCI SLOT masked
Bit [25]	- 0 -	interrupt unmasked – interrupt will be reported to CPU
	- 1 -	interrupt /INTB Mini-PCI SLOT masked
Bit [26]	- 0 -	interrupt unmasked – interrupt will be reported to CPU
	- 1 -	interrupt temperature sensor masked
Bit [27]	- 0 -	interrupt unmasked – interrupt will be reported to CPU

	- 1 -	Interrupt Ethernet PHY masked
Bit [28]	- 0 -	interrupt unmasked – interrupt will be reported to CPU
	- 1 -	Interrupt user button S1 masked
Bit [29]	- 0 -	interrupt unmasked – interrupt will be reported to CPU
	- 1 -	Interrupt user button S2 masked
Bit [30]	- 0 -	interrupt unmasked – interrupt will be reported to CPU
	- 1 -	AC97 interrupt masked
Bit [31]	- 0 -	interrupt unmasked – interrupt will be reported to CPU
	- 1 -	Off chip RTC interrupt masked

Table 51: CPLD- Interrupt status and mask register description

14.3.25.6 CPLD JTAG Connector X1

The 0.1"/2.54mm double row male header at X1 provide access to the JTAG signals of CPLD U8 populated on the development board of the phyCORE-MPC5121e/3-tiny:

Signal	Pin#	Pin#	Signal
PLD_JTAG_TCK	1	2	GND
PLD_JTAG_TDO	3	4	3.3V
PLD_JTAG_TMS	5	6	3.3V
n.c.	7	8	n.c.
PLD_JTAG_TDI	9	10	GND

Table 52: CPLD JTAG Connector X1 Pin Assignment

14.3.26 Pin Assignment Summary of the phyCORE, the Expansion Bus and the Patch Field

Most signals from the phyCORE-MPC5121e/3-tiny extend to the Expansion Bus connector X3 on the Carrier Board. These signals, in turn, are routed in a similar manner to the patch field on an optional expansion board that mounts to the Carrier Board at X30.

Please note that, depending on the design and size of the expansion board, only a portion of the entire patch field is utilized under certain circumstances. When this is the case, certain signals described in the following section will not be available on the expansion board. However, the pin assignment scheme remains consistent.

A two dimensional numbering matrix similar to the one used for the pin layout of the phyCORE-Connector is provided to identify signals on the Expansion Bus connector (X30 on the Carrier Board) as well as the patch field.

However, the numbering scheme for Expansion Bus connector and patch field matrices differs from that of the phyCORE-Connector, as shown in the following two figures:

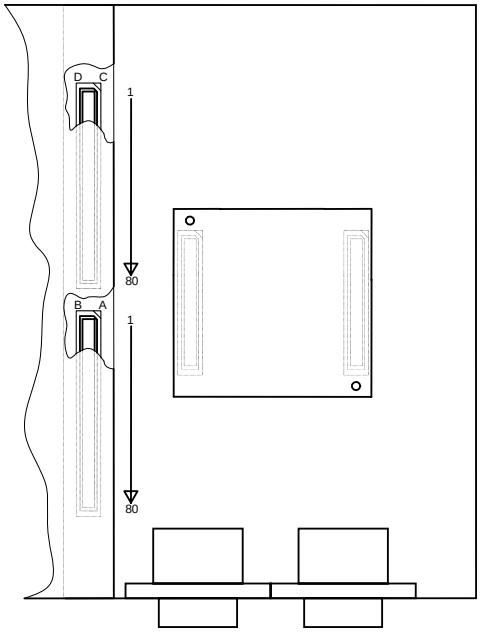


Figure 31: Pin Assignment Scheme of the Expansion Bus

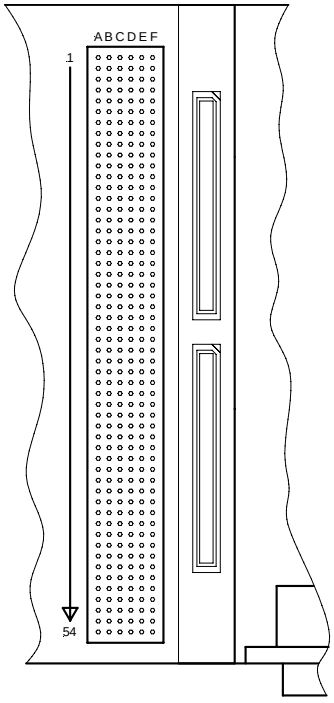


Figure 32: Pin Assignment Scheme of the Patch Field

The pin assignment on the phyCORE-MPC5121e/3-tiny, in conjunction with the Expansion Bus (X30) on the Carrier Board and the patch field on an expansion board, is as follows:

Signal	phyCORE Module	Expansion Bus	Patch Field
EMB_AD0	10B	10B	X10-4
EMB_AD1	11B	11B	X11-4
EMB_AD2	11A	11A	X17-2
EMB_AD3	12B	12B	X12-4
EMB_AD4	13A	13A	X14-4
EMB_AD5	13B	13B	X13-4
EMB_AD6	14A	14A	X15-4
EMB_AD7	15A	15A	X16-4
EMB_AD8	15B	15B	X10-5
EMB_AD9	16A	16A	X17-4
EMB_AD10	16B	16B	X11-5
EMB_AD11	17B	17B	X12-5
EMB_AD12	18A	18A	X14-5
EMB_AD13	18B	18B	X13-5
EMB_AD14	19A	19A	X15-5
EMB_AD15	20A	20A	X16-5
EMB_AD16	20B	20B	X10-6
EMB_AD17	21A	21A	X17-5
EMB_AD18	21B	21B	X11-6
EMB_AD19	22B	22B	X12-6
EMB_AD20	23A	23A	X14-6
EMB_AD21	23B	23B	X13-6
EMB_AD22	24A	24A	X15-6
EMB_AD23	25A	25A	X16-6
EMB_AD24	25B	25B	X10-7
EMB_AD25	26A	26A	X17-6
EMB_AD26	26B	26B	X11-7
EMB_AD27	27B	27B	X12-7
EMB_AD28	28A	28A	X14-7
EMB_AD29	28B	28B	X13-7
EMB_AD30	29A	29A	X15-7
EMB_AD31	30A	30A	X16-7

Table 53: Pin Assignment Data/Address Bus for the phyCORE-MPC5121e/3-tiny / Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
EMB_AX2	8B	8B	X13-2
EMB_AX1	9A	9A	X15-2
EMB_AX0	10A	10A	X16-2
/LP_CS1	5°	5A	X16-1
/LP_CS2	5B	5B	X10-2
LPC_RNW	6B	6B	X11-2
/LPC_OE	6A	6A	X17-1
/LPC_ACK	8A	8A	X14-2
LPC_AX3	7B	7B	X12-2
LPC_CLK	3B	3B	X13-1

Table 54: Pin Assignment Dedicated LocalPlus Control Signals phyCORE-MPC5121e/3-tiny / Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
/PCI_RST_OUT	50°	-	-
PCI_CLOCK	50B	-	-
/PCI_GNT0	51°	-	-
/PCI_REQ0	52B	-	-
/PCI_CBE3	58A	-	-
PCI_IDSEL	58B	-	-
/PCI_CBE2	64°	-	-
/PCI_IRDY	65A	-	-
/PCI_FRAME	65B	-	-
/PCI_DEVSEL	66A	-	-
/PCI_TRDY	66B	-	-
/PCI_STOP	67B	-	-
/PCI_PERR	68A	-	-
PCI_PAR	68B	-	-
/PCI_SERR	69A	-	-
/PCI_CBE1	70°	-	-
/PCI_CBE0	75B	-	-
/PCI_GNT1	47B	-	-
/PCI_GNT2	48°	-	-
/PCI_REQ1	48B	-	-
/PCI_REQ2	49A	-	-
/PCI_INT	46A	-	-
PCI_AD0	80B	-	-
PCI_AD1	80°	-	-
PCI_AD2	79°	-	-
PCI_AD3	78B	-	-
PCI_AD4	78A	-	-
PCI_AD5	77B	-	-
PCI_AD6	76B	-	-
PCI_AD7	76A	-	-
PCI_AD8	75°	-	-
PCI_AD9	74°	-	-
PCI_AD10	73B	-	-
PCI_AD11	73°	-	-

PCI_AD12	72B	-	-
PCI_AD13	71B	-	-
PCI_AD14	71°	-	-
PCI_AD15	70B	-	-
PCI_AD16	73B	-	-
PCI_AD17	73A	-	-
PCI_AD18	72B	-	-
PCI_AD19	71B	-	-
PCI_AD20	71A	-	-
PCI_AD21	70B	-	-
PCI_AD22	70A	-	-
PCI_AD23	59°	-	-
PCI_AD24	57B	-	-
PCI_AD25	56B	-	-
PCI_AD26	56°	-	-
PCI_AD27	55B	-	-
PCI_AD28	55°	-	-
PCI_AD29	54A	-	-
PCI_AD30	53B	-	-
PCI_AD31	53A	-	-

Table 55: Pin Assignment PCI dedicated signals
phyCORE-MPC5121e/3-tiny / Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
/PATA_CE1	35B	37B	X12-10
PATA_IOCHRDY	33A	38A	X14-10
/PATA_CE2	36B	38B	X13-10
PATA_INTRQ	34A	39A	X15-10
PATA_DRQ	35A	40A	X16-10
PATA_ISOLATE	37B	40B	X10-11
/PATA_DACK	36A	41A	X17-10
/PATA_IOR	38B	41B	X11-11
/PATA_IOW	40B	42B	X12-11

Table 56: Pin Assignment Dedicated PATA /IDE Interface Signals phyCORE-MPC5121e/3-tiny / Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
SATA_RXP	40A	-	-
SATA_ANAVIZ	43B	-	-
SATA_RXN	41A	-	-
SATA_TXP	45B	-	-
SATA_TXN	46B	-	-

Table 57: Pin Assignment Dedicated SATA Interface Signals phyCORE-MPC5121e/3-tiny / Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
TXD6-232	23C	-	-
RXD6-232	21C	-	-
PSC6_2_TXD	20C	20C	X8-5
PSC6_3_RXD	19C	19C	X7-5
J1850_TX	24C	24C	X7-6
J1850_RX	25C	25C	X8-6
RXD3-232	22D	-	-
TXD3-232	23D	-	-
PSC3_2_TXD	17D	17D	X4-5
PSC3_3_RXD	16D	16D	X3-5
CAN1_TX	21D	-	-
CAN1_RX	20D	-	-
CAN2_TX	18C	-	-
CAN2_RX	18D	-	-
I2C0_SCL	31C	31C	X2-9
I2C0_SDA	32D	32D	X4-9
I2C1_SCL	26C	26C	X2-7
I2C1_SDA	28C	28C	X5-7
I2C2_SCL	27D	27D	X4-7
I2C2_SDA	28D	28D	X6-7
ETH_RX-	35C	-	-
ETH_RX+	35D	-	-
ETH_TX-	36C	-	-
ETH_TX+	36D	-	-
ETH_LED0	33C	-	-
ETH_LED1	34C	-	-
/PHY_INTR	38C	-	-
FEC_CRS	49C	49A	X15-12
FEC_COL	50C	50A	X16-12
FEC_TXD_3	50D	50B	X10-14
FEC_TXD_1	51C	51A	X17-12
FEC_TXD_2	51D	51B	X11-14
FEC_TXD_0	52D	52B	X12-14
FEC_TX_EN	53C	53A	X14-14
FEC_TX_CLK	53D	53B	X13-14

FEC_TX_ER	54C	54A	X15-14
FEC_RXD_3	55C	55A	X16-14
FEC_RX_DV	55D	55B	X10-15
FEC_RXD_2	56C	56A	X17-14
FEC_RXD_1	56D	56B	X11-15
FEC_RXD_0	57D	57B	X12-15
FEC_RX_ER	58C	58A	X14-15
FEC_RX_CLK	58D	58B	X5-9
FEC__MDC	59C	60A	X16-15
FEC_MDIO	60D	60B	X7-9
USB_UID	46D	-	-
USB_TPA	43D	-	-
USB_DP	43C	-	-
USB_DM	44C	-	-
USB_DRVVBUS	45C	-	-
USB_VBUS	45D	-	-
USB_PWRFAULT	41C	-	-

Table 58: Pin Assignment Interfaces for the phyCORE-MPC5121e/3-tiny / Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
JTAG_TCK	38D	38D	X6-9
/JTAG_TRST	39C	39C	X7-10
JTAG_TDI	40D	40D	X9-10
JTAG_TDO	41D	41D	X3-11
JTAG_TMS	42D	42D	X4-11
/JTAG_CKSTOP_O	40C	40C	X8-10

Table 59: Pin Assignment COP Interface Signals for the phyCORE-MPC5121e/3-tiny /Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
/IRQ0	2B	2B	X12-1
/IRQ1	3A	3A	X14-1
WDI	8D	8D	X7-2
/WDO	8C	8C	X8-1
/PORESET	12D	12D	X4-4
/MR_IN	10D	10D	X2-4
/HReset	11C	11C	X9-2
/SReset	10C	10C	X9-1
/FLASH_RESET	11D	11D	X3-4
/HIB_MODE	7D	7D	X7-1
/FL_WP	9C	9C	X8-2
CLK_RTC	1B	1B	X11-1
PSC3_0	25D	25D	X9-6
PSC3_1	26D	26D	X3-7
PSC3_4	15D	15D	X9-4
PSC4_0	15C	-	-
PSC4_1	14C	-	-
PSC4_2	13D	-	-
PSC4_3	16C	-	-
PSC4_4	13C	-	-
PSC5_0	29C	29C	X7-7
PSC5_1	30D	30D	X9-7
PSC5_2	30C	30C	X8-7
PSC5_3	31D	31D	X3-9
PSC5_4	33D	33D	X6-9
PSC6_0	64C	46C	X2-12
PSC6_1	63D	47D	X4-12
PSC6_4	65C	48C	X5-12
PSC7_0	65D	48D	X6-12
PSC7_1	66C	49C	X7-12
PSC7_2	66D	50D	X9-12
PSC7_3	68C	50C	X8-12
PSC7_4	67D	51D	X3-14
PSC8_0	69C	51C	X2-14
PSC8_1	68D	52D	X4-14

PSC8_2	70C	53C	X5-14
PSC8_3	70D	53D	X6-14
PSC8_4	71C	54C	X7-14
PSC9_0	73C	55C	X8-14
PSC9_1	71D	55D	X9-14
PSC9_2	74C	56C	X2-15
PSC9_3	72D	56D	X3-15
PSC9_4	73D	57D	X4-15
PSC10_0	75C	58C	X5-15
PSC10_1	75D	58D	X6-15
PSC10_2	76C	59C	X7-15
PSC10_3	76D	60C	X8-15
PSC10_4	78C	60D	X9-15
PSC11_0	79C	61C	X2-16
PSC11_1	77D	61D	X3-16
PSC11_2	78D	62D	X4-16
PSC11_3	80C	63C	X5-16
PSC11_4	80D	63D	X6-16
GPIO28	30B	30B	X10-9
GPIO29	31A	31A	X17-7
GPIO30	31B	31B	X11-9
GPIO31	32B	32B	X12-9

Table 60: Pin Assignment Misc. Interface Signals phyCORE-MPC5121e/3-tiny / Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
RDY_BOOT	-	64C	X7-16
PHY0_RXN	-	-	-
PHY0_RXP	-	-	-
PHY0_TXN	-	-	-
PHY0_TXP	-	-	-
NETX_MMIO08	-	67D	X4-17
NETX_MMIO09	-	68D	X6-17
NETX_USB_DNEG	-	-	

NETX_USB_DPOS	-	-	-
PHY1_RXN	-	-	-
PHY1_RXP	-	-	-
PHY1_TXN	-	-	-
PHY1_TXP	-	-	-
NETX_MMIO10	-	72D	X4-19
XM1_TX	-	73C	X5-19
XM0_RX	-	73D	X6-19
XM1_ECLK	-	74C	X7-19
XM1_RX	-	75C	X8-19
XM0_TX	-	75D	X9-19
XM1_IO0	-	76C	X2-20
XM0_ECLK	-	76D	X3-20
XM0_IO0	-	77D	X4-20
NETX_TCLK	-	78C	X5-20
NETX_TMS	-	78D	X6-20
NETX_TDI	-	79C	X7-20
NETX_TDO	-	80C	X8-20
/NETX_TRST	-	80D	X9-20
NETX_MMIO11	-	81C	X2-21
NETX_MMIO12	-	-	-
NETX_MMIO13	-	-	-
NETX_MMIO14	-	-	-
NETX_MMIO15	-	-	-
NETX_MMIO16	-	84C	X7-21
NETX_MMIO17	-	85C	X8-21
NETX_MMIO18	-	85D	X9-21
NETX_MMIO19	-	86C	X2-22
NETX_MMIO20	-	86D	X3-22
NETX_MMIO21	-	87D	X4-22
NETX_MMIO22	-	88C	X5-22
NETX_MMIO23	-	88D	X6-22
NETX_MMIO24	-	89C	X7-22
NETX_MMIO25	-	90C	X8-22
NETX_MMIO26	-	90D	X9-22
NETX_MMIO27	-	91C	X2-24

NETX_MMIO28	-	91D	X3-24
NETX_MMIO29	-	92D	X4-24
NETX_MMIO30	-	93C	X5-24
NETX_MMIO31	-	93D	X6-24
NETX_U0_CTS	-	-	-
NETX_U0_RXD	-	-	-
NETX_U0_RTS	-	-	-
NETX_MMIO36	-	96C	X2-25
NETX_U0_TXD	-	-	-
NETX_MMIO37	-	97D	X4-25
NETX_MMIO38	-	98C	X5-25
NETX_MMIO39	-	98D	X6-25

Table 61: Pin Assignment netX50 Signals for only phyCORE-MPC5121e/3 (not for phyCORE-MPC5121e/3-tiny) / Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
DDC_CLOCK	-	72B	X12-19
DDC_DATA	-	73B	X13-19
MAXII_B2_C10	-	75A	X16-19
MAXII_B2_C9	-	75B	X10-20
MAXII_B2_B10	-	76A	X17-19
MAXII_B2_A10	-	76B	X11-20
MAXII_B2_C8	-	77B	X12-20
MAXII_B2_A9	-	78A	X14-20
MAXII_B2_B9	-	78B	X13-20
MAXII_B2_A8	-	79A	X15-20
MAXII_B2_C7	-	80A	X16-20
MAXII_B2_A7	-	80B	X10-21
MAXII_B2_B8	-	81A	X17-20
MAXII_B2_B5	-	81B	X11-21
MAXII_B2_B7	-	82B	X12-21
MAXII_B2_C6	-	83A	X14-21
MAXII_B2_C5	-	83B	X13-21
MAXII_B2_M14	-	84A	X15-21
MAXII_B2_L16	-	85A	X61-21
MAXII_B2_A6	-	85B	X10-22

MAXII_B2_L13	-	86A	X17-21
MAXII_B2_D5	-	86B	X11-22
MAXII_B2_B6	-	87B	X12-22
MAXII_B2_K15	-	88A	X14-22
MAXII_B2_B4	-	88B	X13-22
MAXII_B2_L14	-	89A	X15-22
MAXII_B2_K16	-	90A	X16-22
MAXII_B2_A5	-	90B	X10-24
MAXII_B2_K14	-	91A	X17-22
MAXII_B2_C4	-	91B	X11-24
MAXII_B2_A4	-	92B	X12-24
MAXII_B2_J15	-	93A	X14-24
MAXII_B2_D4	-	93B	X13-24
MAXII_B2_J14	-	94A	X15-24
MAXII_B2_J16	-	95A	X16-24
MAXII_B2_A2	-	95B	X10-25
MAXII_B2_H14	-	96A	X17-24
MAXII_B2_B3	-	96B	X11-25
MAXII_B2_B1	-	97B	X12-25
MAXII_B2_H16	-	98A	X14-25
MAXII_B2_J12	-	98B	X13-25
MAXII_B2_G14	-	99A	X15-25
MAXII_B2_H15	-	100A	X16-25
MAXII_B2_H12	-	100B	X17-25

Table 62: Pin Assignment MAXII Interface Signals for the phyCORE-MPC5121e/3-tiny Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
3V3	1C, 2C, 4C, 5C, 1D, 2D, 4D, 5D	1C, 2C, 4C, 5C, 1D, 2D, 4D, 5D	X2-1, X2-2, X3-1, X3-2, X4-1, X4-2, X5-1, X5-2
VCC_SRAM	6D	6D	X6-2
VBAT	6C	6C	X6-1
GND	2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 45A, 47A, 52A, 57A, 62A, 67A, 72A, 77A 4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 41B, 44B, 47B 49B,, 51B, 54B, 59B, 64B, 49B, 74B, 79B 3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 72C, 77C 3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D, 74D, 79D	2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A,42A, 45A, 47A, 52A, 57A, 62A, 67A, 72A, 77A, 82A, 87A, 92A, 97A, 4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 47B, 49B, 54B, 59B, 64B, 69B, 74B, 79B, 84B, 89B, 94B, 99B, 3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 72C, 77C, 82C, 87C, 92C, 97C, 3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D, 74D, 79D, 84D, 89D, 94D, 99D	X2-3, X2-8, X2-13, X2-18, X2-23 X3-3, X3-8, X3-13, X3-18, X3-23, X16-11 X4-3, X4-8, X4-13, X4-18, X4-23 X5-3, X5-8, X-13, X5-18, X5-23 X6-3, X6-8, X6-13, X6-18, X6-23 X7-3, X7-8, X7-13, X7-18, X7-23 X8-3, X8-8, X8-13, X8-18, X8-23 X9-3, X9-8, X9-13, X9-18, X9-23, X10-3, X10-8, X10-13, X10-18, X10-23 X11-3, X11-8, X11-13, X11-18, X11-23 X12-3, X12-8, X12-12, X12-13, X12-18, X12-23 X13-3, X13-8, X-13, X13-18, X13-23 X14-3, X14-8, X14-13, X14-18, X14-23 X15-3, X15-8, X15-13,

			X15-18, X15-23 X16-3, X16-8, X16-13, X16-18, X16-23 X17-3, X17-8, X17-13, X17-18, X17-23,
NC	4A, 38A, 39A, 44A, 45A, 33B, 41B, 42B, 46C, 48C, 60C, 61C, 63C, 37D, 47D, 48D, 61D, 62D	4A, 33A, 34A, 35A, 36A, 43A, 44A, 46A, 48A, 59A, 61A, 63A, 64A, 65A, 66A, 68A, 69A, 70A, 71A, 73A, 74A, 33B, 35B, 36B, 43B, 45B, 46B, 61B, 62B, 63B, 65B, 66B, 67B, 68B, 70B, 13C, 14C, 15C, 16C, 18C, 21C, 23C, 33C, 34C, 35C, 36C, 43C, 44C, 45C, 65C, 66C, 68C, 69C, 70C, 71C, 83C, 94C, 95C, 99C, 100C, 13D, 18D, 20D, 21D, 22D, 23D, 25D, 26D, 35D, 36D, 37D, 43D, 45D, 46D, 65D, 66D, 70D, 71D, 81D, 82D, 83D, 95D, 96D, 100D	X15-1, X14-9, X15-9, X16-9, X17-9, X14-11, X15-11, X17-11, X14-12, X15-15, X15-16, X16-16, X17-16, X16-17, X17-17, X14-19, X15-19, X13-9, X10-10, X11-10, X13-11, X10-12, X11-12, X11-16, X12-16, X13-16, X10-17, X11-17, X12-17, X13-17, X10-19, X5-4, X7-4, X8-4, X2-5, X5-5, X2-6, X5-6, X5-9, X7-9, X8-9, X2-10, X5-11, X7-11, X8-11, X8-16, X2-17, X5-17, X7-17, X8-17, X2-19, X5-21, X7-24, X8-24, X7-25, X8-25, X6-4, X6-5, X9-5, X3-6, X4-6, X6-6, X9-6, X3-7,

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Table 63: Pin Assignment Power Supply and not connected signals for the phyCORE-MPC5121e/3-tiny / Carrier Board / Expansion Board

14.3.27 Gold CAP Connector C134

The mounting space C134 (*see PCB stencil*) is provided for connection of a gold cap that buffers the RTC and the SRAM on the phyCORE-MPC5121e/3-tiny. In the event of a VCC operating voltage failure the RTC and the SRAM are automatically supplied with power from the connected gold cap. The optional gold cap required for the RTC and SRAM is available through PHYTEC (order code CG-002).

A Appendix

14.4 Release Notes

The following section contains information about deviations to the description in this manual. Revisions to previous manuals are also listed.

Date	Version numbers	Changes in this manual
25-Jun-2009	Manual L-737e_0 PCM-046 PCB# 1326.0 PCM-962-tiny PCB# 1323.0	First draft, Preliminary documentation. phyCORE-MPC5121e/3-tiny in "Prototype" state

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Document: **phyCORE-MPC5121e/3 tiny**
Document number: **L-737e_0 October 2009**

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