Errata Sheet V1.0 for PCM-014-23111

This Errata Sheet refers to the Hardware Manual of the phyCORE-AT91M55800A

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Problem description:

Due to a design failure of the phyCORE-AT91M55800A with the PCB revision 1192.1 the signals /UB (Pin 33B on X1) and A0/LB (Pin 8B on X1) are switched on the connector X1 if SRAM's with fast access times populate the phyCORE module. The signal A0/LB on pin 37 of the Ethernet controller CS8900A and pin 3 on solder jumper J26 are switched with the /UB signal as well.

Work-around:

Please note the modified pin assignment for X1B33 and X1B8.
In the new PCB revision 1192.2 the signals listed above will be available on their assigned pins as shown in the current version of the Hardware Manual for the phyCORE-AT91M55800A.