phyCORE-MPC565

Hardware Manual

Edition April 2004

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6th Edition: April 2004

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Preface

This phyCORE-MPC565 Hardware Manual describes the board's design and functions. Precise specifications for the Motorola MPC565 microcontroller series can be found in the enclosed MPC565 microcontroller Data-Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal. The MSB and LSB of the data and address busses shown in the circuit diagram are based on the conventions of Motorola. Accordingly, D31 and A31 represent the LSB, while D0 and A0 represent the MSB. These conventions are also valid for the parallel I/O signals.

Declaration regarding Electro Magnetic Conformity of the PHYTEC phyCORE-MPC565

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Note:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header rows or connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-MPC565 is one of a series of PHYTEC Single Board Computers that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports common 8-, 16- and selected 32-bit controllers on two types of Single Boards Computers:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform
(2) as insert-ready, fully functional micro-, mini- and phyCORE OEM modules, which can be embedded directly into the user's peripheral hardware, design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market.

1 Introduction

The phyCORE-MPC565 belongs to PHYTEC's phyCORE Single Board Computer module family. The phyCORE SBCs represent the continuous development of PHYTEC Single Board Computer technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a sub-miniature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments the phyCORE board design features an increased pin package. The increased pin package allows dedication of approximately 20 % of all pin header connectors on the phyCORE boards to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD and laser-drilled Microvias components are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCORE-MPC565 is a subminiature (84 x 57 mm) insert-ready Single Board Computer populated with Motorola's PowerPC MPC565 microcontroller. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to high-density (0.635 mm) Molex pin header connectors aligning two sides of the board, allowing it to be plugged like a "big chip" into a target application.

Precise specifications for the controller populating the board can be found in the applicable controller User's Manual or Data Sheet. The descriptions in this manual are based on the MPC565 controller. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCORE-MPC565.

The phyCORE-MPC565 offers the following features:

- Single Board Computer in subminiature form factor (84 x 57 mm) according to phyCORE specifications
- all applicable controller and other logic signals extend to two high-density 200-pin Molex connectors
- processor: Motorola embedded PowerPC MPC565 (40/56 MHz clock)
- Internal Features of the MPC565:
  - 32-bit PowerPC core, 40 / 56 MHz CPU speed
  - 64-bit Floating Point Unit
  - 36 kByte SRAM; capable of battery buffering
  - 1 MByte Flash (two independent 512 kByte blocks)
  - four UARTs
  - two SPI interfaces
  - one J1850 interface
  - three CAN 2.0B interfaces
  - three TPU with 16 channels each
  - six 16-bit timer systems (MOIS14)
  - twelve 16-bit PWM systems (MIOS14)
  - dual 10-bit ADC (5µs) with 40 (65) channels (ext. MUX)
  - multi-purpose I/O signals
  - JTAG/BDM/Nexus test/debug port

- Memory Configuration[1]:
  - SRAM: 1 MByte to 16 MByte flow-through synchronous burst-RAM, 32-bit access, 0 wait states, 2-1-1-1 burst mode
  - Flash-ROM: 2/4 MB synchronous burst mode Flash-EEPROM, 32-bit access 2 MByte to 8 MByte asynchronous standard Flash-EEPROM, 32-bit access
  - I^2C Memory: 4 kByte EEPROM (up to 32 kByte, alternatively I^2C FRAM, I^2C SRAM)

- Other Board-Level Features:
- UART port: two RS-232 transceivers for channel A and B (RxD/TxD); also configurable as TTL
- CAN port: two CAN transceivers 82C251 for channels A and B; also configurable as TTL
- Ethernet port: 10 Mbit/s CS8900A controller (I/O mode)
- System-EPLD: Lattice device ispMACH LC4064, in-system programmable, 10 free I/O signals, e.g. for additional /CS generation
- I^2C Real-Time Clock with calendar and alarm function
- power-down/wake-up support via RTC, decrementer, or external signal
- JTAG/BDM/Nexus test/debug port
- industrial temperature range (-40…+85°C)

1: Please contact PHYTEC for more information about additional modul configurations.

1.1 Block Diagram

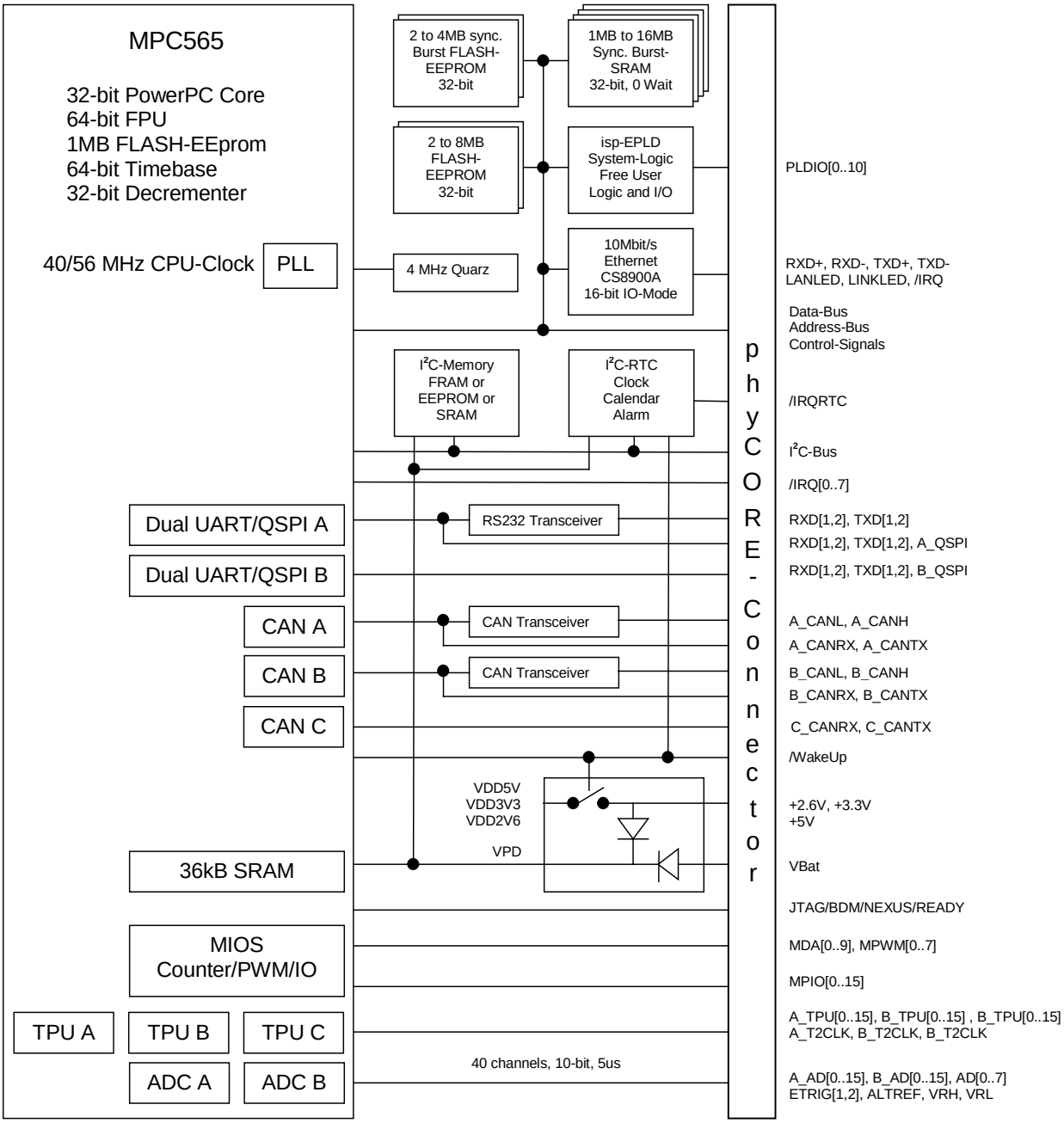


Figure 1: Block Diagram phyCORE-MPC565

1.2 View of the phyCORE-MPC565

Figure 2: View of the phyCORE-MPC565 Revision 1198.2

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 3* indicates, all controller signals extend to surface mount technology (SMT) connectors (0.635 mm) lining two sides of the module (referred to as phyCORE-connector; *refer to section 12*). This allows the phyCORE-MPC565 to be plugged into any target application like a "big chip".

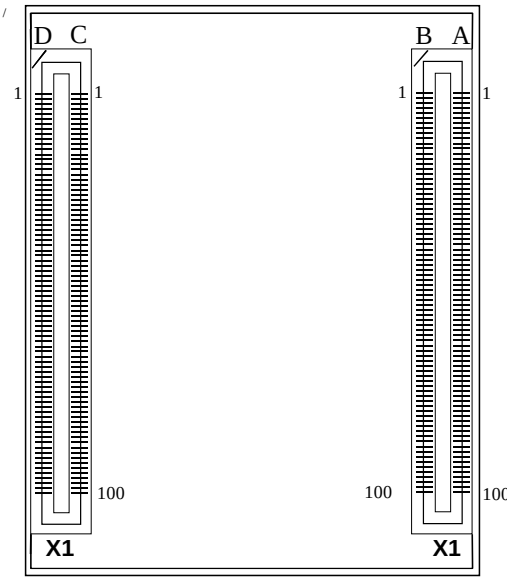


Figure 3: Pinout of the phyCORE-MPC565 (Bottom View)

Many of the controller port pins accessible at the edges of the board have been assigned alternate functions that can be activated via software.

Table 1 provides an overview of the pinout of the phyCORE-connector , as well as descriptions of possible alternative functions. *Please refer to the Motorola MPC565 User Manual/Data Sheet for details on the functions and features of controller signals and port pins.*

Pin Number	Signal	I/O	Comments
Pin row X1A			
1A	EXTCLK	I	Optional external clock input of the MPC565
2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A, 82A, 87A, 92A, 97A	GND	-	Ground 0 V
3A	/IRQ3	I	/IRQ3 interrupt of the MPC565 Alternative: /KR, /RETRY, SGPIOC3 (I/O)
4A	/IRQ0	I	/IRQ0 (/NMI) interrupt of the MPC565 Alternative: SGPIOC0 (I/O)
5A	/CS2	O	/CS signal of the MPC565
6A	/CS1	O	/CS signal of the MPC565
8A	/WE3	O	Write enable signal for the data lines D[24..31]. Note that D31 represents the LSB Alternative: AT3 (O) The alternative function may only be used if no on-board memory is populated.
9A, 10A, 11A, 13A, 14A, 15A, 16A, 18A, 24A, 25A, 26A, 28A	A30, A29, A27, A24, A22, A21, A19, A16, A14, A13, A11, A8	I/O	Address lines Alternative: SGPIOA30, SGPIOA29, SGPIOA27, SGPIOA24, SGPIOA22, SGPIOA21, SGPIOA19, SGPIOA16, SGPIOA14, SGPIOA13, SGPIOA11, SGPIOA8 (I/O) For the use of the alternative function, note that the address lines are partially used for memory addressing.
19A, 20A, 21A, 23A, 29A, 30A, 31A, 33A, 38A, 39A, 40A, 41A, 43A, 44A, 45A, 46A	D30, D29, D27, D24, D22, D21, D19, D16, D14, D12, D11, D9, D6, D4, D3, D1	I/O	Data lines Alternative: SGPIOD30, SGPIOD29, SGPIOD27, SGPIOD24, SGPIOD22, SGPIOD21, SGPIOD19, SGPIOD16, SGPIOD14, SGPIOD12, SGPIOD11, SGPIOD9, SGPIOD6, SGPIOD4, SGPIOD3, SGPIOD1 (I/O) For use of the alternative function, note that the data lines are used to connect the on-board memory and peripheral devices.

Pin Number	Signal	I/O	Comments
34A	/TA	I/O	Transfer acknowledge signal of the MPC565
35A	/TEA	I/O	Transfer error acknowledge signal of the MPC565
36A	/BB	I/O	Bus busy signal of the MPC565 Alternative: VF2 (O), IWP3 (O)
50A	/FLIRQ	O	Interrupt output of the Flash devices
51A	TSIZ0	I/O	Transfer size signal of the MPC565
48A 49A 65A 66A 68A	PLDIO1, PLDIO3, PLDIO5, PLDIO7, PLDIO9	I/O	Free I/O pin of the PLD
53A	/TS	I/O	Transfer start signal of the MPC565
54A	RDNWR	I/O	Read/write (RD//WR) signal of the MPC565
55A	/BDIP	I/O	'Burst data in progress' signal of the MPC565
56A	/BURST	I/O	Burst indicator signal of the MPC565
58A	/BI//STS	I/O	Burst inhibit signal of the MPC565 Alternative: special transfer start (O)
59A	CANSTB	I	Connected to J5 for standby control of the CAN transceivers
60A	/PWRON	O	Power-on signal of the power system
61A	/WAKEUP	I	Wake-up input
63A	PLDTDO	O	JTAG TDO line of the PLD
64A	PLDTDI	I	JTAG TDI line of the PLD
69A	C_T2CLK	I/O	Clock signal of the TPU C of the MPC565
70A 71A 73A 74A 75A 76A 78A 79A	C_TPU15, C_TPU13, C_TPU11, C_TPU9, C_TPU7, C_TPU5, C_TPU3, C_TPU1	I/O	TPU I/O signals connected to the TPU C of the MPC565
80A 81A 83A 84A 85A 86A 88A 89A	B_TPU15, B_TPU13, B_TPU11, B_TPU9, B_TPU7, B_TPU5, B_TPU3, B_TPU1	I/O	TPU I/O signals connected to the TPU B of the MPC565
90A	B_T2CLK	I/O	Clock signal of the TPU B of the MPC565
91A 93A 94A 95A 96A 98A 99A 100A	A_TPU15, A_TPU13, A_TPU11, A_TPU9, A_TPU7, A_TPU5, A_TPU3, A_TPU1	I/O	TPU I/O signals connected to the TPU A of the MPC565

Pin Number	Signal	I/O	Comments
Pin row X1B			
1B	CLKOUT	O	Processor clock of the MPC565
2B	/IRQ1	I	/IRQ1 interrupt request of the MPC565 Alternative: /RSV (O), SGPIOC1 (I/O)
3B	/IRQ2	I	/IRQ2 interrupt request of the MPC565 Alternative: /CR (I), SGPIOC2 (I/O), /MTS (O)
4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B, 84B, 89B, 94B, 99B	GND		Ground 0 V
5B	/CS3	O	/CS signal of the MPC565
6B	/CS0	O	/CS signal of the MPC565 used as control of the on-board Flash memory
7B	/OE	O	Output enable signal of the MPC565
8B, 10B, 11B, 12B, 13B, 15B, 16B, 17B, 23B, 25B, 26B, 27B	A31. A28, A26, A25, A23, A20, A18, A17, A15, A12, A10, A9	I/O	Address lines: A31 is the LSB! Alternative: SGPIOA31, SGPIOA28, SGPIOA26, SGPIOA25, SGPIOA23, SGPIOA20, SGPIOA18, SGPIOA17, SGPIOA15, SGPIOA12, SGPIOA10, SGPIOA9 (I/O) For use of the alternative function, note that the address lines are partially used for memory addressing.
18B, 20B, 21B, 22B, 28B, 30B, 31B, 32B, 37B, 38B, 40B, 41B, 42B, 43B, 45B, 46B	D31, D28, D26, D25, D23, D20, D18, D17, D15, D13, D10, D8, D7, D5, D2, D0	I/O	Data lines: D31 is the LSB and D0 is the MSB! Alternative: SGPIOD31, SGPIOD28, SGPIOD26, SGPIOD25, SGPIOD23, SGPIOD20, SGPIOD18, SGPIOD17, SGPIOD15, SGPIOD13, SGPIOD10, SGPIOD8, SGPIOD7, SGPIOD5, SGPIOD2, SGPIOD0 (I/O) For use of the alternative function, note that the address lines are partially used for memory addressing.
33B	/WE2	O	Write enable signal for data lines D[16..23] Alternative: AT2 (O) The alternative function can only be used when no on-board memory is populated.

Pin Number	Signal	I/O	Comments
35B	/BG	I/O	Bus grant signal of the MPC565 Alternative: VF0 (O), LWP1 (O)
36B	/BR	I/O	Bus request signal of the MPC565 Alternative: VF1 (O), IWP2 (O)
47B 48B 50B 65B 66B 67B	PLDIO0, PLDIO2, PLDIO4, PLDIO6, PLDIO8, PLDIO10	I/O	Free I/O pin of the PLD
51B	TSIZ1	I/O	Transfer size signal of the MPC565
52B	/WE1	O	Write enable signal for data lines D[8..15] Alternative: AT1 (O) The alternative function can only be used when no on-board memory is populated.
53B	/WE0	O	Write enable signal for data lines D[0..7]. Note that D0 represents the MSB! Alternative AT0 (O) The alternative function can only be used when no on-board memory is populated.
55B	/IRQ4	I	/IRQ4 interrupt request of the MPC565 Alternative: AT2 (O), SGPIOC4 (I/O)
56B	/IRQ5	I	/IRQ5 interrupt request of the MPC565 Alternative: SGPIOC5 (I) This signal is multiplexed with MODCK1. The input is not 3.3 V tolerant.
57B	/IRQ6	I	/IRQ6 interrupt request of the MPC565. This signal is multiplexed with MODCK2. The input is not 3.3 V tolerant.
58B	/IRQ7	I	/IRQ7 interrupt request of the MPC565. This signal is multiplexed with MODCK3. The input is not 3.3 V tolerant.
60B	VDDGOOD	O	Status output of the local supply voltages VDD5V, VDD3V3 and VDD2V6
61B	/VDDGOOD	O	Inverse VDDGOOD
62B	PLDTMS	I	JTAG TMS of the PLD
63B	PLDTCK	I	JTAG clock input of the PLD
68B	ZZ	I	Snooze enable input of the sync. SRAM devices: This active HIGH, asynchronous input causes the devices to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored. *For additional information refer the description of Jumper J21*.

Pin Number	Signal	I/O	Comments
70B 71B 72B 73B 75B 76B 77B 78B	C_TPU14, C_TPU12, C_TPU10, C_TPU8, C_TPU6, C_TPU4, C_TPU2, C_TPU0	I/O	TPU I/O signals connected with the TPU C of the MPC565
80B 81B 82B 83B 85B 86B 87B 88B	B_TPU14, B_TPU12, B_TPU10, B_TPU8, B_TPU6, B_TPU4, B_TPU2, B_TPU0	I/O	TPU I/O signals connected with the TPU B of the MPC565
90B	A_T2CLK	I/O	Clock signal of the TPU A of the MPC565
91B 92B 93B 95B 96B 97B 98B 100B	A_TPU14, A_TPU12, A_TPU10, A_TPU8, A_TPU6, A_TPU4, A_TPU2, A_TPU0	I/O	TPU I/O signals connected with the TPU A of the MPC565

Pin Number	Signal	I/O	Comments
Pin row X1C			
1C, 2C	+3V3	I	Supply voltage +3.3 VDC
3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C	GND	-	Ground 0 V
4C, 5C	+5V	I	Supply voltage +5 VDC
6C	VBAT	I	Connection for external battery (+) 2.4-3.3 V
8C	PWRGOOD	O	/PORESET signal
9C	TEXP / /RSTCNF	O	Timer expired output of the MPC565. Do not use for control of the reset config word. *Refer to J18*.
10C	/HRESET	I/O	Hard reset signal of the MPC565. An Open-Drain transceiver controls /HRESET.
11C	/PORSET	O	Power-on reset of the MPC565.
13C 14C 15C 16C 43C 44C 45C 46C	MPIO1, MPIO3, MPIO5, MPIO7 MPIO9 MPIO11 MPIO13 MPIO15	I/O	MIOS GPIO signals of the MPC565
18C	B_CANH	I/O	CANH output of the CAN transceiver of the second CAN interface.
19C	A_RXD2TTL	I	Receive line of the second MPC565 UART A. Alternative: QGPI2 general purpose input (I). When the alternative function is used, the solder jumper J24 must be open in order to disconnect the receive output of the RS-232 transceiver.
20C	A_TXD2TTL	O	Transmit line of the second MPC565 UART A. Alternative: QGPO2 general purpose output (O).
21C	RXD2	I	RxD input of the RS-232 transceiver of the second serial interface UART A. J24 must be closed in order to use this interface.
23C	TXD2	O	TxD output of the RS-232 transceiver of the second serial interface of UART A.

Pin Number	Signal	I/O	Comments
24C 25C	A_QGPIO1, A_QGPIO3,	I/O	General purpose input/output of the MPC565. Alternative: PCS1, PCS3 peripheral /CS signal of the QSPI interfaces. (I/O)
26C	A_QGPIO5	I/O	General purpose input/output of the MPC565. Alternative: MOSI master out/slave in of the QSPI interfaces. (I/O)
28C	ECK	I	External baud clock input of both UARTs of the MPC565.
29C	B_QGPIO1	I/O	General purpose input/output of the MPC565. Alternative: PCS1 peripheral /CS signal of the QSPI interfaces. (I/O)
30C	B_QGPIO3	I/O	PCS3 peripheral /CS signal of the QSPI interfaces. (I/O). Alternative: J1850 TX
31C	SCL	I/O	I^2C clock signal: The signal can be generated with MDA14 via software or by using an external pin. SCL and MDA14 can be connected using a 100R resistor at R60. R60 is **not** populated per default.
33C	LINKLED	O	Ethernet Link LED output.
34C	LANLED	O	Ethernet LAN LED output.
35C	ETHRXD-	I	Ethernet negative receive input.
36C	ETHTXD-	O	Ethernet negative transmit output.
38C	B_QGPIO5	I/O	General purpose input/output of the MPC565. Alternative: MOSI master out/slave in of the QSPI interfaces. (I/O)
39C	B_QGPO1	O	QGPO1 General purpose output (O). Alternative: transmit line of the first MPC565 UART B.
40C	B_QGPI1	I	QGPI1 General purpose input (I). Alternative: receive line of the first MPC565 UART B.
41C	SGPIOC7	I/O	General purpose input/output of the MPC565 Alternative: /IRQOUT interrupt out Alternative: LWP0 load/store watch point 0. After reset, the LWP0 function is active.
48C 49C 50C 51C 53C 54C	MDA11, MDA13, MDA15, MDA27, MDA29, MDA31	I/O	Double action I/O of the MPC565 MIOS. These signals serve either as input capture or output compare

Pin Number	Signal	I/O	Comments
55C 56C 58C 59C	MPWM1, MPWM3, MPWM17, MPWM19	I/O	PWM output or I/O signals of the MPC565 MIOS
60C	DSDI	I	Development serial data input of the MPC565 BDM interface. Alternative: TDI test data in of the MPC565 JTAG port.
61C	DSCK	I	Development serial clock of the MPC565 BDM port. Alternative: TCK test clock of the MPC565 JTAG port
63C	TMS	I	Test mode select of the MPC565 JTAG port
64C 65C 66C 68C 69C 70C	BDO1 BDO3 /MESO MDI1 /EVTI /RSTI	I/O	MPC565 ready port
71C	EPEE	I	This control signal externally controls the program or erase operations for the MPC565 Flash memory. When low, program or erase operations in both of the Flash UC3F modules (UC3F_512KA and UC3F_512KB) are disabled. A 10kOhm pull-down resistor is connected on-board.
72C, 77C, 82C, 87C, 92C, 97C	GNDA	-	Analog Ground 0 V
73C	ETRIG1	I	Trigger inputs of the QADC modules A and B on the MPC565
74C 75C 76C 78C	AN86, AN84, AN82 AN80	I	QADC inputs of the MCP565
79C 80C 81C 83C 84C 85C 86C 88C	B_AN78 B_AN76 B_AN74 B_AN72 B_AN70 B_AN68 B_AN66 B_AN64	I	QADC inputs of the MCP565

Pin Number	Signal	I/O	Comments
89C 90C 91C 93C 94C 95C 96C 98C	A_AN58 A_AN56 A_AN54 A_AN52 A_AN50 A_AN48 A_AN46 A_AN44	I	QADC inputs of the MCP565
99C	ALTREF	I	Alternate reference voltage input for the QADC.
100C	VDDA5V	O	Voltage supply +5 V of the analog signals. VDDA is coupled with VDD5V using a choke.

Pin Number	Signal	I/O	Comments
Pin row X1D			
1D, 2D	+3V3	I	Supply voltage +3.3 VDC
3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D	GND	-	Ground 0 V
4D, 5D	+2V6	-	Supply voltage +2.6 VDC
6D	VPD	O	Power-down supply voltage VPD is generated by VBAT or +3V3 using a diode-switcher. VPD serves as supply voltage for the MPC565 internal SRAM, the Real-Time Clock, and the serial EPROM
7D	/PFI	I	Power fail input is a TTL input that serves as a manual reset input for the /PORESET.
8D	/SRESET	I/O	Soft reset of the MPC565
10D	/HRESIN	I	Hard reset input controls the system Reset /HRESET.
11D 12D 13D 15D 45D 46D 47D 48D	MPIO0, MPIO2, MPIO4, MPIO6 MPIO8 MPIO10 MPIO12 MPIO14	I/O	MIOS GPIO MPIO32B signals of the MPC565
16D	A_RXD1TTL	I	Receive line of the first MPC565 UART. Alternative: QGPI1 general purpose input If the alternative function is used, the solder jumper J23 must be open in order to disconnect the receive output of the RS-232 transceiver.
17D	A_TXD1TTL	O	Transmit-line of the first MPC565 UART. Alternative: QGPO1 general purpose output
18D	B_CANL	I/O	CANL output of the CAN transceiver of the second CAN interface
20D	A_CANL	I/O	CANL output of the CAN transceiver of the first CAN interface
21D	A_CANH	I/O	CANH output of the CAN transceiver of the first CAN interface
22D	RXD1	I	RxD input of the RS-232 transceiver of the first serial interface. Jumper J23 must be closed to use this interface.
23D	TXD1	O	TxD output of the RS-232 transceiver of the first serial interface

Pin Number	Signal	I/O	Comments
25D	A_QGPIO0	I/O	General purpose input/output of the MPC565 Alternative: PCS0 peripheral /CS signals of the QSPI interfaces (I/O). SS: with the help of this bi-directional signal, the QSPI interface can switch into slave mode.
26D	A_QGPIO2	I/O	General purpose input/output of the MPC565 Alternative: PCS2, peripheral /CS signals of the QSPI interfaces (I/O)
27D	A_QGPIO4	I/O	General purpose input/output of the MPC565. Alternative: MISO master in/slave out of the QSPI interface (I/O).
28D	A_QGPIO6	I/O	General purpose input/output of the MPC565 Alternative: SCK clock of the QSPI interface (I/O)
30D	B_QGPIO0	I/O	General purpose input/output of the MPC565 Alternative: PCS0 peripheral /CS signals of the QSPI interfaces (I/O). SS: with the help of this bi-directional signal, the QSPI interface can switch into slave mode.
31D	B_QGPIO2	I/O	General purpose input/output of the MPC565 Alternative: PCS2, peripheral /CS signals of the QSPI interfaces (I/O)
32D	SDA	I/O	Data line of the I^2C bus. SDA can be connected to the MPC565 signal MDA15 via a 100 Ohm resistor at R61
33D	/IRTC	O	Interrupt output of the RTC. /IRTC can be connected to /WAKEUP using jumper J26
35D	ETHRXD+	I	Ethernet positive receive input.
36D	ETHTXD+	O	Ethernet positive transmit output.
37D	/LANIRQ	O	Ethernet interrupt output signal. /LANIRQ is connected to the CPLD and routed to /IRQ1 of the MPC565. For more information refer to section 7.
38D	B_QGPIO4	I/O	General purpose input/output of the MPC565. Alternative: MISO master in/slave out of the QSPI interfaces. (I/O)

Pin Number	Signal	I/O	Comments
40D	B_QGPIO6	I/O	General purpose input/output of the MPC565 Alternative: SCK clock of the QSPI interface (I/O)
41D	B_QGPO2	O	QGPO2 general purpose output (O). Alternative: transmit line of the second MPC565 UART B.
42D	B_QGPI2	I	QGPI2 general purpose input (I). Alternative: receive line of the second MPC565 UART B.
43D	SGPIOC6	I/O	General purpose input/output of the MPC565. Alternative: FRZ freeze (O) Alternative: /PTR program trace (O) The /PTR function is active after reset.
50D 51D 52D 53D	MDA12, MDA14, MDA28, MDA30	I/O	Double action I/O of the MPC565 MIOS. These signals serve either as input capture or output compare.
55D 56D 57D 58D	MPWM0, MPWM2, MPWM16, MPWM18	I/O	PWM output or I/O signals of the MPC565 MIOS.
60D	DSDO	O	Development serial data output of the MPC565 BDM port.
61D, 62D	VFLS0, VFLS1	O	Visible history buffer flush status of the MPC565 BDM port. Alternative: IWP[0,1] instruction watch point (O).
38D, 40D	MPIO2, MPIO0	I/O	MIOS GPIO signals of the MPC565 Alternative: VF2, VF0- Visible-Instruction-Queue-Flush-Status (VF bit in MIOS1TPCR) (O)
63D 65D 66D 67D 68D 70D	MCKO BDO0 BDO2 MCKI MDI0 /MSEI	I/O	MPC565 ready port

Pin Number	Signal	I/O	Comments
71D	B0EPEE	I	This signal externally controls the program or erase operations for the MPC565 Flash memory block 0. When low, program or erase operations in block 0 of the Flash UC3F module (UC3F_512KA) are disabled. A 10 kOhm pull-down resistor is connected on-board.
72D	ETRIG2	I	Trigger inputs of the QADC modules A and B on the MPC565.
73D 75D 76D 77D	AN87, AN85, AN83 AN81	I	QADC inputs of the MCP565.
74D, 79D, 84D, 89D, 94D, 99D	GNDA	-	Ground 0 V of the analog signals. GNDA is connected to GND using the 0R resistor at R2.
78D 80D 81D 82D 83D 85D 86D 87D	B_AN79 B_AN77 B_AN75 B_AN73 B_AN71 B_AN69 B_AN67 B_AN65	I	QADC inputs of the MCP565.
88D 90D 91D 92D 93D 95D 96D 97D	A_AN59 A_AN57 A_AN55 A_AN53 A_AN51 A_AN49 A_AN47 A_AN45	I	QADC Inputs of the MCP565
98D	VRL	I/O	Reference voltage of the QADC module. If Jumper J30=5+6, VRH is connected with GNDA. In order to use an external reference voltage, J30 must be opened.
100D	VRH	I/O	Reference voltage of the QADC module. If jumper J30=3+4, VRH is connected with VDDA5V. In order to use an external reference voltage, J30 must be opened.

Table 1: Pinout of the phyCORE-Connector X1

3 Jumpers

For configuration purposes, the phyCORE-MPC565 has 42 solder jumpers, some of which have been installed prior to delivery. *Figure 4* illustrates the numbering of the jumper pads, while *Figure 5* and *Figure 6* indicate the location of the jumpers on the board.

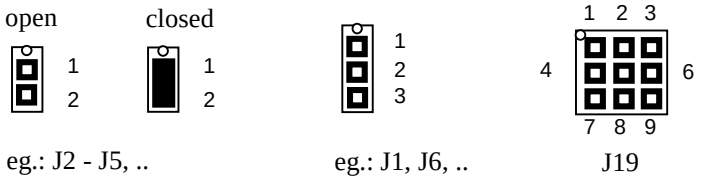


Figure 4: Numbering of the Jumper Pads

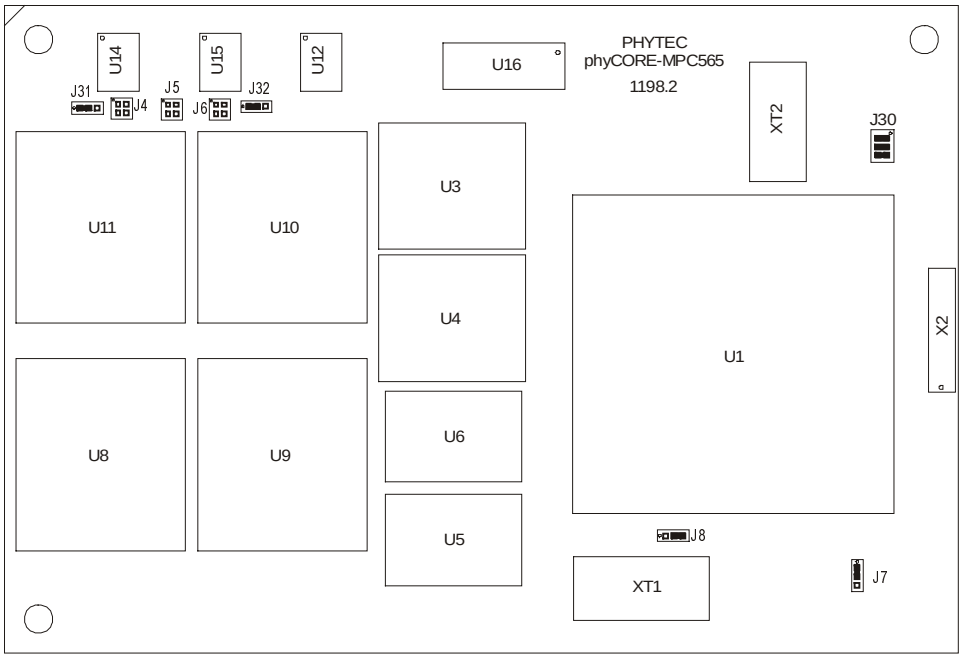


Figure 5: Location of the Jumpers (Controller Side) and Default Settings (phyCORE-MPC565 Standard Version)[1]

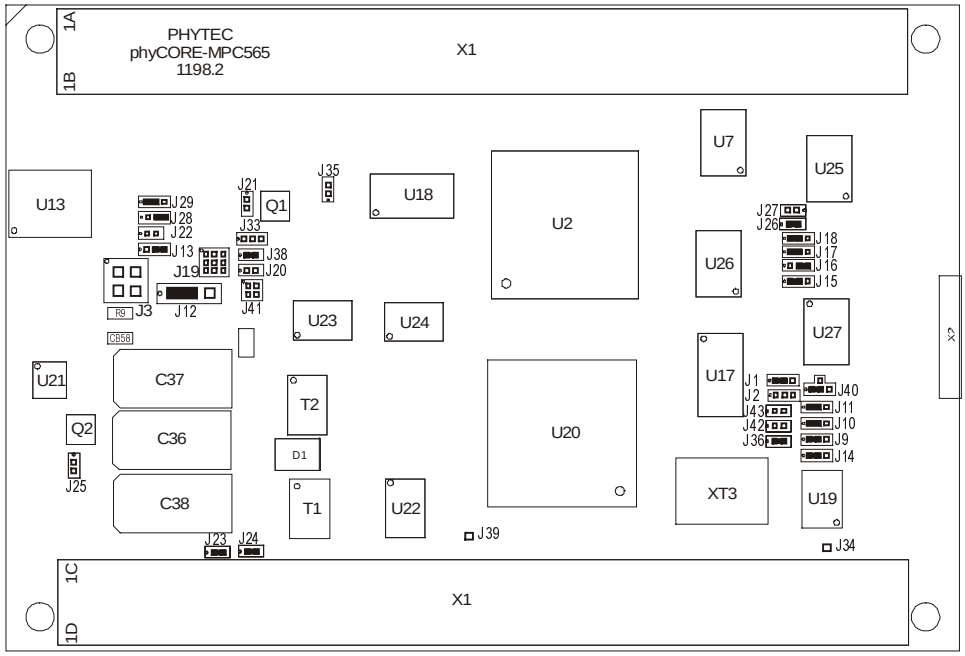


Figure 6: Location of the Jumpers (Connector Side) and Default Settings (phyCORE-MPC565 Standard Version)[1]

[1]: Jumper J19, J20, J38 and J41 may have different settings according to the purchased memory configuration of the phyCORE-MPC565.

The jumpers (J = solder jumper) have the following functions:

Jumper	Default	Comment
J1		This jumper connects /CS0 to /CSFL1 or /CSFL2.
1 + 2	X	Connects /CS0 to /CSFL1 (burst mode Flash).
2 + 3		Connects /CS0 to /CSFL2 (standard Flash). Do not set this configuration while factory default firmware is contained in the CPLD. The CPLD will drive /CSFL2 dependent on /CS2
Package Type		0R in SMD 0402
J2	open	This jumper connects /CS2 to /CSFL1 or /CSFL2.
1 + 2		Connects /CS2 to /CSFL1 (burst mode Flash).
2 + 3		Connects /CS2 to /CSFL2 (standard Flash). Do not set this configuration while factory default firmware is contained in the CPLD. The CPLD will drive /CSFL2 dependent on /CS2
Package Type		0R in SMD 0402
J3		The JTAG interface of the synchronous burst mode SRAM's connects to J3.
1		TCK signal. A 1kΩ pull-down is present.
2		TDI signal
3		TMS signal. A 1kΩ pull-up to VDD3V3 is present.
4		TDO signal
Pad Type		SMD 0402
J4		J4 bypasses the CAN signals of port B_CAN. This jumper must only closed if the transceiver circuit U14 is removed.
1 + 2		Bypasses B_CANTX0 to B_CANH pin of X1.
3 + 4		Bypasses B_CANRX0 to B_CANL pin of X1.
Package Type		0R in SMD 0402
J5		J5 connects the CANSTB signal to the CAN transceivers RS inputs (pin 8).
1 + 2		Connects CANSTB signal to RS input of the B_CAN (U14).
3 + 4		Connects CANSTB signal to RS input of the A_CAN (U15).
Package Type		0R in SMD 0402
J6		J6 bypasses the CAN signals of port A_CAN. This jumper must only closed if the Transceiver circuit U15 is removed**.**
1 + 2		Bypasses B_CANTX0 to A_CANH pin of X1.
3 + 4		Bypasses B_CANRX0 to A_CANL pin of X1.
Package Type		0R in SMD 0402

Jumper	Default	Comment
J7		J7 selects the power supply for the Keep Alive Power input (KAPWR) of the MPC565.
1 + 2	X	The module input voltage +2V6 supplies the KAPWR input.
2 + 3		The local power net VDD2V6 supplies the KAPWR input.
Package Type		0R in SMD 0402
J8		J8 configures the PULLSEL input of the MPC565. This signal determines whether the pull devices on the MIOS and TPU pins are pull-ups or pull-downs. When pull-ups are selected, the pull-ups are to 5V. The following MIOS pins always have pull-down resistors unless disabled in the PDMCR register: VF[0:2]/MPIO32B[0:2], VFLS[0:1]/MPIO32B[3:4], and MDO[7:4]/MPIO32B[7:10].
1 + 2		Select the pull-down resistors.
2 + 3	X	Select the pull-up resistors.
Package Type		0R in SMD 0402
J9		J9 selects the power supply for the internal SRAM1 (32 kByte CALRAM_A) module of the MPC565.
1 + 2	X	The module input voltage +2V6 supplies the on-chip SRAM.
2 + 3		The local power net VDD2V6 supplies the VDDSRAM1 input.
Package Type		0R in SMD 0402
J10		J10 selects the power supply for the internal SRAM2 (4kByte CALRAM_B) module of the MPC565.
1 + 2	X	The module input voltage +2V6 supplies the on-chip SRAM.
2 + 3		The local power net VDD2V6 supplies the VDDSRAM2 input.
Package Type		0R in SMD 0402
J11		J11 selects the power supply for the internal SRAM arrays in the DPTRAM_AB (6 kBytes), DPTRAM_C (4 kBytes), and the BBC DECRAM (4 kBytes) modules.
1 + 2	X	The module input voltage +2V6 supplies the on-chip SRAM.
2 + 3		The local power net VDD2V6 supplies the VDDSRAM3 input.
Package Type		0R in SMD 0402

Jumper	Default	Comment
J12		J12 selects the power supply for the external burst mode SRAM device U8.
1 + 2	X	The local power net VDD3V3 supplies U8.
2 + 3		The backup voltage VCAP3V3 supplies U8.
Package Type		0R in SMD 0805
J13		J13 selects the supply voltage (VPD or VDD5V) of the serial memory. VPD is used in the case that a serial SRAM, which requires buffering of its memory contents, populates the module. For EEPROM and FRAM memory, VDD5V is used, as these memory devices are not volatile.
1 + 2		The serial memory is supplied with VPD.
2 + 3	X	The serial memory is supplied with VDD5V.
Package Type		0R in SMD 0402
J14		J14 selects the supply voltage (VPD or VDD5V) for the RTC module into the MCP565.
1 + 2	X	The module input voltage +2V6 supplies the VDDRTC input.
2 + 3		The local power net VDD2V6 supplies the VDDRTC input.
Package Type		0R in SMD 0402
J15, J16, J17		These jumpers configure the clock mode of the MPC565. When /PORESET is active, the bit-pattern connects to the MODCK [1..3] signals of the MPC565. Only the standard configurations using the MPC565's oscillator and quartz are shown below. The default configuration depends on the frequency of the external quartz populating the module. Configurations for use of an external clock source can be found in the MPC565 user's manual.
1+2, 2+3, 1+2	X	4MHz Quartz, limp-mode activated (MODCK[1..3]=010)
Package Type		0R in SMD 0402

Jumper	Default	Comment
J18		J18 determines the source of the Hard Reset Configuration Word (HRCW). During /HRESET, the HRCW configures the MPC565.
1 + 2	X	The HRCW is read via the data bus. Except D20 the data bus is supported by pull-down resistors and accordingly guarantees a valid data word. J33 configures D20 and determines the internal or external Flash memory as boot code source.
2 + 3		Reads the internal default word as HRCW. /HC = 0: reads the bit-pattern (CMFCFIG) from the internal Flash /HC = 1: reads the internal default HRCW 0x00000000
Package Type		0R in SMD 0402
J19[1]		J19 connects the memory bank address signals BA0 and BA1 to the corresponding address lines of the processor. The configuration of these jumpers is dependent on the memory size of the synchronous burst SRAM populating the module. The factory setting of J19 is in accordance with the memory configuration of each individual module. All four memory banks are typically equipped with the same devices. Please note that jumper J20 must be specifically set in accordance with the board's memory configuration.. *Refer to section 6.4, Table 7 for a detailed overview of applicable jumper settings.*
Package Type		0R in SMD 0402
J20[1]		J20 connects the memory bank address signal BA1 to the processor address line A8. This jumper must be closed in the case that the module is populated with synchronous BURST-SRAM's that have a capacity of 1M x 32/36-bit (4MByte) or larger per device. Also jumper J19 must be specifically set in accordance with the board's memory configuration. The factory default setting of J20 will be set according to the particular memory configuration of each individual module. *Refer to section 6.4, Table 7 for a detailed overview of applicable jumper settings.*
Package Type		0R in SMD 0402
J21		J21 bridges the ZZ line to the ZZ0 signal of the first Synchronous Burst SRAM device U8. The ZZ line comes from X1 and connects the remaining SRAM devices U9-U11. ZZ0 is driven during /HRESET inactive by an open-drain driver. During /HRESET active ZZ0 is pulled high for data

Jumper	Default	Comment
		retention. ZZ can be driven by an I/O signal to enable the SNOOZE mode if J21 is open. This enables the phyCORE SRAM banks to be switched to an energy saving state via software. During this state, the memory cannot be read or written to. The connection of an I/O signal to ZZ has to be established externally.
open closed Package Type	X	Disconnects ZZ to ZZ0. Snooze mode is enabled by ZZ=high (driven externally) for the memory banks U9-U11. A pull-down held this line low. Connects ZZ to ZZ0. During normal operation ZZ0 respectively ZZ is driven low. 0R in SMD 0402
J22 open closed Package Type	 X	J22 switches Pin 7 of the serial memory at U12 to high-level. On many memory devices, Pin 7 enables the activation of a writing protection function. It is not guaranteed that the standard serial memory populating the phyCORE-MPC565 will have this writing protection function. *Please refer to the corresponding memory data sheet for more detailed information.* Writing protection function is deactivated.. Writing protection function is activated. 0R in SMD 0402

Jumper	Default	Comment
J23, J24		J23 and J24 disconnect the receive lines of MPC565 UART A from the RS-232 transceiver at U16. This makes the controller's RS-232 TTL-signals available at pins X1D16 (A_RXD1TTL) and X1C19 (A_RXD2TTL). This is useful, for instance, for optically decoupling the RS-232 interface.
open		The UART receive signals A_RXD1TTL and A_RXD2TTL are disconnected from the RS-232 transceiver.
closed	X	The UART receive signals A_RXD1TTL and A_RXD2TTL are connected to the RS-232 transceiver.
Package Type		0R in SMD 0402
J25		J25 connects the VBAT input to the local VCAP3V3. This mode can be used for buffering the first SRAM array U8 over the VBAT input. In this mode, a direct connection to an external Battery is not advisable. In runtime, +3V3 supplies VBAT.
open	X	Decouples VBAT from VCAP3V3. VBAT can be uses as battery input.
closed		Connects VBAT to VCAP3V3. In runtime, VCAP3V3 is connected to the module's input voltage +3V3.
Package Type		0R in SMD 0402
J26		Jumper J26 connects the alarm interrupt output of the Real-Time Clock (RTC) to the /WAKEUP signal of the power supply. Through programming of the RTC alarm functions, a precise wake up from a power down can be executed.
open		The signal /IRTC is disconnected from the /WAKEUP input. /WAKEUP is tied to the potential of the supply voltage +2V6 via the pull-up resistor R59.
closed	X	The signal /IRTC is connected with the /WAKEUP input. The interrupt output of the RTC is of open-drain type. /WAKEUP can further be used on the target hardware side (Wired-OR against GND).
Package Type		0R in SMD 0402
J27		Do not use. For testing purposes only.
open	X	
closed		Do not close!
Package Type		0R in SMD 0402

Jumper	Default	Comment
J28, J29		J28 and J29 define the slave addresses (A2 and A1) of the serial memory U12 on the I^2C bus. In the high-nibble of the address, I^2C memory devices have the slave ID 0xA. The low-nibble consists of A2, A1, A0, and the R/W bit. A0 is tied to GND. It must be noted that the RTC at U13 is also connected to the I^2C bus. The RTC has the address 0xA2/ 0xA3 which can not be changed.
1 + 2, 2 + 3		A2= 0, A1= 0, A0= 0 (0xA0 / 0xA1)
1 + 2, 1 + 2		A2= 1, A1= 0, A0= 0 (0xA8 / 0xA9)
2 + 3, 2 + 3		A2= 0, A1= 1, A0= 0 (0xA4 / 0xA5)
2 + 3, 1 + 2	X	A2= 1, A1= 1, A0=0 (0xAC / 0xAD) I^2C slave address 0xAC for the writing operations and 0xAE for reading access.
Package Type		0R in SMD 0402
J30		J30 is used to bridge the analog reference inputs ALTREF, VRH and VRL of the MPC565 QADC module to local potentials. To feed external reference voltages, leave the corresponding jumper connection open.
1 + 2	X	ALTREF connected to VDDA5V
3 + 4	X	VRH connected to VDDA5V
5 + 6	X	VRL connected to GNDA
Package Type		0R in SMD 0402
J31, J32		J31 and J32 serve to configure the CAN transceiver of TouCAN channels A and B on the MPC565. 82C251 (or compatible) devices are used as transceivers. Using a resistor tied to GND, the rise time of the CAN signal edge can be configured. With a 0R solder jumper against VDD5V, the transceivers are switched to stand-by.
1 + 2	X	0R resistor: minimal rise time
1 + 2		To reduce electromagnetic interference (EMI), a suitable resistor can populate the board in support of a lower baud rates.
2 + 3		0R resistor: Stand-by
Package Type		SMD 0402

Jumper	Default	Comment
J33		Determines the memory for a program start after reset.
1 + 2		Internal (on-chip) Flash memory (D20 –> VDD2V6)
2 + 3		External (on-board) Flash memory (D20 –> GND)
open	X	D20 must be externally configured via a 4k7 resistor
Package Type		0R in SMD 0402
J34		Test point for JCOMP signal.
Package Type		Single pad
J35		This jumper connects the PLD clock input CIN to the PLDIO0 signal.
open	X	CIN is not connected to PLDIO0.
closed		Connects CIN to PLDIO0.
Package Type		0R in SMD 0402
J36		Connects the processor's /CS1 to the /CSRAM Chip Select signal. /CSRAM controls the entire sync. SRAM memory bank.
open		/CSRAM is controlled by EPLD pin 16.
closed	X	/CS1 controls /CSRAM. The EPLD pin 16 must be inactive. This is determined by the EPLD firmware (default).
Package Type		0R in SMD 0402
J37		J37 connects the processor signal /BDIP to the /BAA input on both burst mode Flash devices at U3 and U4.
open	X	Current Flash devices do not need this connection. The burst mode is configured by software to a fixed scheme.
closed		For Flash devices that support this feature.
Package Type		0R in SMD 0402
J38		J38 connects the inverted SRAM bank address signal /BA1 to the devices.
open		/BA1 controlled by EPLD output pin 3.
closed	X	/BA1 controlled by inverter logic U7B. EPLD pin 3 must be inactive (default with standard firmware).
Package Type		0R in SMD 0402
J39		The ACC/VPP pins of the burst mode Flash memory devices U3 and U4 are connected to this test point.
Package Type		Single pad.

Jumper	Default	Comment
J40		J40 connects the highest address line to the decoder logic that controls the selection of the Burst-Mode Flash memory devices U3 and U4. This jumper is independent of the populated memory device. It predefines an 2 MByte address space for each Flash device. This means, the first device starts at 0x0 and the second device starts at an offset of 0x200000 relative to the base address for the processor Chip Select that is used to control the devices (*refer to J1 and J2*).
1 + 2	X	2 MByte address range
2 + 4		4 MByte address range
3 + 2		8 MByte address range
Package Type		0R in SMD 0402
J41		J41 connects the SRAM bank address signals BA0 and BA1 to GND. This jumper will be configured (factory default) depending on the memory devices populating the module. U8 only 1 + 2 and 3 + 4 U8 and U9 3 + 4 U8 to U11 open *Refer to section 6.4, Table 7 for a detailed overview of applicable jumper settings.*
1 + 2		Connects BA0 signal to GND.
3 + 4		Connects BA1 signal to GND
Package Type		0R in SMD 0402
J42		J42 connects the processor's Chip Select signal /CS3 to the second burst mode Flash memory device at U4. For this mode the logic device U27 must be removed, in order to avoid signal collision of its output driver with /CS3.
open	X	/CSFL1B is provided from the logic device at U27.
closed		Connects /CS3 to /CSFL1B. U27 must be removed!
Package Type		0R in SMD 0402
J43		J43 connects the Chip Select signal /CSFL1 to the first Burst-Mode Flash memory device at U3. For this mode the logic device U27 must be removed, in order to avoid signal collision of its output driver with /CSFL1. /CSFL1 configures J1 or J2 to the desired processor chip select output /CS0 or /CS2.
open	X	/CSFL1B is provided from the logic device U27.
closed		Connects /CSFL1 to /CSFL1B. U27 has to be removed.
Package Type		0R in SMD 0402

Table 2: Jumper Settings

[1]: Jumper J19 ,J20 and J41 may have different settings according to the purchased memory configuration of the phyCORE-MPC565.

4 Power System and Reset Behavior

The phyCORE-MPC565 must be supplied with three different supply voltages:

Supply voltage 1: +3.3 V
Supply voltage 2: +5 V
Supply voltage 3: +2.6 V

Caution:
All three supply voltages are required for proper operation of the phyCORE-MPC565. The module must **never** be put into operation whit only one or two of the supply voltages are connected to the device! This might render the module inoperable.

The power supplies are connected to the module via Field Effect Transistors. These FET switches can be switched off via software using the TEXPS bit found in the PLPRCR register. This supports the MPC565's "Power Down" energy savings mode. *Figure 7* depicts the generation and the distribution of the supply voltages.

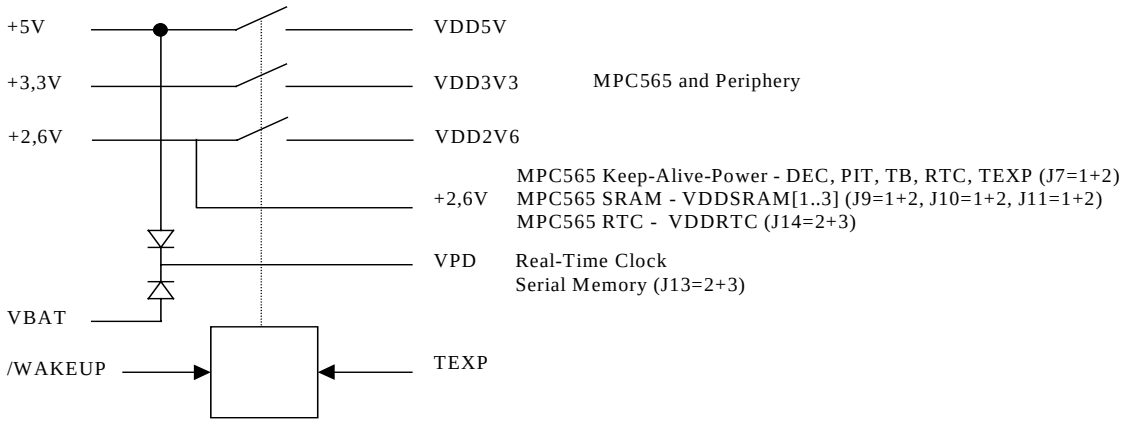


Figure 7: Power Concept

Power-On Behavior

When all supply voltages are attached to the corresponding ports of the module, a power-on reset (/PORESET) cycle will start. After successful completion of this cycle (/PORESET inactive), the hard-reset cycle is triggered. During the hard-reset cycle, the FET switch is automatically activated in order to set up the local supply voltages, VDD5V, VDD3V3 and VDD2V6. The /HRESET cycle is fully completed when all local voltages have reached a valid level and the /HRESET timeout of the reset device has occurred. The processor is now fully functional and will start program execution with the commands given at the reset exception address 0x00000100.

Power-Off Behavior

When the power-down mode of the MPC565 has been programmed, the bit/signal TEXPS/TEXP will turn off the FET switches. The local supply voltages, VDD5V, VDD3V3 and VDD2V6, will drop to zero and the board will remain without power. Only the components in the MPC565 that control this mechanism are still supplied with power (direct from input +2.6 V). The power consumption is reduced to a minimum. /PORESET and /HRESET remain inactive (high) during this state.

Wake-Up Behavior

After an event that negates the TEXP signal, the FET switch is activated again and the /HRESET cycle will start. Such an event can include a decrementer overflow, etc. A renewed /PORESET cycle will not run. Therefore the wake-up time of the processor depends only upon the /HRESET cycle. Events that do not originate from the MPC565 can also trigger a wake-up. Such events may include an alarm interrupt of the on-board Real-Time Clock (U13, RTC8564) or a low-level at the /WAKEUP port (pin X1A61 of the phyCORE-connector).

The alarm interrupt (/IRTC) must either be connected to the /WAKEUP signal of the board, via jumper 26, or routed back externally (pin X1D33 connected to pin 1A61). Even if the /IRTC is connected to /WAKEUP, additional input sources may be connected. For additional input sources, a wired-OR connector (open-drain or open-collector transceiver) must be connected to GND.

5 Start-up System Configuration

The system configuration occurs in multiple phases. This section describes the mechanism that is active until execution of the initial software commands.

- Power-on reset phase
- Hard-reset phase
- Initialization via software

5.1 Power-On Reset Phase

The processor's clock generator is configured during the power-on reset phase with the help of jumpers J15, J16, and J17. Depending on the desired clock source, a corresponding bit pattern must be present. During the /PORESET phase, the static bit pattern is connected to the processor lines MODCK[1..3]. Because these signals are multiplexed with the interrupt inputs /IRQ5, /IRQ6, and /IRQ7, an on-board multiplex device ensures proper signal routing.

J15	J16	J17	Clock Mode
1 + 2	2 + 3	2 + 3	20 MHz quartz, limp mode activated (MODCK[1..3]=011)
1 + 2	1 + 2	2 + 3	20 MHz quartz, limp mode deactivated (MODCK[1..3]=001)
1 + 2	2 + 3	1 + 2	4 MHz quartz, limp mode activated – default (MODCK[1..3]=010)

Caution:
Special care should be taken when initializing the PLL. Make sure the proper values are configured and the processor system is not clocked with a higher value then specified. This may result in system failure. We recommend to integrate a special software routine into the startup code that checks the status of the PLL to avoid clock failures.

5.2 Hard Reset Configuration Word

The components of the MPC565 which are necessary for accessing and executing the start-up code are initialized during the hard reset phase. A data value, the hard-reset configuration word (HRCW), determines the initialization process. The HRCW can be supplied by various sources. Possible sources are the data bus, the internal (on-chip) Flash memory or an internal default data value.

The sources for the HRCW are determined by two conditions: the setting of jumper J18 and the /HC bit in the internal Flash memory.

External HRCW

When J18 is closed at 1+2, the HRCW is read via the data bus. On the phyCORE-MPC565, pull-down resistors are connected to the data bus (except D20). The signal level of D20 is configured to low or high via jumper J33. D20 determines the Flash memory that is active after reset (1+2 = internal Flash, 2+3 = external Flash at /CS0).

Internal Default HRCW

If J18 is closed at 2+3 and /HC = 1 (Flash is cleared), then the internal default HRCW 0x00000000 is read.

Internal Flash HRCW (UC3FCFIG)

If J18 is set at 2+3 and /HC=0, the bit-pattern (UC3FCFIG) from the internal Flash is read.

6 System Memory

Two memory models can be distinguished when using the phyCORE-MPC565: the memory model that is active after reset and the runtime model. The runtime model can be configured via software.

6.1 Memory Model after Reset

After reset, the memory model is defined via a special mechanism. While /HRESET is active, the memory model, as well as several other system configurations, are determined by the hard reset configuration word (HRCW).

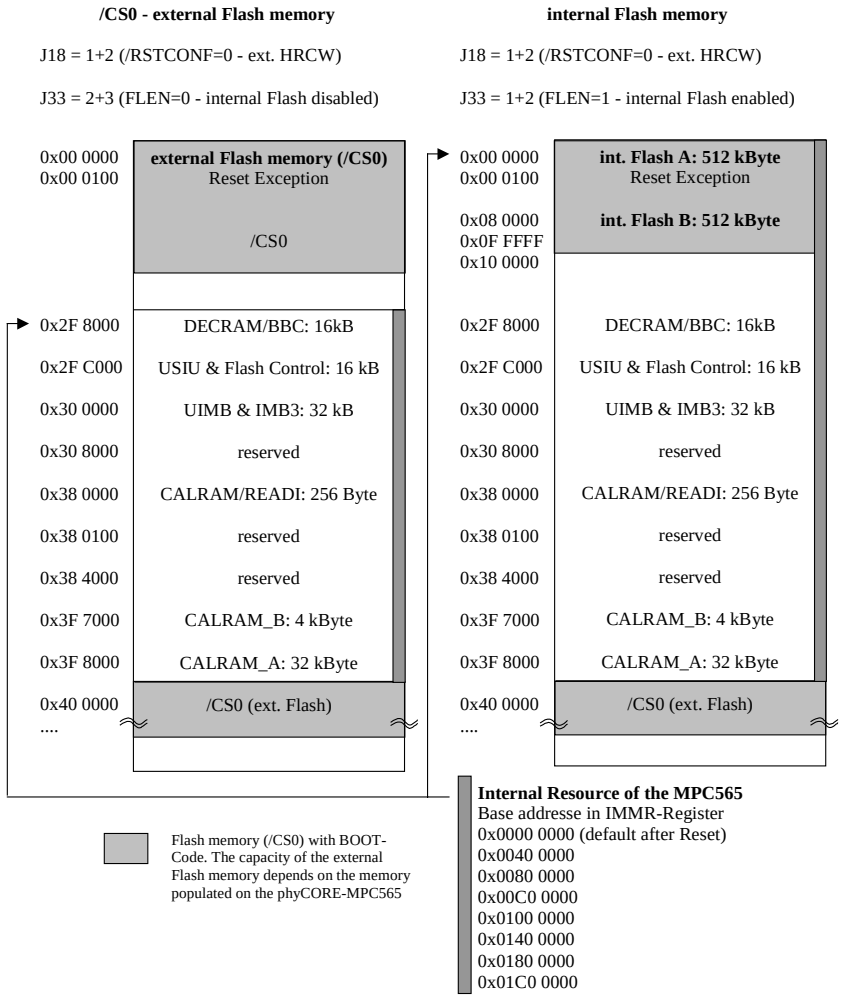


Figure 8: Default Memory Model after Hardware Reset

- Starting from external memory controlled by /CS0

  Configuration: J33 = 2 + 3 (FLEN bit in HRCW is zero)

  Following a reset, the address space for /CS0 is pre-initialized to cover the entire memory space and begins from the absolute address 0x0000 0000 excluding the internal register resources. This means that any access within the address space will show the content – or mirrored content - of the Flash memory connected to /CS0. To enable additional Chip Select signals, the startup code must reduce the address mask in the OR0 register to release parts of the address space for additional Chip Select channels. The internal resources start at address 0x002F 8000. The base address of the internal resources can be changed in the IMMR register. As *Figure 8* depicts seven configuration options are available.

  After reset, the processor runs code from the reset exception location at address 0x0000 0100.

  It is also possible to map the external Flash memory into a completely different address space. This depends on the application requirements and is further determined by the runtime memory model.

- Starting from internal Flash memory

  Configuration: J33 = 1 + 2 (FLEN bit in HRCW is one)

  Following a reset, the internal Flash memory array is present starting at address 0x0000 0000. In this case Chip Select channel 0 (/CS0) is disabled for the first 4 MByte address space. During runtime, /CS0 can be re-enabled for the first 4 Mbyte in user software by programming the FLEN-bit (IMMR register). The processor runs code starting from the reset exception location at 0x0000 0100.

6.2 Runtime Memory Model

The runtime memory model is configured by software in the internal registers of the MPC565. A register set (BR-, OR-register) exists for every Chip Select signal. The base address, the size of the address space and the bus characteristic are configured in these registers.

- Default Chip Select assignment

MPC565 Chip Select	Periphery Chip Select	Periphery Device
/CS0	/CSFL1	on-board Burst Mode Flash memory First device at U3: lower 8 MByte Second device at U4: upper 8 MByte
/CS1	/CSRAM	on-board Burst SRAM
/CS2	/CSFL2 /CSLAN	on board standard Flash memory, lower 8 MByte (A8=0) on board Ethernet controller, upper 8 MByte area (A8=1)
/CS3	-	Free

Table 3: Default Chip Select Assignment

The Chip Select assignment can be configured by reprogramming the on-board system logic device populating U2 (EPLD) and/or changing the soldering jumper J1, J2, J36, J42 and J43 (*refer to section 3*).

The runtime memory model is dependent on the application requirements. *Table 4* shows example configurations.

Address Space	**Space**	**Peripheral**	**MPC565 Register**
0x0000 0000 0x000F FFFF	1 MByte	MPC565 on-chip Flash	IMMR[FLEN] = 1b IMMR[ISB]= 000b
0x002F 8000 0x002F FFFF		MPC565 Periphery	IMMR[ISB]= 000b
0x0000 0000 0x007F 0000	16 MByte	/CS0 - /CSFL1 Burst Mode Flash	IMMR[FLEN] = 0b BR0= 0x0000 000B OR0= 0xFF00 0020
0x1000 0000 0x00FF FFFF	16 MByte	/CS1 - /CSRAM Burst SRAM	BR1= 0x1000 0001 OR1= 0xFF00 0000
0x2000 0000 0x207F FFFF	8 MByte	/CS2 - /CSFL2	BR2= 0x2000 0007 OR2= 0xFF00 00F0
0x2080 0000 0x20FF FFFF	8 MByte	/CS2 - /CSLAN	
0x3000 0000 0x30FF FFFF	16 MByte	/CS3 – free.	BR3= 0x3000 XXXX OR3= 0xFF00 XXXX

Table 4: Runtime Memory Map

The register values for /CS3 depend on the connected peripherals. The places designated with an “X” determine the specific characteristics (bus-width, burst or non-burst, etc.) of the bus interface.

6.3 Flash Memory

Use of Flash as non-volatile memory on the phyCORE-MPC565 provides an easily reprogrammable means of code storage. Various Flash devices can be used on the phyCORE-MPC565.

- Internal MPC565 Flash memory
- External burst mode Flash memory
- External standard Flash memory

6.3.1 Internal Flash Memory of the MPC565

To program the internal Flash memory of the MPC565, the on-chip Flash must first be unlocked with the B0EPEE and/or EPEE signal. B0EPEE/EPEE can be contacted via the pin X1D71/X1C71 in the connector lining the edge of the module. B0EPEE and EPEE are pulled to GND via on-board pull-down resistors. These signals must be pulled to high level for activation.

B0EPEE	controls the Flash block 0
EPEE	controls the remaining Flash blocks

For more details refer to the Motorola MPC565 Reference Manual.

6.3.2 External Burst Mode Flash Memory (U3, U4)

The burst mode Flash memory bank supports the following AMD memory devices:

Type	Size	Manufacturer	Device Code	Manufacturer Code
Am29BDD160G	2 MByte	AMD	007E	01

Table 5: Choice of Burst Mode Flash Memory Devices and Manufacturers

The organization of the burst mode Flash device is 32-bit width. Two of these 32-bit memory devices are connected to the system bus controlled by a processor Chip Select signal (/CS0 as default). U3 represents the first and U4 the second memory device. The first device is accessible starting at address 0x0 and address space of the second device starts at 0x200000 (2 MByte) relative to the base address of the processor's Chip Select signal. This memory arrangement is configured by the solder jumper J40. These two memory devices are completely independent. This means program and erase operations can be done in one device while code runs in the other device.

The access speed depends on the MPC565 processor clock. For asynchronous access the following values apply:

40 MHz processor frequency	2 wait states
56 MHz processor frequency	3 wait states

Burst mode access runs without wait states (0 wait states) and is supported up to 56 MHz bus frequency.

After reset, the devices always start in asynchronous mode. To enter the burst mode, a special initialization sequence must be sent to the memory devices.

The burst mode memory bank is controlled by the periphery Chip Select signal /CSFL1. For standard configuration, /CSFL1 is connected to the MPC565 Chip Select signal /CS0.

No additional voltages are needed for in-system programming. As of the printing of this manual, Flash devices generally have a life expectancy of at least 1 million erase-/program cycles. *Refer to the applicable AMD data sheet for detailed description of the erasing and programming procedure.*

6.3.3 External Standard Flash Memory (U5, U6)

The Flash memory devices used on the phyCORE-MPC565 operate in 16-bit mode and are organized in 32-bit with. The device at U5 connects to the low data bus while device U6 connects to the high data bus.

Type	Size	Manufacturer	Device Code	Manufacturer Code
29LV800T/B	1 MByte	AMD	22DA/225B	01
29LV160T/B	2 MByte	AMD	22C4/2249	01
29LV320T/B	4 MByte	AMD	22F6/22F9	01
29DL800T/B	1 MByte	AMD	224A/22CB	01

Table 6: Choice of Standard Flash Memory Devices and Manufacturers

The access speed depends on the MPC565 processor frequency and the speed grade of populated flash devices. The speed grade varies due to production deviations. To provide for a worst case scenario take the following values into consideration:

56 MHz processor frequency	4 wait states
40 MHz processor frequency	3 wait states

Caution:
Wait states are not configurable in the option register (OR2) of the MPC565 memory controller unit. The bus cycles will be controlled externally by the system logic controller U2 (EPLD). Therefore, the memory base register BR2 should always be programmed for external assertion of the transfer acknowledge signal /TA (bit SETA=1).

The Flash memory bank is controlled by the periphery Chip Select signal /CSFL2. For standard configuration, /CSFL2 is connected to the MPC565 Chip Select signal /CS2. /CS2 is also used to access the Ethernet device. Due to this fact, the memory space is divided into two 8 MByte sections handled by the re-programmable system logic device (EPLD) at U2. The Flash area is located in the lower 8 MByte address range. The memory space of /CS2 should always be configured to 16 MByte address range.

Use of Flash memory enables in-circuit programming of the module. The Flash devices on the phyCORE-MPC565 are programmable at 3.3 VDC. Consequently, no dedicated programming voltage is required. As of the printing of this manual, Flash devices generally have a life expectancy of at least 100,000 erase/program cycles.

6.4 Synchronous Burst SRAM (U8 - U11)

Use of synchronous flow-through burst SRAM supports the fastest mode of the MPC565 memory interface. The memory is organized in 32-bit width and consists of four banks. These banks appear to the processor as linear address spaces and do not require special activation. The memory is generally accessed via /CS1 without wait states.

The phyCORE-MPC565 can be populated with memory devices of various capacities. Generally, each memory bank can only be populated with memory devices of a consistent size. Solder jumpers J19, J20 and J41 are used to configure the memory capacity.

Table 7 shows all of the possible memory configurations.

Capacity	Type	Device	J19	J20	J41
0	N.A.	N.A.	open	open	open
256 kByte	64k x 32/36-bit	U8	open	open	1 + 2, 3 + 4
512 kByte	64k x 32/36-bit	U8-9	1 + 4	open	3 + 4
	128k x 32/36-bit	U8	open	open	1 + 2, 3 + 4
1 MByte	64k x 32/36-bit	U8-11	1 + 4, 2 + 3	open	open
	128k x 32/36-bit	U8-9	3 + 6	open	3 + 4
	256k x 32/36-bit	U8	open	open	1 + 2, 3 + 4
2 MByte	128k x 32/36-bit	U8-11	3 + 6, 5 + 8	open	open
	256k x 32/36-bit	U8-9	5 + 6	open	3 + 4
	512k x 32/36-bit	U8	open	open	1 + 2, 3 + 4
4 MByte	256k x 32/36-bit	U8-11	5 + 6, 7 + 8	open	open
	512k x 32/36-bit	U8-9	4 + 7	open	3 + 4
8 MByte	512k x32/36-bit	U8-11	4 + 7, 8 + 9	open	open
	1M x 32/36-bit	U8-9	6 + 9	open	3 + 4
16 MByte	1M x 32/36-bit	U8-11	6 + 9	closed	open

Table 7: Memory Options for the Synchronous Burst SRAM

6.5 Serial Memory (U12)

The phyCORE-MPC565 features a non-volatile memory device with a serial I^2C interface. This memory can be used for storage of configuration data or operating parameters, that must not be lost in the event of a power interruption. Depending on the module's configuration, this memory can be in the form of an EEPROM, FRAM or SRAM. The available capacity ranges from 512 Byte to 32 kByte or more.

If SRAM is used, solder jumper J13 must be closed at position 2+3 to supply the memory device via VPD. Because the MPC565 does not provide an on-chip I^2C interface, the protocol has to be generated by software. The processor port pins MDA15 and MDA14 can be connected to SDA and SCL using the resistors R61 and R60. As default, these resistors are not populated on the module. We recommend to establish the connection of SCA and SCL externally. This enables the user to choose different processor I/O signals.

Table 8 gives an overview of the possible devices for use at U12 as of the printing of this manual.

Type	Size	I^2C Frequency	Address Pins	Write Cycles	Life of Data	Device	Manufacturer
EEPROM	256/512 Byte	400 kHz	A2, A1, A0	1 000 000	100 yrs.	CAT24WC02/04	CATALYST
	1/ 2 kByte	400 kHz	A2, A1, A0	1 000 000	100 yrs.	CAT24WC08/16	CATALYST
	4/8 kByte	400 kHz	A2, A1, A0	1 000 000	100 yrs.	CAT24WC32/64	CATALYST
	32 kByte	1 MHz	A1, A0	100 000	100 yrs.	CAT24WC256	CATALYST
FRAM	512 Byte	1 MHz	A2, A1	10 billion	10 yrs.	FM24C04	RAMTRON
	8 kByte	1 MHz	A2, A1, A0	10 billion	10 yrs.	FM24C64	RAMTRON
SRAM	256 Byte	100 kHz	A2, A1, A0	-	-	PCF8570	PHILIPS

Table 8: Serial Memory Options for U12

It is important to note that the RTC is also connected to the I^2C bus. The RTC can operate with a bus frequency up to 400 kHz. Therefore the use of high bus frequencies for accessing the serial memory is not recommended. The RTC has the I^2C bus slave address 0xA2 / 0xA3. The slave address of the serial memory must be selected accordingly using the solder jumpers J28 (A1) and J29 (A2), so that no collision occurs. The address input A0 is hardwired to GND.

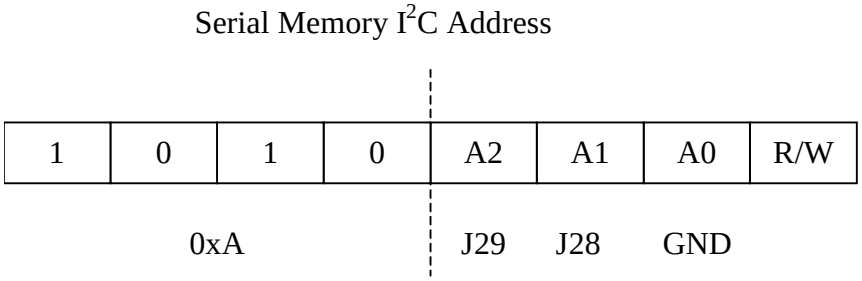


Figure 9: Serial Memory I²C Slave Address

Possible configuration options are shown below:

I²C Address	**J28 A1**	**J29 A2**
0xA0 / 0xA1	1 + 2	2 + 3
0xA4 / 0xA5	2 + 3	2 + 3
0xA8 / 0xA9	1 + 2	1 + 2
0xAC / 0xAD	2 + 3	1 + 2

Table 9: Serial Memory I²C Address (Examples)

Address lines A1 and A2 are not always made available by certain serial memory types. This should be noted when configuring the I²C bus slave address.

7 System Logic Device (EPLD) U2

The system logic device at U2 is responsible for the resource routing from the MPC565 microcontroller to the peripheral components. The device used on the phyCORE-MPC565 is an in-system re-programmable type supplied by Lattice Semiconductor (www.latticesemi.com). It is a member of the high-speed, low power ispMACH4000 family. In-system re-programming is provided via a separate JTAG interface with its signals available at the module's phyCORE-connector at X1.

The ispMACH LC4064V25T100-5I device populates the standard version of the phyCORE-MPC565.

The following section gives an overview of the logic equations. The complete design is contained in the BSP (Board Support Package). Refer to the folder ..*Lattice*\.. for the source code.

```
/CSFL2      = /CS2 & !A8;     // Standard Flash memory U5 and U6
/CSLAN      = /CS2 & A8       // Ethernet controller U20

LANA1       = A19;            // Ethernet address line A1
LANA2       = A18;            // Ethernet address line A2
LANA3       = A17;            // Ethernet address line A3

LANDIR      = RDNWR;          // Bus buffer direction signal
LANEN       = /CS2 & A8;      // Bus buffer enable signal
/IRQ1       = /LANIRQ;        // Ethernet interrupt
LANRESET = !/HRESET;          // Ethernet reset line
/LANSTB     = inactive;       // Ethernet always full operation
```

/TA controls a synchronous state machine that is initiated by /CS2

A number of free I/O pins (PLDIO[0..10]) are reserved for future functions. These pins can be used to create specific functionality required by the application periphery externally. For example, additional Chip Select lines can be easily created by adding simple equations to the logic source.

Example for additional external Chip Select generation relative to the base address of the processor /CS3:

```
/PLDIO0 = /CS3 & !A13 & !A14 & !A15;  // 0x00000 to 0x0FFFF
/PLDIO1 = /CS3 & !A13 & !A14 &  A15;  // 0x10000 to 0x1FFFF
/PLDIO2 = /CS3 & !A13 &  A14 & !A15;  // 0x20000 to 0x2FFFF
```

...and so on ...

The logic code is developed in ABEL source structure and can be re-written, compiled and fitted with the Lattice ispLEVER design software. A fully functional trial version is provided free of charge by Lattice Semiconductor. To download the installation package please go to the web page www.latticesemi.com.

The included programming tool Lattice ispVM handles the output of the source compiler/fitter and communicates over the printer port via the isp/BDM-DB25 connector located on the PHYTEC phyCORE Development Board PCM-991.

Jumper J31 on the Development Board must be closed in order to support reprogramming the EPLD at U2. Jumper J31 activates the isp-functionality (isp – In-System Programming) of the interface logic located on the Development Board and holds the phyCORE-MPC565 target system in reset state. The interface logic connects the JTAG port of the EPLD with the BDM-DB25 connector. With the power supply attached to X6, the system is ready for the reprogramming procedure (*refer also to section 11.3.11*).

Caution:
Changes in the logic design may alter the system performance and result in instability and malfunction of the phyCORE-MPC565.

8 Serial Interfaces

8.1 RS-232 Interface

A dual-channel RS-232 transceiver is located on the phyCORE-MPC565 at U16. This device adjusts the signal levels for the A_RxD1TTL/A_TxD1TTL and A_RxD2TTL/A_TxD2TTL lines (first MPC565 UART). The RS-232 interface enables connection of the module to a COM port on a host-PC. In this instance the RxD1 or RxD2 line (X1D22 / X1C21) of the transceiver is connected to the corresponding TxD line of the COM port; while the TxD1 or TxD2 line (X1D23 / X1C23) is connected to the RxD line of the COM port. The Ground circuitry of the phyCORE-MPC565 must also be connected to the applicable Ground pin on the COM port.

The micrcontroller's on-chip UART does not support handshake signal communication. However, depending on user needs, handshake communication can be replicated using port pins on the microcontroller. Use of an RS-232 signal level in support of handshake communication requires use of an external RS-232 transceiver not located on the module.

Furthermore it is possible to use the TTL signals of both of the UART channels externally. These signals are available at X1D16, X1C54 (A_RxD1TTL, A_TxD1TTL) and X1C19, X1C20 (A_RxD2TTL, A_TxD2TTL) on the phyCORE-connector. External connection of TTL signals is required for galvanic separation of the interface signals. Using the solder jumpers J23 and J24, the TTL transceiver outputs of the on-board RS-232 devices can be disconnected from the receive lines A_RxD1TTL and A_RxD2TTL. This is required so that the external transceiver doesn't drive signals against the on-board transceiver. The transmit lines A_TxD1TTL/A_TxD2TTL can be connected parallel to the transceiver input without causing any signal conflicts.

8.2 CAN Interface

Two CAN transceivers (82C251 or 82C250) populate the phyCORE-MPC565 module at U14 / U15. The signals for the third CAN interface of the MPC565 with their logic levels as generated by the controller are available on the phyCORE-connector pins X1C45 (C_CANTX) and X1D48 (C_CANRx).

The on-board transceivers enable transmission and reception of CAN signals via A_CNTX0 / A_CNRX0 and B_CNTX0 / B_CNRX0. The CAN transceivers support transmission speeds of up to 1 MBit/s and connection of up to 110 nodes on a single CAN network. Data transmission occurs with differential signals between CANH and CANL. A Ground connection between nodes on a CAN bus is not required, yet is recommended to better protect the network from electromagnetic interference (EMI). Additionally, the common mode voltage of both CAN transceivers must not exceed the specified threshold: -8 V / +18 V for the 82C250 and ±40 V for the 82C251. If the CAN bus system exceeds these limiting values optical isolation of the CAN signals is required. For larger CAN bus systems, an external opto-coupler should be implemented to galvanically separate the CAN transceiver and the phyCORE-MPC565.

To add external circuits for optical isolation, the CAN transceivers must be removed and the CAN bus signals bypassed by means of soldering jumpers J4 and J6. Then the CAN TTL signals are routed to pins X1C18, X1D18 (B_CNTX0, B_CNRX0) and X1D21, X1D20 (A_CNTX0, A_CNRX0) of the phyCORE-connector.

For connection of the CANTx and CANRx lines to an external transceiver we recommend using a Hewlett Packard HCPL06xx, Toshiba TLP113, Sharp PC410L0NIP or similar fast opto-coupler. Parameters for configuring a proper CAN bus system can be found in the DS102 norms from the CiA[1] (CAN in Automation) User and Manufacturer's Interest Group.

[1] CiA CAN in Automation -.Founded in March 1992, CiA provides technical, product and marketing information with the aim of fostering Controller Area Network's image and providing a path for future developments of the CAN protocol.

In order to ensure proper message transmission over the CAN bus, a 120 Ohm termination resistor must be connected to each end of the CAN bus between the CAN_H and CAN_L signals.

Configuration of the On-Board Transceiver:

Populating jumpers J31 and J32 with a 10k resistor, the transceivers at U14 and U15 can be switched to stand-by (position 2+3). Closing jumper J5 routes the standby inputs to the phyCORE-connector at pin X1A59. This enables external control of the transceivers.
Furthermore, the rise time can be configured by closing both jumpers at 1+2 (leaving 2+3 open). This results in reduced interference from the CAN bus when using lower baud rates. *For additional information refer to the data sheet for the 82C250/82C251 CAN transceivers*.

8.3 BDM-Debug Interface

The MPC565 offers an on-chip Background Debug (BDM) interface. This interface allows external debug access to the controller without requiring a service software or firmware, such as a Monitor program, running on the chip. This internal debug interface also contains hardware features supporting use with common cross development systems and debug environments, such as Metrowerks‘ CodeWarrior. For instance, the MPC565 features internal breakpoint registers enabling debugging in Flash-ROM memory.

The on-chip BDM interface extends from the MPC565 to a 10-pin connector at which an external BDM signal converter circuitry, such as a Wiggler, can be attached. Such BDM signal converters enable connection of the MPC565 to a host-PC for debugging purposes. This BDM connector is **NOT** located on the phyCORE-MPC565 module.

Instead, these signals are routed to pins on the Molex connectors (*refer to Figure 10*). The BDM signals are also available on the pin header connector X2 located at the front edge of the phyCORE module (*refer to Figure 2*). The footprint of X2 is designed for a 10-pin header with 2 mm pin spacing. The pin assignment is shown in *Figure 10*. Pin header X2 is not installed on the standard phyCORE-MPC565 module.

The phyCORE-MPC565 Development Board (PCM-991) contains a BDM signal converter circuitry, through which decoded BDM signals are routed to the connector at P3. This enables easy connection of the phyCORE-MPC565 (mounted on a Development Board) to a host-PC for start-up, download of user code and debugging.

Figure 10 shows the pin assignment for a 10-pin standard BDM interface connection.

phyCORE Pin	**Signal**	**BDM Connector**			**Signal**	**phyCORE Pin**
X1D61	VFLS0	1	o	o 2	/SRESET	X1D8
X1D59	GND	3	o	o 4	DSCK	X1C61
X1C62	GND	5	o	o 6	VFLS1	X1D62
X1C10	/HRESET	7	o	o 8	DSDI	X1C60
X	VCC	9	o	o 10	DSDO	X1D60

Figure 10: 10-Pin BDM Connector (X2) and Corresponding Pins on the phyCORE-Connector (X1)

X The supply voltage of the BDM converter depends on the type used. *For additional information, please refer to the accompanying data sheet of the converter*. Pin 9 at X2 is connected to the local power net VDD2V6.

9 CS8900A Ethernet Controller

Connection of the phyCORE-MPC565 to the world wide web or a local network is possible if the optional CS8900A 10-Mbit Ethernet Controller populates the module at U20.

This section only describes the functional characteristics of the CS8900A as implemented on the phyCORE-MPC565 A detailed description of the Ethernet controller itself can be found in the corresponding datasheet for the Crystal LAN Ethernet controller from Cirrus Logic.

9.1 Operational Modes

The Crystal LAN CS8900A Ethernet controller from Cirrus Logic offers various operational modes. The following sections explain the I/O mode of the Ethernet controller. The memory mode of the Ethernet controller is not supported.

9.1.1 CS8900A I/O Access Mode

The I/O mode is enabled following a reset of the module. This I/O mode allows the user to configure and operate the Ethernet controller through an eight address 16-bit port structure. Since the CS8900A starts in 8-bit mode after reset an access via the address/data bus must take place to switch into 16-bit mode before further configuration can be done. This switching can be accomplished by simple access to the device (via Chip Select).

Due to the internal big to little Endian conversion of the CS8900A – the controller was designed for X86 systems with ISA bus – the byte portions of the 16-bit data bus are connected in reversed order to the MPC565 data bus (D7 from the MPC565 to D0 on the CS8900A, D15_565 to D8_ETH). This signal reassignment is done with the help of 74LVC245 bus drivers populating U17 and U18. This feature allows for straight throughput of network data that is normally organised in big Endian byte ordering.

The phyCORE-MPC565 works in big Endian mode exclusively. Because of the byte swapping, the meaning of the CS8900A control register is byte-mirrored as well. The software driver has to take this detail into account for all control register access except for the data frame register.

9.2 Addressing the Ethernet Controllers

The System-EPLD at U2 generates the address and control signals for accessing the Ethernet controller CS8900A. The logic device handles the specific timing required by the CS8900A and generates the Chip Select as well as other control signals. According to the standard factory-default configuration of the logic device (the EPLD is in-system re-programmable) the Chip Select signal /CSLAN a well as the address signals LANA1 to LANA3 are generated from the MPC565 signals in the following fashion:

/CSLAN = /CS2 & A8
LANA1 = A19
LANA2 = A18
LANA3 = A17

Based on the address configuration shown above, the offset between the CS8900A register base address (/CSLAN) and all other internal register addresses is 0x1000. For example:

Register 0 address: 0x20800000
Register 1 address: 0x20801000
Register 2 address: 0x20802000
Register 3 address: 0x20803000

The address range for /CS2 must be configured to 16 MByte address range minimum. /CSLAN is active for the upper 8 MByte of the 16 MByte address range. The lower 8 MByte address range is responsible for accessing the second Flash (/CSFL2) memory bank. Take into account that the access speed of the address range /CSLAN is controlled by the System-EPLD and not by the MPC565 memory controller wait states. The required access speed corresponds to 7 wait states. *Refer also to section 6.2* to get an overview of a suggested runtime memory model with all applicable configuration and initialisation values.

9.3 Interrupt

The interrupt request output INTRQ0 (U20, pin 32) of the Ethernet controller CS8900A connects to the MPC565 interrupt input /IRQ1 indirectly. The System-EPLD at U2 configures the /IRQ1 routing according to the following logic equation:

/IRQ1 = /LANIRQ

/LANIRQ represents the inverted (via inverter U7D) high-active INTRQ0 signal from the CS8900A. /LANIRQ is also available at pin X1D37 on the phyCORE-connector. The IRQ assignment can be changed to another processor interrupt input. The EPLD code can changed or the /LANIRQ can be routed to a different MPC565 IRQ line externally.

9.4 Hardware Standby

To conserve power the CS8900A can be switched to hardware power-down mode. The /SLEEP input signal of the Ethernet controller must be set to low level in order to activate the power-down mode. The /SLEEP signal is connected to an I/O pin of the System-EPLD (U2). With the standard EPLD logic equation this signal is always inactive. To implement the Standby feature, modify or add the logic equation for the EPLD accordingly and re-program the device. *For details about the EPLD and re-programming instructions refer to section 7.*

9.5 MAC Address

In a computer network such as a “local area network” (LAN), the MAC (Media Access Control) address is a ***unique*** computer hardware number. For a connection to the Internet, a table is used to convert the assigned IP number to the hardware’s MAC address.

In order to guarantee that the MAC address is unique, all addresses are managed in a central location. PHYTEC has acquired a pool of MAC addresses. The MAC address of the phyCORE-MPC565 is located on the bar code sticker attached to the module. This number is a 12-position HEX value.

The MAC address has already been programmed into the Ethernet controller's EEPROM (U19), so that the MAC address is automatically loaded to the Ethernet controller following a reset (*refer to section 9.6*).

9.6 Ethernet EEPROM U19

The EEPROM (U19) connected to the Ethernet controller can be used to store configuration data that are automatically loaded into the CS8900A following a hardware-reset. The EEPROM can be programmed on-board via the Ethernet controller. *For detailed programming instructions please refer to the CS8900A data sheet.* The EEPROM is pre-programmed with the MAC address at time of delivery (*refer to section 9.5*).

9.7 10Base-T Interface

The phyCORE-MPC565 has been designed for use in 10Base-T networks exclusively. The 10Base-T interface with its signals including LANLED and LINKLED extends to phyCORE-connector X1. The AUI interface of the CS8900A is not available to the user. In order to connect the module to an existing 10Base-T network some external circuitry is required. It is important to note that the CS8900A variant implemented on the phyCORE-MPC565 operates with a 3 V supply voltage (CS8900A-Q3). *Please refer to the CS8900A-Q3 documentation for circuitry examples*.

If you are using the applicable Development Board for the phyCORE-MPC565 (part number PCM-991), the external circuitry mentioned above is already integrated on the board (*refer to section 11*). In addition, PHYTEC also offers an Ethernet adapter module (part number EAD-001-3V).

10 Real-Time Clock RTC-8564 (U13)

For real-time or time-driven applications, the phyCORE-MPC565 is equipped with an RTC-8564 Real-Time Clock at U13. This RTC device provides the following features:

- Serial input/output bus (I^2C), address 0xA2
- Power consumption

  Bus active (400 kHz): < 1 mA
  Bus inactive, CLKOUT inactive: < 1 µA
- Clock function with four year calendar
- Century bit for year 2000-compliance
- Universal timer with alarm and overflow indication
- 24-hour format
- Automatic word address incrementing
- Programmable alarm, timer and interrupt functions

If the phyCORE-MPC565 is equipped with a battery (VBAT), the Real-Time Clock runs independently of the board's power supply.

The Real-Time Clock is programmed via the I^2C bus (address 0xA2 / 0xA3) with the help of external I/O lines connected to SCL and SDA. To enable an on-board connection of the I²C signals to MDA15 and MDA14, a 100R resistor can be populated at spaces R60 and R61 (not pre-mounted in default configuration). Since the MPC565 is not equipped with an internal I^2C controller, the protocol must be emulated via software (*refer also to section 6.5)*

The Real-Time Clock also provides an interrupt output that extends to the /WAKEUP signal via jumper J26. An interrupt occurs in the event of a clock alarm, timer alarm, timer overflow and event counter alarm. It has to be cleared by software. With the interrupt function, the Real-Time Clock can be utilized in various applications. For example, closing jumper J26 allows time-controlled wake up of the phyCORE-MPC565, including start-up and operation from power-down mode.

If the RTC interrupt should be used as a software interrupt via a corresponding interrupt input of the processor, the signal /IRTC must be connected externally with a processor interrupt input. *For more information on the features of the RTC-8564, refer to the corresponding Data Sheet.*

Note:
After connection of the supply voltage, or after a reset, the Real-Time Clock generates **no** interrupt. The RTC must first be initialized (*see RTC Data Sheet for more information*).

11 phyCORE Development Board PCM-991

PHYTEC Development Boards are fully equipped with all mechanical and electrical components necessary for the speedy and secure start-up and subsequent communication to and programming of applicable PHYTEC Single Board Computer (SBC) modules. Development Boards are designed for evaluation, testing and prototyping of PHYTEC Single Board Computers in laboratory environments prior to their use in customer designed applications.

11.1 Concept of the phyCORE Development Board PCM-991

The phyCORE Development Board PCM-991 provides a flexible development platform enabling quick and easy start-up and subsequent programming of the phyCORE-MPC565 Single Board Computer module. The Development Board design allows easy connection of additional expansion boards featuring various functions that support fast and convenient prototyping and software evaluation.
This modular development platform concept is depicted in *Figure 11* and includes the following components:

- The actual **Development Board** (1), which offers all essential components and connectors for start-up including: a power socket enabling connection to an **external power adapter** (2) and **serial interfaces** (3) of the SBC module at DB-9 connectors. Two RS-232 Interfaces and two CAN interfaces are available. A RJ-45 connector (10) for Ethernet connection is also available. The DB-25 connector (4) is used for the debug link from the MPC565's BDM port to a host-PC printer port. This connection also supports reprogramming of the system EPLD (Lattice ispMACH4000 family) mounted on the phyCORE-MPC565.
- Most of the signals from the SBC module mounted on the Development Board extend to two receptacle connectors. The pin assignment of the **expansion bus** (11) depends on the pinout of the SBC module mounted on the Development Board.

- As the physical layout of the expansion bus is standardized across all applicable PHYTEC Development Boards, we are able to offer various **expansion boards** (5) that attach to the Development Board at the expansion bus connectors. These modular expansion boards offer **supplemental I/O functions** (6) as well as peripheral support devices for specific functions offered by the controller populating the **SBC module** (9) mounted on the Development Board.
- Most controller and on-board signals provided by the SBC module mounted on the Development Board are broken out 1:1 to the expansion board by means of its **patch field** (7). The required connections between SBC module / Development Board and the expansion board are made using **patch cables** (8) included with the expansion board.

Figure 11 illustrates the modular development platform concept:

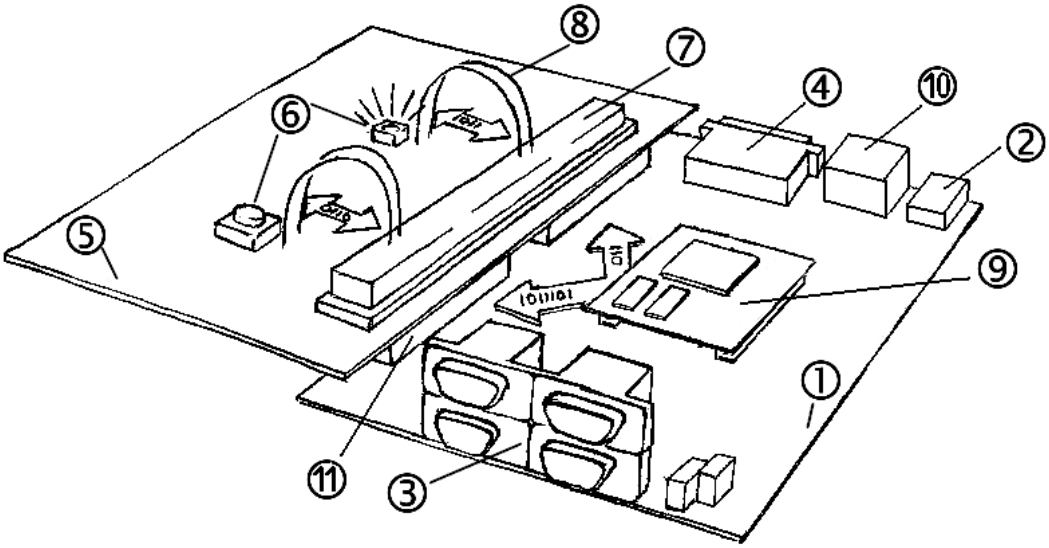


Figure 11: Modular Development and Expansion Board Concept with the phyCORE-MPC565

The following sections contain specific information relevant to the operation of the phyCORE-MPC565 mounted on the phyCORE Development Board PCM-991.

11.2 Development Board PCM-991 Overview

11.2.1 Connectors, Buttons, LED's

As shown in *Figure 12*, the following connectors are available on the phyCORE Development Board PCM-991:

X1-	phyCORE-connector enabling mounting of applicable phyCORE modules
X2-	mating receptacle for expansion board connectivity
X3	NEXUS debug port connector, 40-pin
X4	NEXUS debug port connector, 50-pin
X5	BDM header, 10-pin
X6	socket for +5 Volt power supply connectivity
X7	RJ45 Ethernet connector
X8	GND connector (for connection of GND signal of measuring devices such as an oscilloscope)
P1	dual DB-9 sockets for serial RS-232 interface connectivity
P2	dual DB-9 connectors for CAN interface connectivity
U8/U9	space for an optional silicon serial number chip
BAT1	receptacle for an optional battery
S1	Boot push button
S2	Reset push button
D1	green power LED, monitors +5 V
D2	green power LED, monitors +3V3V
D3	green power LED, monitors +2V6V
D6	red LED, monitors MPC565 I/O line MPIO0
D9	red LED, monitors the Reset line
D10	red LED, monitors BDM debug freeze status

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

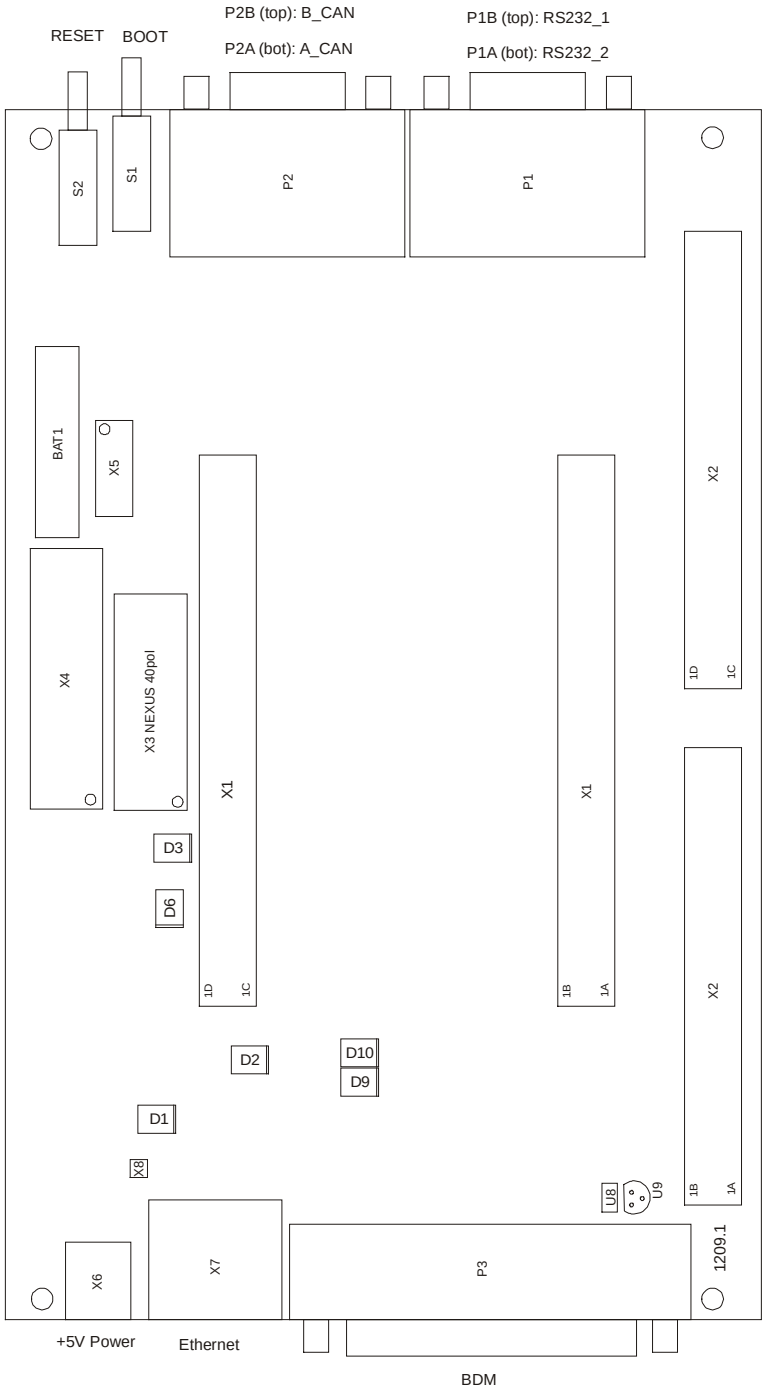


Figure 12: Location of Connectors, Buttons and LED's on the phyCORE Development Board PCM-991

11.2.2 Jumpers on the phyCORE Development Board PCM-991

Peripheral components of the phyCORE Development Board PCM-991 can be connected to the signals of the phyCORE-MPC565 by setting the applicable jumpers.

The Development Board's peripheral components are configured for use with the phyCORE-MPC565 by means of removable jumpers. If no jumpers are set, no signals are connected to the DB-9 connectors, the control and display units or the CAN transceivers. The Reset input on the phyCORE-MPC565 directly connects to the Reset button (S2). *Figure 13* illustrates the numbering of the jumper pads, while *Figure 14* indicates the location of the jumpers on the Development Board.

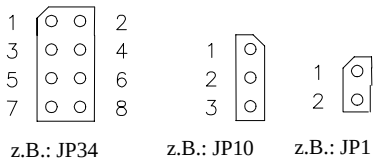


Figure 13: Numbering of Jumper Pads

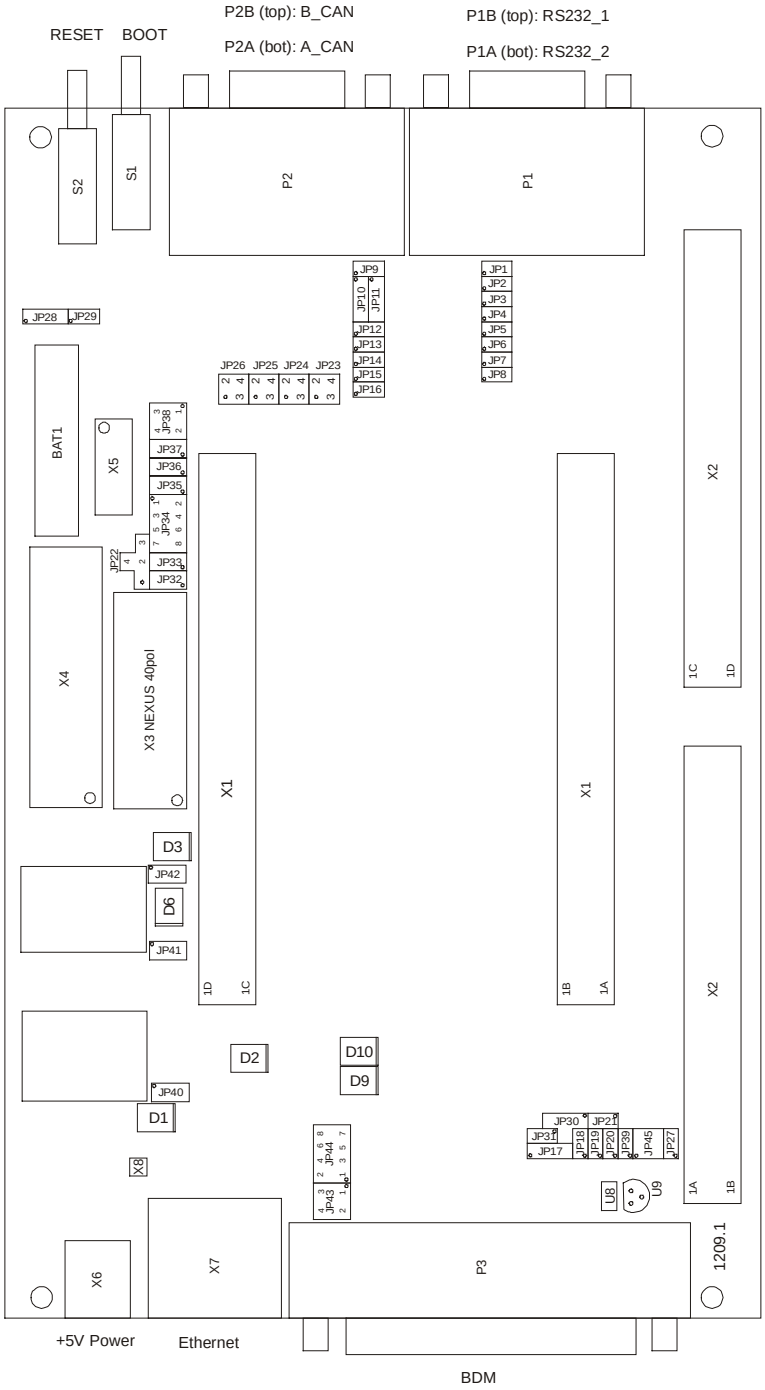


Figure 14: Location of the Jumpers (View of the Component Side)

Jumper	Default Setting	Description
JP1	closed	Pin 2 of DB-9 socket P1A connected with RS-232 signal TxD2 of the phyCORE-MPC565
JP2	open	Pin 9 of DB-9 socket P1A not connected
JP3	open	Pin 7 of DB-9 socket P1A not connected
JP4	open	Pin 4 of DB-9 socket P1A not connected
JP5	open	Pin 6 of DB-9 socket P1A not connected
JP6	open	Pin 8 of DB-9 socket P1A not connected
JP7	open	Pin 1 of DB-9 socket P1A not connected
JP8	closed	Pin 3 of DB-9 socket P1A connected with RS-232 signal RxD2 from the phyCORE-MPC565
JP9	closed	Pin 2 of DB-9 socket P1B connected with RS-232 signal TxD1 of the phyCORE-MPC565
JP10	open	Pin 9 of DB-9 socket P1B not connected
JP11	open	Pin 7 of DB-9 socket P1B not connected
JP12	open	Pin 4 of DB-9 socket P1B not connected
JP13	open	Pin 6 of DB-9 socket P1B not connected
JP14	open	Pin 8 of DB-9 socket P1B not connected
JP15	open	Pin 1 of DB-9 socket P1A not connected
JP16	closed	Pin 3 of DB-9 socket P1B connected with RS-232 signal RxD1 from the phyCORE-MPC565
JP17 1 + 2 2 + 3	 X	JP17 selects the memory that is used to boot the phyCORE-MPC565. JP17 is connected to the data line D20. During /HRESET D20 controls the FLEN bit in the Hard Reset Configuration Word. For proper operation, the jumper J33 on phyCORE-MPC565 must be removed (default): Boot from internal Flash memory. Boot from external Flash memory connected to /CS0. For the phyCORE standard configuration, /CS0 controls the Bust Mode Flash memory (U3/U4). Start-Up out of the second external asynchronous standard Flash does not work due to /CS2 controls it.
JP18	closed	I²C SCL Connects the MPC565 signal MDA14 to the local I²C bus clock signal SCL.
JP19	closed	I²C SDA Connects the MPC565 signal MDA15 to the local I²C bus data signal SDA.

Jumper	Default Setting	Description
JP20	closed	ZZ - Snooze Enable of burst-RAM: Connects the MPC565 signal MDA27 to the ZZ input of the target.
JP21	closed	LED D6 Connects the MPC565 signal MPIO0 to control the LED. Low level causes the LED to illuminate.
JP22		JP22 connects the push button S2 to different reset signals:
1 + 2		Connects /SRESET to push button S2.
2 + 4		Connects /RESIN to the push button S2.
2 + 3	X	Connects /HDRESET to push button S2.
JP23		Routing of the A_CANH signal (*refer to section 0*):
1 + 2	X	Connects A_CANH to pin 7 of P2A.
1 + 3		Connects A_CNTX0 to the opto-coupler U3.
2 + 4		Connects transceiver output CAN_H0 to P2A.
JP24		Routing of the A_CANL signal (*refer to section 0*):
1 + 2	X	Connects A_CANL to pin 2 of P2A.
1 + 3		Connects A_CNRX0 to the opto-coupler U4.
2 + 4		Connects transceiver output CAN_L0 to P2A.
JP25		Routing of the B_CANH signal (*refer to section 11.3.6*):
1 + 2	X	Connects B_CANH to pin 7 of P2B.
1 + 3		Connects B_CNTX0 to the opto-coupler U5.
2 + 4		Connects transceiver output CAN_H1 to P2B.
JP26		Routing of the B_CANL signal (*refer to section 0 or 11.3.6*):
1 + 2	X	Connects B_CANL to pin 2 of P2B.
1 + 3		Connects B_CNRX0 to the opto-coupler U6.
2 + 4		Connects transceiver output CAN_L1 to P2B.
JP27	open	Connects the MPC565 MPIO2 signal to the silicon serial number chip at U8/9 (*refer to section 11.3.10*).

Jumper	Default Setting	Description
JP28	open	CAN bus power selection (*refer to section 11.3.6*):
1 + 2		Optically isolated parts of the CAN bus circuitry are powered by a separate regulator at U7. U7 is supplied via voltage applied on pin 9 of P2A **or** P2B.
2 + 3		Optically isolated parts of the CAN bus circuitry are powered by the local non-isolated +5 V board voltage.
JP29	open	No connection between the isolated CAN bus ground VCAN- and the local board ground GND.
JP30		Selection of the BDM supply voltage (*refer to section 11.3.11*):
2 + 1		Connects +3V3 supply to the BDM circuits.
2 + 3	X	Connects +2V6 supply to the BDM circuits.
2 + 4		Connects +5 V supply to the BDM circuits.
JP31		Interface mode of the P3 connector:
open	X	BDM mode for debug operation.
closed		isp mode for reprogramming the phyCORE EPLD.
JP32		DSDI signal
JP33		DSCK signal
JP35		VFLS0 signal
JP36		VFLS0 signal
JP37		DSDO signal
open		Disconnected from the processor.
closed	X	Connected to the processor.
JP34		Reset connection to the target:
open		Disconnected from the target board.
1 + 2		/PORESET
3 + 4		/RESEIN
5 + 6	X	/HDRESET
7 + 8		/SRESET
JP38		Reset connection to the development host:
open		Disconnected from the host.
1 + 2	X	/HDRESET
3 + 4		/SRESET
JP39	open	Connects the MPC565 Flash enable signals B0EPEE and EPEE.

Jumper	Default Setting	Description
JP40	closed	5 V main supply voltage to the phyCORE-MPC565
JP41	closed	3.3 V main supply voltage to the phyCORE-MPC565
JP42	closed	2.6 V main supply voltage to the phyCORE-MPC565
JP43		Ethernet status LED's located at RJ-45 connector:
1 + 2	X	Connects LAN_LED signal to the RJ-45 connector.
3 + 4	X	Connects LINK_LED signal to the RJ-45 connector.
JP44		Routing of Ethernet signals:
1 + 2	X	Connects the ETHRXD- signal to transformer IC U18.
3 + 4	X	Connects the ETHRXD+ signal to transformer IC U18.
5 + 6	X	Connects the ETHTXD- signal to transformer IC U18.
7 + 8	X	Connects the ETHTXD+ signal to transformer IC U18.
JP45		Enables Flash programming of the MPC565's internal Flash memory:
1 + 2	X	Enables EPEE
3 + 4	X	Enables B0EPEE

Table 10: Development Board Jumper Overview

Figure 15 shows the factory default jumper settings for operation of the phyCORE Development Board PCM-991 with the standard phyCORE-MPC565. Jumper settings for other functional configurations of the phyCORE-MPC565 module mounted on the Development Board are described in *section 11.3*.

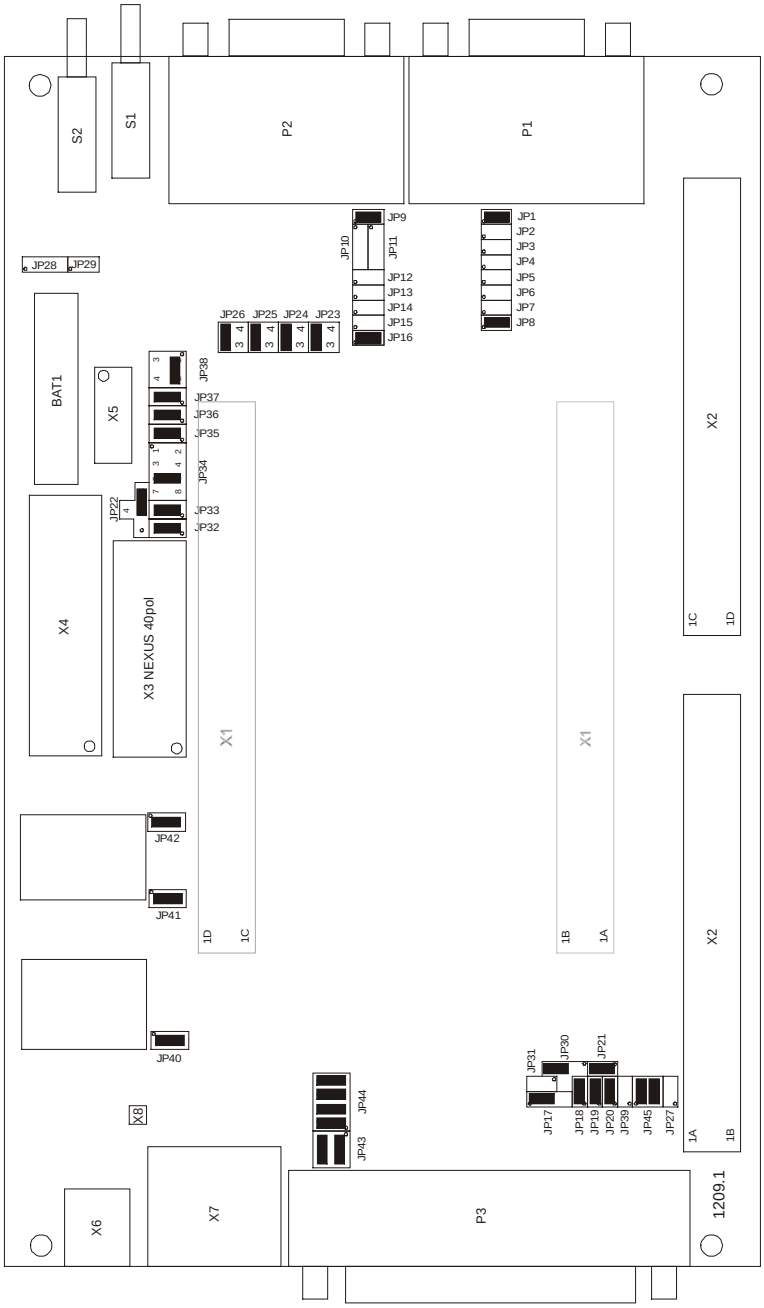


Figure 15: Default Jumper Settings of the phyCORE Development Board PCM-991 with phyCORE-MPC565

11.3 Functional Components on the phyCORE Development Board PCM-991

This section describes the functional components of the phyCORE Development Board PCM-991 supported by the phyCORE-MPC565 and appropriate jumper settings to activate these components. Depending on the specific configuration of the phyCORE-MPC565 module, alternative jumper settings can be used. These jumper settings are different from the factory default settings as shown in *Figure 15* and enable alternative or additional functions on the phyCORE Development Board PCM-991 depending on user needs.

11.3.1 Power Supply at X1

Caution:
Do not use a laboratory adapter to supply power to the Development Board! Power spikes during power-on could destroy the phyCORE module mounted on the Development Board! Do not change modules or jumper settings while the Development Board is supplied with power!

Permissible input voltage: +5 VDC regulated.

The required current load capacity of the power supply depends on the specific configuration of the phyCORE-MPC565 mounted on the Development Board as well as whether an optional expansion board is connected to the Development Board. An adapter with a minimum supply of 1000 mA is recommended.

Jumper	Setting	Description
JP40	closed	3.3 V primary main supply voltage to the phyCORE-MPC565
JP41	closed	5 V as secondary main supply voltage to the phyCORE-MPC565
JP42	closed	2.6 V as third main supply voltage to the phyCORE-MPC565

Table 11: JP9, JP16 Configuration of the Main Supply Voltages VCC1, VCC2 and VCC3

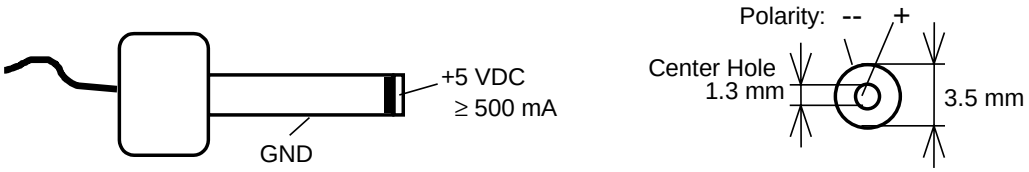


Figure 16: Connecting the Supply Voltage at X1

Caution:
Do not remove any of these jumpers and power the board. One missing main supply voltage can destroy the module.

11.3.2 First Serial Interface at Socket P1B

Socket P1B is the upper socket of the double DB-9 connector at P1. P1B is connected via jumpers to the second serial interface of the phyCORE-MPC565. The following description is based on a module configuration that utilizes the on-board RS-232 transceivers for the second serial interface.

Jumper	Setting	Description
JP9	closed	Pin 2 of DB-9 socket P1B connected with RS-232 signal TxD1 of the phyCORE-MPC565
JP10	open	Pin 9 of DB-9 socket P1B not connected
JP11	open	Pin 7 of DB-9 socket P1B not connected
JP12	open	Pin 4 of DB-9 socket P1B not connected
JP13	open	Pin 6 of DB-9 socket P1B not connected
JP14	open	Pin 8 of DB-9 socket P1B not connected
JP15	open	Pin 1 of DB-9 socket P1B not connected
JP16	closed	Pin 3 of DB-9 socket P1B connected with RS-232 signal RxD1 from the phyCORE-MPC565

Table 12: Jumper Configuration for the First RS-232 Interface

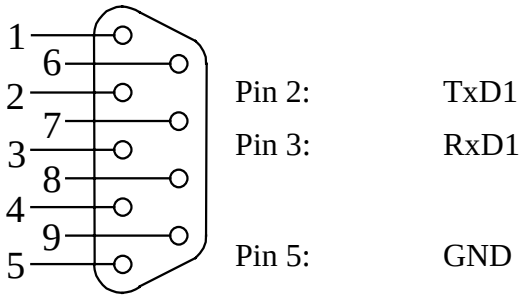


Figure 17: Pin Assignment of the DB-9 Socket P1B as First RS-232 (Front View)

Caution:
Do not install any of the remaining jumpers without transforming the corresponding signals to RS-232 voltage levels. If an RS-232 cable is connected to P1B, the voltage level on the RS-232 lines could destroy the phyCORE-MPC565.

11.3.3 Second Serial Interface at Socket P1A

Socket P1A is the lower socket of the double DB-9 connector at P1. P1A is connected via jumpers to the second serial interface of the phyCORE-MPC565.

Jumper	Setting	Description
JP1	closed	Pin 2 of DB-9 socket P1A connected with RS-232 signal TxD2 of the phyCORE-MPC565
JP2	open	Pin 9 of DB-9 socket P1A not connected
JP3	open	Pin 7 of DB-9 socket P1A not connected
JP4	open	Pin 4 of DB-9 socket P1A not connected
JP5	open	Pin 6 of DB-9 socket P1A not connected
JP6	open	Pin 8 of DB-9 socket P1A not connected
JP7	open	Pin 1 of DB-9 socket P1A not connected
JP8	closed	Pin 3 of DB-9 socket P1A connected with RS-232 signal RxD2 from the phyCORE-MPC565

Table 13: Jumper Configuration for the Second RS-232 Interface

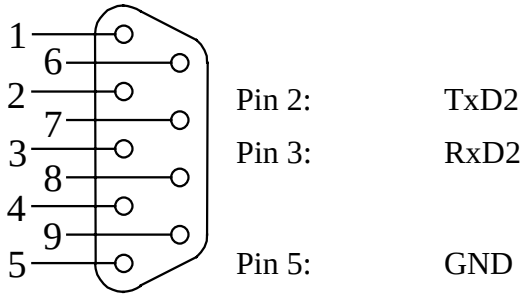


Figure 18: Pin Assignment of the DB-9 Socket P1A as Second RS-232 (Front View)

Caution:
Do not install any of the remaining jumpers without transforming the corresponding signals to RS-232 voltage levels. If an RS-232 cable is connected to P1A, the voltage level on the RS-232 lines could destroy the phyCORE-MPC565.

11.3.4 Power Supply to External Devices via Socket P1B

The Development Board PCM-991 can be populated by additional components that provide a 5 V supply voltage at pin 6 of DB-9 socket P1B. This allows for easy and secure supply of external devices connected to P1B. This power supply option supports connectivity to analog and digital modems. Such modems enable communication of the phyCORE-MPC565 over the Internet or a direct dial connection.

The components at U19 and U20 guarantee electronic protection against over-voltage and excessive current draw at pin 6 of P1B; in particular:

- Load detection and controlled voltage supply switch-on:
  In order to ensure clear detection of the switch-on condition, the connected device should cause a current draw of at least 10 mA at pin 6. The controlled voltage supply switch-on prevents voltage drop off on the Development Board PCM-991.
- Overvoltage Protection:
  If the voltage at pin 6 exceeds the limiting value that can be provided by the phyCORE Development Board PCM-991, the voltage at pin 6 will be switched off immediately. This prevents damage to the phyCORE Development Board PCM-991 as well as connected modules and expansion boards.
- Overload Protection:
  If the current draw at pin 6 exceeds the limiting value of approximately 150 mA, the voltage at pin 6 will be switched off immediately. This prevents damage to the phyCORE Development Board PCM-991 and its power adapter caused by current overload.

This configuration option provides the following possibility:

Jumper	Setting	Description
JP11	2 + 3	Electronically protected 5 V at pin 6 for supply of external devices connected to P1A

Table 14: JP11 Power Supply to External Devices Connected to P1B on the Development Board

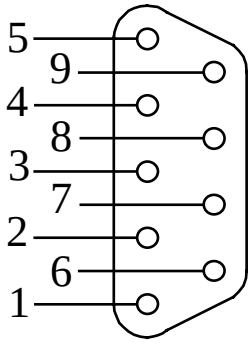
11.3.5 First CAN Interface at Plug P2A

Plug P2A is the lower plug of the double DB-9 connector at P2. P2A is connected to the first CAN interface (A_CAN) of the phyCORE-MPC565 via jumpers. Depending on the configuration of the CAN transceivers and their power supply, the following three configurations are possible:

1. CAN transceiver on the phyCORE-MPC565 is populated and the CAN signals from the module extend directly to plug P2A.

Jumper	Setting	Description
JP24	1 + 2	Pin 2 of the DB-9 plug P2A is connected to A_CANL from on-board transceiver on the phyCORE module
JP23	1 + 2	Pin 7 of the DB-9 plug P2A is connected to A_CANH from on-board transceiver on the phyCORE module

Table 15: Jumper Configuration for CAN Plug P2A using the CAN Transceiver on the phyCORE-MPC565



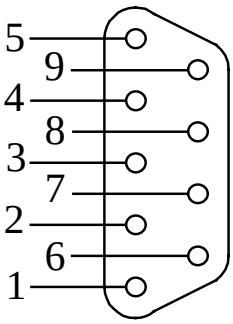
Pin 3:	GND	(Development Board Ground)
Pin 7:	CAN-H0	(not galvanically separated)
Pin 2:	CAN-L0	(not galvanically separated)
Pin 6:	GND	(Development Board Ground)

Figure 19: Pin Assignment of the DB-9 Plug P2A (CAN Transceiver on phyCORE-MPC565, Front View)

2. No CAN transceiver is populating the phyCORE-MPC565 and Jumper J6 is closed at 1+2 and 3+4; CAN signals generated by the CAN transceiver (U1) on the Development Board extending to connector P2A **without galvanic separation:**

Jumper	Setting	Description
JP24	2 + 4 1 + 3[1]	Pin 2 of the DB-9 plug P2A is connected to CAN_L0 from on-board transceiver on the Development Board PCM-991. Output at opto-coupler U4 on the phyCORE Development Board PCM-991 connected with A_CNRX0 of the phyCORE-MPC565.
JP23	2 + 4 1 + 3[1]	Pin 7 of the DB-9 plug P2A is connected to CAN_H0 from on-board transceiver on the Development Board PCM-991. Input at opto-coupler U3 on the phyCORE Development Board PCM-991 connected with A_CNTX0 of the phyCORE-MPC565.
JP28	2 + 3	Supply voltage to CAN transceiver and opto-coupler on the phyCORE Development Board PCM-991
JP29	1 + 2	GND potential at CAN transceiver and opto-coupler on the phyCORE Development Board PCM-991

Table 16: Jumper Configuration for CAN Plug P2A using the CAN Transceiver on the Development Board PCM-991



Pin 3: GND (Development Board Ground)
Pin 7: CAN-H0 (not galvanically separated)
Pin 2: CAN-L0 (not galvanically separated)
Pin 6: GND (Development Board Ground

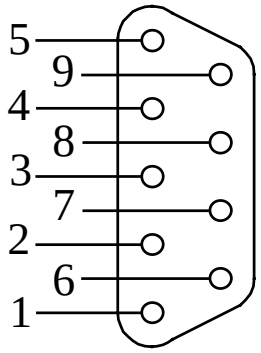
Figure 20: Pin Assignment of the DB-9 Plug P2A (CAN Transceiver on Development Board)

[1]: Please make sure the CAN transceiver on the phyCORE-MPC565 is not populated and Jumper J6 is closed at 1+2 and 3+4.

3. The CAN transceiver is not populated on the phyCORE-MPC565 and Jumpers J6 is closed at 1+2 and 3+4; CAN signals generated by the CAN transceiver (U1) on the Development Board extend to connector P2A **with galvanic separation.** This configuration requires connection of an external CAN supply voltage of 7 to 13 V. The external power supply must be **only** connected to either P2A **or** P2B.

Jumper	Setting	Description
JP24	2 + 4	Pin 2 of the DB-9 plug P2A is connected to CAN_L0 from on-board transceiver on the Development Board PCM-991.
	1 + 3[1]	Output at opto-coupler U4 on the phyCORE Development Board PCM-991 connected with A_CNRX0 of the phyCORE-MPC565.
JP23	2 + 4	Pin 7 of the DB-9 plug P2A is connected to CAN_H0 from on-board transceiver on the Development Board PCM-991.
	1 + 3[1]	Input at opto-coupler U3 on the phyCORE Development Board PCM-991 connected with A_CNTX0 of the phyCORE-MPC565.
JP28	1 + 2	Supply voltage for on-board voltage regulator from pin 9 of DB-9 plug P2A or P2B
JP29	open	CAN transceiver and opto-coupler on the Development Board disconnected from local GND potential

Table 17: Jumper Configuration for CAN Plug P2A using the CAN Transceiver on the Development Board with Galvanic Separation



Pin 9: VCAN+

Pin 3: VCAN-
Pin 7: CAN-H0 (galvanically separated)
Pin 2: CAN-L0 (galvanically separated)
Pin 6: VCAN-

Figure 21: Pin Assignment of the DB-9 Plug P2A (CAN Transceiver on Development Board with Galvanic Separation)

[1]: Please make sure the CAN transceiver on the phyCORE-MPC565 is not populated and Jumper J6 is closed at 1+2 and 3+4.

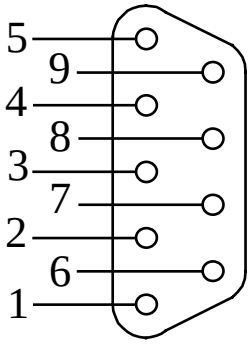
11.3.6 Second CAN Interface at Plug P2B

Plug P2B is the upper plug of the double DB-9 connector at P2. P2B is connected to the second CAN interface (B_CAN) of the phyCORE-MPC565 via jumpers. Depending on the configuration of the CAN transceivers and their power supply, the following three configurations are possible:

1. CAN transceiver populating the phyCORE-MPC565 is populated and the CAN signals from the module extend directly to plug P2B.

Jumper	Setting	Description
JP26	1 + 2	Pin 2 of the DB-9 plug P2B is connected to B_CANL from on-board transceiver on the phyCORE module
JP25	1 + 2	Pin 7 of the DB-9 plug P2B is connected to B_CANH from on-board transceiver on the phyCORE module

Table 18: Jumper Configuration for CAN Plug P2B Using the CAN Transceiver on the phyCORE-MPC565



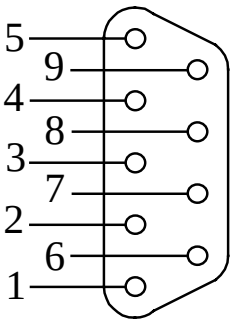
Pin 3: GND (Development Board Ground)
Pin 7: CAN-H1 (not galvanically separated)
Pin 2: CAN-L1 (not galvanically separated)
Pin 6: GND (Development Board Ground)

Figure 22: Pin Assignment of the DB-9 Plug P2B (CAN Transceiver on phyCORE-MPC565, Front View)

2. No CAN transceiver is populating the phyCORE-MPC565 and Jumpers J4 is closed at 1+2 and 3+4; CAN signals generated by the CAN transceiver (U2) on the Development Board extending to connector P2B **without galvanic separation:**

Jumper	Setting	Description
JP26	2 + 4 1 + 3[1]	Pin 2 of the DB-9 plug P2B is connected to CAN_L1 from on-board transceiver on the Development Board PCM-991. Output at opto-coupler U6 on the phyCORE Development Board PCM-991 connected with B_CNRX0 of the phyCORE-MPC565.
JP25	2 + 4 1 + 3[1]	Pin 7 of the DB-9 plug P2B is connected to CAN_H1 from on-board transceiver on the Development Board PCM-991. Input at opto-coupler U5 on the phyCORE Development Board PCM-991 connected with B_CNTX0 of the phyCORE-MPC565.
JP28	2 + 3	Supply voltage to CAN transceiver and opto-coupler on the phyCORE Development Board PCM-991
JP29	1 + 2	GND potential at CAN transceiver and opto-coupler on the phyCORE Development Board PCM-991

Table 19: Jumper Configuration for CAN Plug P2B using the CAN Transceiver on the Development Board PCM-991



Pin 3: GND (Development Board Ground)
Pin 7: CAN-H1 (not galvanically separated)
Pin 2: CAN-L1 (not galvanically separated)
Pin 6: GND (Development Board Ground

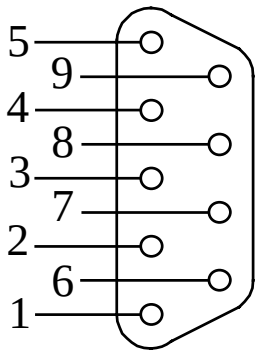
Figure 23: Pin Assignment of the DB-9 Plug P2B (CAN Transceiver on Development Board)

[1]: Please make sure the CAN transceiver on the phyCORE-MPC565 is not populated and Jumper J4 is closed at 1+2 and 3+4.

3. The CAN transceiver is not populated on the phyCORE-MPC565 and Jumper J4 is closed at 1+2 and 3+4; CAN signals generated by the CAN transceiver (U2) on the Development Board extend to connector P2B **with galvanic separation.** This configuration requires connection of an external CAN supply voltage of 7 to 13 V. The external power supply must be **only** connected to either P2A **or** P2B.

Jumper	Setting	Description
JP26	2 + 4	Pin 2 of the DB-9 plug P2B is connected to CAN_L1 from on-board transceiver on the Development Board PCM-991.
	1 + 3[1]	Output at opto-coupler U6 on the phyCORE Development Board PCM-991 connected with B_CNRX0 of the phyCORE-MPC565.
JP25	2 + 4	Pin 7 of the DB-9 plug P2B is connected to CAN_H1 from on-board transceiver on the Development Board PCM-991.
	1 + 3[1]	Input at opto-coupler U5 on the phyCORE Development Board PCM-991 connected with B_CNTX0 of the phyCORE-MPC565.
JP28	1 + 2	Supply voltage for on-board voltage regulator from pin 9 of DB-9 plug P2B or P2A
JP29	open	CAN transceiver and opto-coupler on the Development Board disconnected from local GND potential

Table 20: Jumper Configuration for CAN Plug P2B using the CAN Transceiver on the Development Board with Galvanic Separation



Pin 9: VCAN+

Pin 3: VCAN-
Pin 7: CAN-H1 (galvanically separated)
Pin 2: CAN-L1 (galvanically separated)
Pin 6: VCAN-

Figure 24: Pin Assignment of the DB-9 Plug P2B (CAN Transceiver on Development Board with Galvanic Separation)

[1]: Please make sure the CAN transceiver on the phyCORE-MPC565 is not populated and Jumper J4 is closed at 1+2 and 3+4.

11.3.7 Programmable LED D6

The phyCORE Development Board PCM-991 offers a programmable LED at D6 for user implementations. This LED can be connected to port pin MPIO0 of the phyCORE-MPC565 which is available via signal GPIO0 (JP21 = closed). A low-level at port pin MPIO0 causes the LED to illuminate, LED D6 remains off when writing a high-level to MPIO0.

Jumper	Setting	Description
JP21	closed	Port pin MPIO0 (GPIO0) of the MPC565 controls LED D6 on the Development Board

Table 21: JP21 Configuration of the Programmable LED D6

11.3.8 Pin Assignment Summary of the phyCORE, the Expansion Bus and the Patch Field

As described in *section 11.1*, most signals from the phyCORE-MPC565 extend to the expansion bus connector X2 on the Development Board. These signals, in turn, are routed in a similar manner to the patch field on an optional expansion board that mounts to the Development Board at X2.

Please note that, depending on the design and size of the expansion board, only a portion of the entire patch field is utilized under certain circumstances. When this is the case, certain signals described in the following section will not be available on the expansion board. However, the pin assignment scheme remains consistent.

A two dimensional numbering matrix similar to the one used for the pin layout of the phyCORE-connector is provided to identify signals on the expansion bus connector (X2 on the Development Board) as well as the patch field.

However, the numbering scheme for expansion bus connector and patch field matrices differs from that of the phyCORE-connector, as shown in the following two figures:

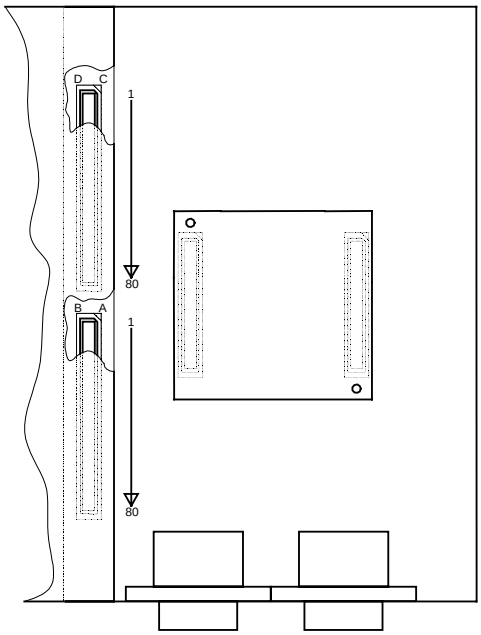


Figure 25: Pin Assignment Scheme of the Expansion Bus

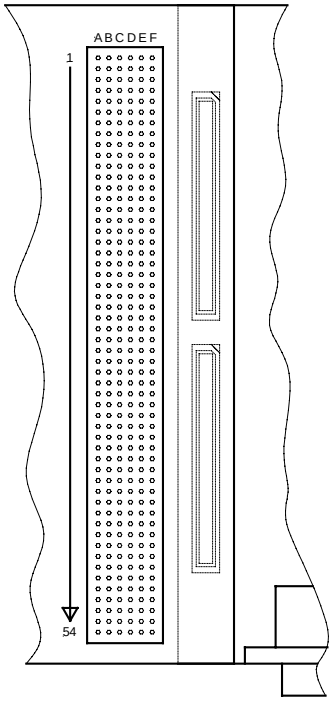


Figure 26: Pin Assignment Scheme of the Patch Field

The pin assignment on the phyCORE-MPC565, in conjunction with the expansion bus (X2) on the Development Board and the patch field on an expansion board, is as follows:

phyCORE-MPC565		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
1A	EXTCLK	BUS0	1A	BUS0	28A
3A	/IRQ3	BUS3	3A	BUS3	28B
4A	/IRQ0	BUS5	4A	BUS5	29A
5A	/CS2	BUS6	5A	BUS6	29E
6A	/CS1	BUS8	6A	BUS8	29D
8A	/WE3	BUS11	8A	BUS11	30E
9A	A30	BUS13	9A	BUS13	30D
10A	A29	BUS14	10A	BUS14	30F
11A	A27	BUS16	11A	BUS16	31E
13A	A24	BUS19	13A	BUS19	32A
14A	A22	BUS21	14A	BUS21	32E
15A	A21	BUS22	15A	BUS22	32B
16A	A19	BUS24	16A	BUS24	33A
18A	A16	BUS27	18A	BUS27	33B
24A	A14	BUS37	24A	BUS37	35D
25A	A13	BUS38	25A	BUS38	35F
26A	A11	BUS40	26A	BUS40	36E
28A	A8	BUS43	28A	BUS43	37A
34A	/TA	BUS53	34A	BUS53	39A
35A	/TEA	BUS54	35A	BUS54	39E
36A	/BB	BUS56	36A	BUS56	39D
38A	D14	BUS59	19A	BUS29	34A
39A	D12	BUS61	20B	BUS31	34B
40A	D11	BUS62	21A	BUS32	34D
41A	D9	BUS64	22B	BUS34	35A
43A	D6	BUS67	29A	BUS45	37E
44A	D4	BUS69	30B	BUS47	37F
45A	D3	BUS70	31A	BUS48	38A
46A	D1	BUS72	32B	BUS50	38E
48A	PLDIO1	BUS75	38A	BUS59	40E
49A	PLDIO3	BUS77	39A	BUS61	40D
50A	/FLIRQ	BUS78	40A	BUS62	40F
51A	TSIZ0	BUS80	41A	BUS64	41E
53A	/TS	BUS83	43A	BUS67	42A
54A	RDNWR	BUS85	44A	BUS69	42E
55A	/BDIP	BUS86	45A	BUS70	42B
56A	/BURST	BUS88	46A	BUS72	43A

phyCORE-MPC565		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
58A	/BI//STS	BUS91	48A	BUS75	43B
59A	CANSTB	BUS93	49A	BUS77	44A
60A	/PWRON	BUS94	50A	BUS78	44E
61A	/WAKEUP	BUS96	51A	BUS80	44D
63A	PLDTDO	BUS99	53A	BUS83	45E
64A	PLDTDI	BUS101	54A	BUS85	45D
65A	PLDIO5	BUS102	55A	BUS86	45F
66A	PLDIO7	BUS104	56A	BUS88	46E
68A	PLDIO9	BUS107	58A	BUS91	47A
69A	C_T2CLK	BUS109	59A	BUS93	47E
80A	B_TPU15	BUS126	60A	BUS94	47B
81A	B_TPU13	BUS128	61A	BUS96	48A
83A	B_TPU11	BUS131	63A	BUS99	48B
84A	B_TPU9	BUS133	64A	BUS101	49A
85A	B_TPU7	BUS134	65A	BUS102	49E
86A	B_TPU5	BUS136	66A	BUS104	49D
88A	B_TPU3	BUS139	68A	BUS107	50E
89A	B_TPU1	BUS141	69A	BUS109	50D
90A	B_T2CLK	BUS142	70A	BUS110	50F
91A	A_TPU15	BUS144	71A	BUS112	51E
93A	A_TPU13	BUS147	73A	BUS115	52A
94A	A_TPU11	BUS149	74A	BUS117	52E
95A	A_TPU9	BUS150	75A	BUS118	52B
96A	A_TPU7	BUS152	76A	BUS120	53A
98A	A_TPU5	BUS155	78A	BUS123	53B
99A	A_TPU3	BUS157	79A	BUS125	54A
100A	A_TPU1	BUS158	80A	BUS126	54E
1B	CLKOUT	BUS1	1B	BUS1	28C
2B	/IRQ1	BUS2	2B	BUS2	28E
3B	/IRQ2	BUS4	3B	BUS4	28F
5B	/CS3	BUS7	5B	BUS7	29B
6B	/CS0	BUS9	6B	BUS9	29F
7B	/OE	BUS10	7B	BUS10	30A
8B	A31	BUS12	8B	BUS12	30B
10B	A28	BUS15	10B	BUS15	31A
11B	A26	BUS17	11B	BUS17	31B
12B	A25	BUS18	12B	BUS18	31F
13B	A23	BUS20	13B	BUS20	32C
15B	A20	BUS23	15B	BUS23	32F
16B	A18	BUS25	16B	BUS25	33C
17B	A17	BUS26	17B	BUS26	33E

phyCORE-MPC565		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
23B	A15	BUS36	23B	BUS36	35B
25B	A12	BUS39	25B	BUS39	36A
26B	A10	BUS41	26B	BUS41	36B
27B	A9	BUS42	27B	BUS42	36F
33B	/WE2	BUS52	33B	BUS52	38F
35B	/BG	BUS55	35B	BUS55	39B
36B	/BR	BUS57	36B	BUS57	39F
37B	D15	BUS58	18B	BUS28	33F
38B	D13	BUS60	20A	BUS30	34E
40B	D10	BUS63	21B	BUS33	34F
41B	D8	BUS65	23A	BUS35	35E
42B	D7	BUS66	28B	BUS44	37C
43B	D5	BUS68	30A	BUS46	37B
45B	D2	BUS71	31B	BUS49	38C
46B	D0	BUS73	33A	BUS51	38B
47B	PLDIO0	BUS74	37B	BUS58	40A
48B	PLDIO2	BUS76	38B	BUS60	40B
50B	PLDIO4	BUS79	40B	BUS63	41A
51B	TSIZ1	BUS81	41B	BUS65	41B
52B	/WE1	BUS82	42B	BUS66	41F
53B	/WE0	BUS84	43B	BUS68	42C
55B	/IRQ4	BUS87	45B	BUS71	42F
56B	/IRQ5	BUS89	46B	BUS73	43C
57B	/IRQ6	BUS90	47B	BUS74	43E
58B	/IRQ7	BUS92	48B	BUS76	43F
60B	VDDGOOD	BUS95	50B	BUS79	44B
61B	/VDDGOOD	BUS97	51B	BUS81	44F
62B	PLDTMS	BUS98	52B	BUS82	45A
63B	PLDTCK	BUS100	53B	BUS84	45B
65B	PLDIO6	BUS103	55B	BUS87	46A
66B	PLDIO8	BUS105	56B	BUS89	46B
67B	PLDIO10	BUS106	57B	BUS90	46F
68B	ZZ	BUS108	58B	BUS92	47C
80B	B_TPU14	BUS127	60B	BUS95	47F
81B	B_TPU12	BUS129	61B	BUS97	48C
82B	B_TPU10	BUS130	62B	BUS98	48E
83B	B_TPU8	BUS132	63B	BUS100	48F
85B	B_TPU6	BUS135	65B	BUS103	49B
86B	B_TPU4	BUS137	66B	BUS105	49F
87B	B_TPU2	BUS138	67B	BUS106	50A
88B	B_TPU0	BUS140	68B	BUS108	50B

phyCORE-MPC565		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
90B	A_T2CLK	BUS143	70B	BUS111	51A
91B	A_TPU14	BUS145	71B	BUS113	51B
92B	A_TPU12	BUS146	72B	BUS114	51F
93B	A_TPU10	BUS148	73B	BUS116	52C
95B	A_TPU8	BUS151	75B	BUS119	52F
96B	A_TPU6	BUS153	76B	BUS121	53C
97B	A_TPU4	BUS154	77B	BUS122	53E
98B	A_TPU2	BUS156	78B	BUS124	53F
100B	A_TPU0	BUS159	80B	BUS127	54B
6C	VBAT	VBAT	6C	VBAT	2B
8C	PWRGOOD	PFO	8C	PFO	3E
9C	TEXP//RSTCNF	BOOT//BOOT	9C	BOOT//BOOT	3B
10C	/HRESET	/HDRESET	10C	/RESET	3D
11C	/PORESET	/PORESET	11C	/RESOUT	4E
13C	MPIO1	GPIO2	13C	GPIO2	4F
14C	MPIO3	GPIO4	14C	GPIO4	5C
15C	MPIO5	GPIO5	15C	GPIO5	5E
16C	MPIO7	GPIO7	16C	GPIO7	5F
18C	B_CANH	GPIO10	18C	GPIO10	6E
19C	A_RXD2TTL	GPIO12	19C	GPIO12	6F
20C	A_TXD2TTL	GPIO13	20C	GPIO13	7A
21C	RXD2	GPIO15	21C	GPIO15	7B
23C	TXD2	GPIO18	23C	GPIO18	8A
24C	A_QGPIO1	GPIO20	24C	GPIO20	8B
25C	A_QGPIO3	GPIO21	25C	GPIO21	8D
26C	A_QGPIO5	GPIO23	26C	GPIO23	9A
28C	ECK	GPIO26	28C	GPIO26	9F
29C	B_QGPIO1	GPIO28	29C	GPIO28	10C
30C	B_QGPIO3	GPIO29	30C	GPIO29	10E
31C	SCL	GPIO31	31C	GPIO31	10F
38C	B_QGPIO5	GPIO42	33C	GPIO34	11E
39C	B_QGPO1	GPIO44	34C	GPIO36	11F
40C	B_QGPI1	GPIO45	35C	GPIO37	12A
41C	SGPIOC7	GPIO47	36C	GPIO39	12B
43C	MPIO9	GPIO50	38C	GPIO42	13A
44C	MPIO11	GPIO52	39C	GPIO44	13B
45C	MPIO13	GPIO53	40C	GPIO45	13D
46C	MPIO15	GPIO55	41C	GPIO47	14A
48C	MDA11	GPIO58	43C	GPIO50	14F
49C	MDA13	GPIO60	44C	GPIO52	15C
50C	MDA15	GPIO61	45C	GPIO53	15E

phyCORE-MPC565		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
51C	MDA27	GPIO63	46C	GPIO55	15F
53C	MDA29	GPIO66	48C	GPIO58	16E
54C	MDA31	GPIO68	49C	GPIO60	16F
55C	MPWM1	GPIO69	50C	GPIO61	17A
56C	MPWM3	GPIO71	51C	GPIO63	17B
58C	MPWM17	GPIO74	53C	GPIO66	18A
59C	MPWM19	GPIO76	54C	GPIO68	18B
70C	/RSTI	GPIO93	55C	GPIO69	18D
71C	EPEE	GPIO95	56C	GPIO71	19A
73C	ETRIG1	GPIO98	58C	GPIO74	19F
79C	B_AN78	GPIO108	59C	GPIO76	20C
80C	B_AN76	GPIO109	60C	GPIO77	20E
81C	B_AN74	GPIO111	61C	GPIO79	20F
83C	B_AN72	GPIO114	63C	GPIO82	21E
84C	B_AN70	GPIO116	64C	GPIO84	21F
85C	B_AN68	GPIO117	65C	GPIO85	22A
86C	B_AN66	GPIO119	66C	GPIO87	22B
88C	B_AN64	GPIO122	68C	GPIO90	23A
89C	A_AN58	GPIO124	69C	GPIO92	23B
90C	A_AN56	GPIO125	70C	GPIO93	23D
91C	A_AN54	GPIO127	71C	GPIO95	24A
93C	A_AN52	GPIO130	73C	GPIO98	24F
94C	A_AN50	GPIO132	74C	GPIO100	25C
95C	A_AN48	GPIO133	75C	GPIO101	25E
96C	A_AN46	GPIO135	76C	GPIO103	25F
98C	A_AN44	GPIO138	78C	GPIO106	26E
99C	ALTREF	GPIO140	79C	GPIO108	26F
100C	VDDA5V	GPIO141	80C	GPIO109	27A
6D	VPD	VPD	6D	VPD	2D
7D	/PFI	PFI	7D	PFI	2F
8D	/SRESET	/SRESET	8D	WDI	3A
10D	/HRESIN	/RESIN	10D	/RESIN	3F
11D	MPIO0	GPIO0	11D	GPIO0	4A
12D	MPIO2	GPIO1	12D	GPIO1	4B
13D	MPIO4	GPIO3	13D	GPIO3	5A
15D	MPIO6	GPIO6	15D	GPIO6	5B
16D	A_RXD1TTL	GPIO8	16D	GPIO8	6A
17D	A_TXD1TTL	GPIO9	17D	GPIO9	6C
18D	B_CANL	GPIO11	18D	GPIO11	6B
20D	A_CANL	GPIO14	20D	GPIO14	7E
21D	A_CANH	GPIO16	21D	GPIO16	7D

phyCORE-MPC565		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
22D	RXD1	GPIO17	22D	GPIO17	7F
23D	TXD1	GPIO19	23D	GPIO19	8E
25D	A_QGPIO0	GPIO22	25D	GPIO22	8F
26D	A_QGPIO2	GPIO24	26D	GPIO24	9E
27D	A_QGPIO4	GPIO25	27D	GPIO25	9B
28D	A_QGPIO6	GPIO27	28D	GPIO27	10A
30D	B_QGPIO0	GPIO30	30D	GPIO30	10B
31D	B_QGPIO2	GPIO32	31D	GPIO32	11A
32D	SDA	GPIO33	32D	GPIO33	11C
33D	/RTCIRQ	GPIO35	33D	GPIO35	11B
37D	/LANIRQ	GPIO41	35D	GPIO38	12E
38D	B_QGPIO4	GPIO43	36D	GPIO40	12D
40D	B_QGPIO6	GPIO46	37D	GPIO41	12F
41D	B_QGPO2	GPIO48	38D	GPIO43	13E
42D	B_QGPI2	GPIO49	40D	GPIO46	13F
43D	SGPIOC6	GPIO51	41D	GPIO48	14E
45D	MPIO8	GPIO54	42D	GPIO49	14B
46D	MPIO10	GPIO56	43D	GPIO51	15A
47D	MPIO12	GPIO57	45D	GPIO54	15B
48D	MPIO14	GPIO59	46D	GPIO56	16A
50D	MDA12	GPIO62	47D	GPIO57	16C
51D	MDA14	GPIO64	48D	GPIO59	16B
52D	MDA28	GPIO65	50D	GPIO62	17E
53D	MDA30	GPIO67	51D	GPIO64	17D
55D	MPWM0	GPIO70	52D	GPIO65	17F
56D	MPWM2	GPIO72	53D	GPIO67	18E
57D	MPWM16	GPIO73	55D	GPIO70	18F
58D	MPWM18	GPIO75	56D	GPIO72	19E
71D	B0EPEE	GPIO96	57D	GPIO73	19B
72D	ETRIG2	GPIO97	58D	GPIO75	20A
80D	B_AN77	GPIO110	60D	GPIO78	20B
81D	B_AN75	GPIO112	61D	GPIO80	21A
82D	B_AN73	GPIO113	62D	GPIO81	21C
83D	B_AN71	GPIO115	63D	GPIO83	21B
85D	B_AN69	GPIO118	65D	GPIO86	22E
86D	B_AN67	GPIO120	66D	GPIO88	22D
87D	B_AN65	GPIO121	67D	GPIO89	22F
88D	A_AN59	GPIO123	68D	GPIO91	23E
90D	A_AN57	GPIO126	70D	GPIO94	23F
91D	A_AN55	GPIO128	71D	GPIO96	24E
92D	A_AN53	GPIO129	72D	GPIO97	24B

phyCORE-MPC565		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
93D	A_AN51	GPIO131	73D	GPIO99	25A
95D	A_AN49	GPIO134	75D	GPIO102	25B
96D	A_AN47	GPIO136	76D	GPIO104	26A
97D	A_AN45	GPIO137	77D	GPIO105	26C
98D	VRL	GPIO139	78D	GPIO107	26B
100D	VRH	GPIO142	80D	GPIO110	27E

Table 22: Signal Pin Assignment for the phyCORE-MPC565 / Development Board / Expansion Board

phyCORE MPC565		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
+3V3	1C, 2C, 1D, 2D	3V3	1C, 2C, 1D, 2D	VCC1	1A, 1C
+5V	4C, 5C	5V	4C, 5C	VCC2	2A, 1B
+2V6	4D, 5D	2V6	4D, 5D	VCC3	2C, 1D
GND, GNDA	2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A, 82A, 87A, 92A, 97A, 4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B, 84B, 89B, 94B, 99B, 3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D, 72C, 77C, 82C, 87C, 92C, 97C, 74D, 79D, 84D, 89D, 94D, 99D	GND	2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A, 4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B, 3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 72C, 77C, 3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D, 74D, 79D	GND	3C, 4C, 7C, 8C, 9C, 12C, 13C, 14C, 17C, 18C, 19C, 22C, 23C, 24C, 27C, 29C, 30C, 31C, 34C, 35C, 36C, 39C, 40C, 41C, 44C, 45C, 46C, 49C, 50C, 51C, 54C, 4D, 5D, 6D, 9D, 10D, 11D, 14D, 15D, 16D, 19D, 20D, 21D, 24D, 25D, 26D, 28D, 31D, 32D, 33D, 36D, 37D, 38D, 41D, 42D, 43D, 46D, 47D, 48D, 51D, 52D, 53D, 1E, 2E

Table 23: Pin Assignment Power Supply for the phyCORE-MPC565 / Development Board / Expansion Board

11.3.9 Battery Connector BAT1

The mounting space BAT1 (see PCB stencil) is provided for connection of a battery that buffers the RTC on the phyCORE-MPC565. In the event of a VCC operating voltage failure the RTC is automatically supplied with power from the connected battery. The optional battery required for the RTC buffering is available through PHYTEC (order code BL-011).

11.3.10 DS2401 Silicon Serial Number

Communication to a DS2401 Silicon Serial Number can be implemented in various software applications for the definition of a node address or as copy protection in networked applications. The DS2401 can be soldered on space U8 or U9 on the Development Board, depending on the type of device packaging being used.

The Silicon Serial Number Chip mounted on the phyCORE Development Board PCM-991 can be connected to port pin MPIO2 of the MPC565 available at GPIO1 (JP27 = closed).

Jumper	Setting	Description
JP27	closed	Port pin MPIO2 (GPIO1) of the MPC565 is used to access the Silicon Serial Number

Table 24: JP27 Jumper Configuration for Silicon Serial Number Chip

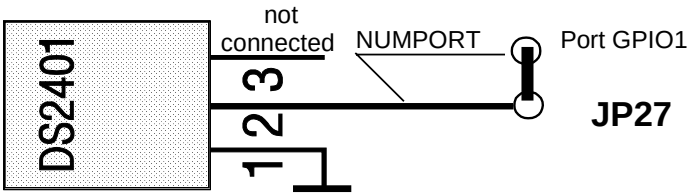


Figure 27: Connecting the DS2401 Silicon Serial Number

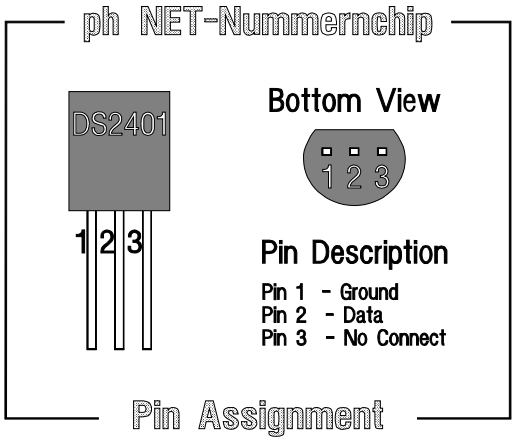


Figure 28: Pin Assignment of the DS2401 Silicon Serial Number

11.3.11 DB25 BDM/isp Connector P3

The DB-25 plug at P3 is used to connect the on-board BDM/isp-interface logic to the host-PC's printer port.

This port is used for two purposes:

- BDM debug functionality
- In-system-programming of the phyCORE-MPC565 EPLD

Jumper JP31 selects the function of this port:

Jumper	Default Setting	Description
JP31		Function of the signals at connector P3.
open	X	BDM debug port functionality.
closed		In-system programming functionality for the phyCORE EPLD device.

Table 25: JP31 P3 Connector Configuration

To establish the connection, a standard DB-25 extension cable (male-to-female) must be used. The cable length must not exceed 2 meters.

A set of associated jumpers is available to configure the on-board BDM interface.

Jumper	Default Setting	Description
JP30		Selection of the BDM supply voltage:
2 + 1		Connects +3V3 supply to the BDM circuits.
2 + 3	X	Connects +2V6 supply to the BDM circuits.
2 + 4		Connects +5V supply to the BDM circuits.
JP32 **JP33** **JP35** **JP36** **JP37**		DSDI signal DSCK signal VFLS0 signal VFLS0 signal DSDO signal
open		Disconnected from the processor.
closed	X	Connected to the processor.
JP34		Reset connection to the target:
open		Disconnected from the target board.
1 + 2		/PORESET
3 + 4		/RESEIN
5 + 6	X	/HDRESET
7 + 8		/SRESET
JP38		Reset connection to the development host:
open		Disconnected from the host.
1 + 2		/HDRESET
3 + 4	X	/SRESET

Table 26: Jumper Configuration for the P3 connection

Two LED's are provided to display the status of the target. If the phyCORE-MPC565 is held in debug mode, the red LED D10 will illuminate. D9 represents the status of the Reset line. As long as Reset is active D9 will illuminate.

11.3.12 BDM Pin Header Connector X5

The 10-pin header connector at X5 on the Development Board enables connection of an external BMD interface device.

Signal	Pin Number	Pin Number	Signal
VFLS0	1	2	/SRESET
GND	3	4	DSCK
GND	5	6	VFLS1
/HDRESET	7	8	DSDI
VBDM	9	10	DSDO

Table 27: Pin Assignment of the BDM Pin Header X5

Caution:
The following jumpers must removed before installing any external BDM interface:

- JP32, JP33, JP34, JP35, JP36, JP37 and JP38

If these jumpers are installed, the Development Board, the phyCORE module and the external BDM interface device will be damaged.

11.3.13 NEXUS Pin Header Connector X3

The pin header connector at X3 supports a standard 40-pin NEXUS debug connection (connector type AMP 104549-6) to various emulator probes.

Signal	Pin Number	Pin Number	Signal
/HDRESET	1	2	+2V6
/EVTI	3	4	+2V6
/RSTI	5	6	SGPIOC7
/MSEI	7	8	GND
MCKI	9	10	GND
MDI0	11	12	GND
Nc	13	14	GND
Nc	15	16	GND
/BG\VF0\LWP1	17	18	GND
/MSEO	19	20	GND
MCKO	21	22	GND
MDO0	23	24	GND
MDO1	25	26	GND
MDO2	27	28	GND
MDO3	29	30	GND
MDO4	31	32	GND
MDO5	33	34	GND
MDO6	35	36	GND
MDO7	37	38	GND
MDI1	39	40	GND

Table 28: Pin Assignment of the READI/NEXUS Pin Header X3

The location at X4 is unpopulated on the Development Board. The pin assignment of this 50-pin connector is a proprietary version of NEXUS port. *Refer to the board schematics for details about the pin assignment.*

12 Technical Specifications

The physical dimensions of the phyCORE-MPC565 are represented in *Figure 29.*

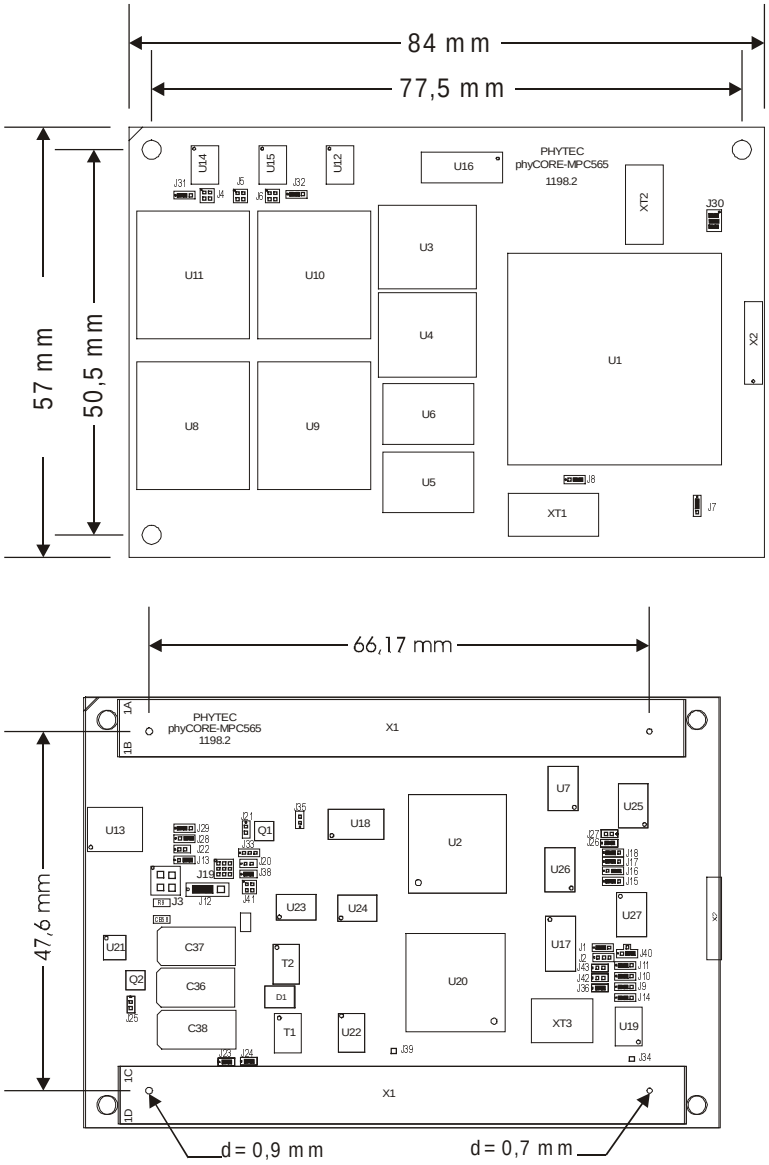


Figure 29: Physical Dimensions

The height of all components on the top side of the PCB is ca. 3 mm. The PCB itself is approximately 1.3 mm thick. The Molex connector pins are located on the underside of the PCB, oriented parallel to its two long sides. The maximum height of components on the underside of the PCB is 3 mm.

Additional Technical Data:

Parameter	Requirements	Characteristics
Dimensions		84 mm x 57 mm
Weight	With maximum circuitry installed	Approx. 40 grams
Humidity		Max. 95 % r.F. not condensed
Storage Temp. Range		-40° to +90°C
Operating Temp. Range: Standard Extended		 0 °C to +70 °C -40 °C to +90 °C
Operating voltages: Voltage 2.6 V Voltage 3.3 V Voltage 5 V		 2.6 .. 2.7 V 3.3 V ±3 % 5 V ±3 %
Operating Power Consumption: Voltage 2.6 V Voltage 3.3 V Voltage 5 V Voltage 2.6 V Voltage 3.3 V Voltage 5 V	56 MHz frequency 4 MByte SRAM 4 MByte Burst Flash 2 MByte stand. Flash 2 MByte SRAM 2 MByte stand. Flash	 Typ. 350 mA Typ. 300 mA Typ. 50 mA Typ. 250 mA Typ. 250 mA Typ. 50 mA

Table 29: Technical Data

These specifications describe the standard configuration of the phyCORE-MPC565 as of the printing of this manual.

Connectors on the phyCORE-MPC565:

Manufacturer	Molex
Number of pins per contact rows	200 (2 rows of 100 pins each)
Molex part number	52760-2009 (receptacle)

Two different heights are offered for the receptacle sockets that correspond to the connectors populating the underside of the phyCORE-MPC565. The given connector height indicates the distance between the two connected PCBs when the module is mounted on the corresponding carrier board. In order to get the exact spacing, the maximum component height (3 mm) on the underside of the phyCORE must be subtracted.

- Component height 6 mm

Manufacturer	Molex
Number of pins per contact row	200 (2 rows of 100 pins each)
Molex type number	55091-2009 (header)

- Component height 10 mm

Manufacturer	Molex
Number of pins per contact row	200 (2 rows of 100 pins each)

Please refer to the coresponding data sheets and mechanical specifications provided by Molex (www.molex.com).

13 Hints for Handling the Module

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Integrating the phyCORE-MPC565 in Application Circuitry

Successful integration in user target circuitry depends on whether the layout for the GND connections matches those of the phyCORE module. It is recommended that the target application circuitry is equipped with one layer dedicated to carry the GND potential. In any case, be sure to connect all GND pins neighboring signals which are used in the application circuitry. For the supply voltage, there must be contact with at least six of the GND pins neighboring the supply voltage pins.

14 Design Considerations - Check List

Please note the following points when implementing the phyCORE-MPC565 into target applications:

- Data line D31 represents the LSB and D0 the MSB.
- Address line A31 represents the LSB and A8 the MSB.
- Byte ordering is big Endian.
- Due to the conversion of little to big Endian byte ordering, the byte portions of CS8900A data bus are swapped to the MPC565 data bus. Respectively the processor recognizes the CS8900A register contents byte-swapped. The network data stream, read from the frame buffer, is supplied in correct Big Endian byte order.
- Data bus, address bus, control signals are not 5 V tolerant. Signal levels of up to 3.3 V are acceptable. Due to the different processor core voltage (2V6) and the periphery voltage (3V3), the initialization code has to set the PREDIS_EN bit contained in the MPC565 register PDMCR2.
- /IRQ5, /IRQ6, /IRQ7 are not 3.3 V tolerant due to the on-board MUX for IRQ and MODCK lines.
- ZZ is a wired-OR input to shut down the synchronous SRAM devices. Connect an open collector driver to GND.
- MPC565 I/O signals (not bus signals) need CMOS input level, e.g. 3.5 V to recognize a high-level on an input.
- Never connect signals to the MPC565 output drivers carrying a higher potentials (e.g. pull-ups) than the internal supply voltage.

For more information on the controller's I/O voltage range as well as other controller-related features *please refer to the detailed MPC565 User's Manual provided by Motorola.*

15 Revision History

Date	Version numbers	Changes in this manual
22-April-2003	Manual L-635e_1 PCM-019 PCB# 1198.1 PCM-991 PCB# 1209.1	First edition.
23-May-2003	Manual L-635e_2 PCM-019 PCB# 1198.2 PCM-991 PCB#1209.1	Second edition. Do not use this edition for PCB#1198.1 Various changes in section 3, Jumpers. Update for PCB#1198.2. Description for Burst Mode Flash added in section 6.3.2. Also see section Release Notes for comparison to PCB#1198.1 Section 11.2.2, Jumper on the phyCORE Development Board PCM-991, Table 10, Error in Default Settings at JP20 corrected.
19-Sept.-2003	Manual L-635e_3 PCM-019 PCB# 1198.2 PCM-991 PCB# 1209.1	Table 1, section 36 - 80D (page 21 to 22) deleted. Table 1, Pin 56C connection corrected. Table 2, footnote: J41 added Figure 8, internal Flash memory, J33 corrected. Following page, starting from external / internal Flash, J33 corrected. Table 29, Standard Extended corrected.
11-Nov.-2003	Manual L-635e_4 PCM-019 PCB# 1198.2 PCM-991 PCB# 1209.1	Table 1, description for I^2C signals SCL (31C) and SDA (32D) as well as signal name for pin 93D (A_AN51) Section 6.5, I^2C bus signal names corrected (MPC565 controller lines MDA14 and MDA15 can be used). Section 10, I^2C bus signal names corrected.
03-Mar.-2004	Manual L-635e_5 PCM-019 PCB# 1198.2 PCM-991 PCB# 1209.1	Comments added to pin description for pin # 31C and 37D. Description expanded for J1, J2, J41 in section 3. J41 added in section 6.4. Technical data added in section 12. Comments added in section 14. Figure 6: J20 and J38 corrected Table 7: J19, J20, J41 corrected
13-April-2004	Manual L-635e_6 PCM-019 PCB# 1198.2 PCM-991 PCB# 1209.1	Technical Data added in *Table 6* *Table 26*: J38 SRESET signal corrected *Figure 12:* Molex connectors A/B, C/D corrected.

A Appendices

A.1 Release Notes

The following section contains information about deviations to the description in this manual. Revisions to previous manuals are also listed.

Caution:
This manual exclusively describes the board revision 1198.2

Revision: PCB# 1198.1

- Burst mode Flash works in synchronous mode up to 40MHz.
- TPU A_T2CLK and B_T2CLK have pull-down resistors.

Revision: PCB# 1198.2

Comparison to 1198.1:

- New Burst-Mode Flash devices Am29BDD160G (2MByte).

  Two independent 32-bit devices. Address arrangement of both devices depends via Jumper J40. The default configuration (J40=2+3) locates the first device to address 0x0 and the second device to address 0x800000 (8 MByte) relative to the base address of the processor's Chip Select signal (default /CS0). These devices support up to 56 MHz bus frequency
- Additional solder jumpers (J1, J2, J36, J42 and J43) to hard-wire processor Chip Select signals direct to the on-board memory devices. A system operation without EPLD is now supported.
- Pull-up resistors are now connected to the TPU clock inputs A_T2CLK, B_T2CLK and C_T2CLK.
- The EPLD pin assignment has slightly changed. The following pins have been altered: 98, 99, 100, 3, 14, 15, 56, 58
  Solder jumper J35 is provided to connect (default=open) pin 53 (PLDIO0) to the global clock input 89 (CIN).
- Additional solder jumper J41 (default=open) to hard-wire the SRAM bank address signals BA0 and BA1 to GND.

- The resistors R60 and R61 now connect the processor's peripheral signals MDA14 and MDA15 to the local I²C bus signals SCL and SDA. These resistors are not populated for the standard version of the phyCORE-MPC565. The I²C bus signals should be connected to the desired signals externally. For example, on the Development Board PCM-991, MDA14 (JP18) and MDA15 (JP19) are routed to the I²C signals.
- During power-down the current consumption has not been fully characterized. Especially on the +5V supply side additional current is still drawn and will not decrease to less than 10 mA.

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Document: **phyCORE-MPC565**
Document number: **L-635e_6, April 2004**

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Published by PHYTEC

Ordering No. L-635e_6
Printed in Germany